ENCM 467 Lab 3
Static and Dynamic Behaviour of CMOS logic Gates

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1 CMOS Digital Logic Gates

There are 2 digital logic gates that will be used throughout this lab, a CMOS NAND gate (figure 1) and CMOS NOR gate (figure 2).

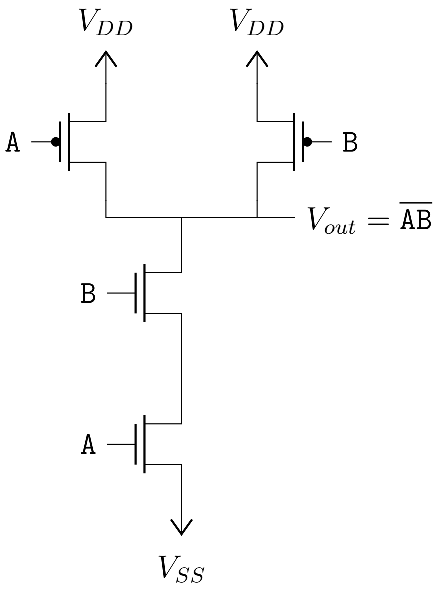


Figure 1: A CMOS NAND Gate

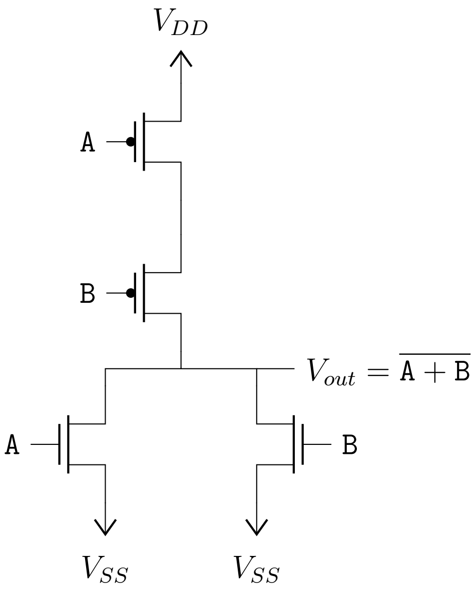
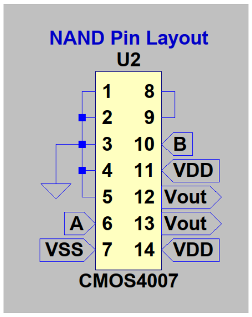


Figure 2: A CMOS NOR Gate

The NAND and NOR gates are implemented in LTspice using the CD 4007 CMOS integrated circuit as shown in figures 3 and 4 respectively. All inputs not used are tied to ground to prevent floating inputs.



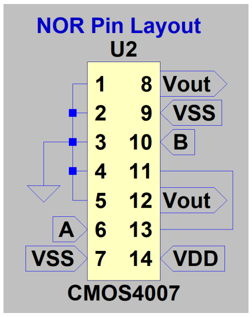


Figure 3: The NAND circuit built in LTspice. Figure 4: The NOR circuit built in LTspice.

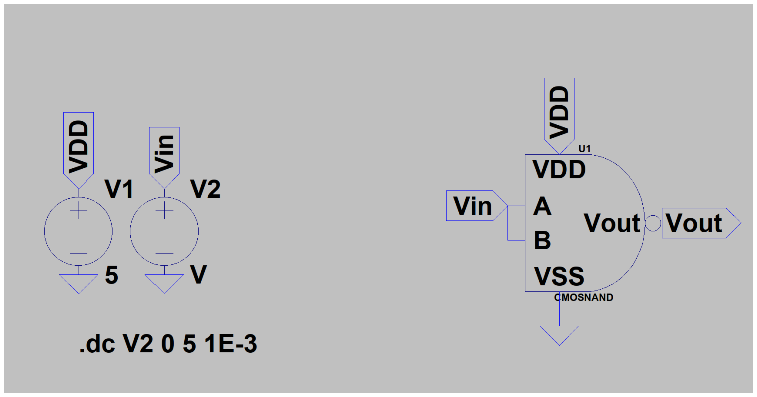
The NAND and NOR circuits are then exported as a sub circuit similar to the CMOS4007 component so that they can be reused throughout the rest of the lab as a discrete component.

2 Logic Gate Measurements

2.1 Static Behaviour of CMOS NAND and NOR Gates

2.1.1 NAND Gate Measurements

The static measurements of the CMOS NAND gate is done using the circuit setup in LTspice shown in figure 5. Note that the NAND gate use (as with all NAND gates in the lab) is the NAND gate as designed in section 1.



```
.dc V2 0 5 1E-3
```

Figure 5: The NAND gate circuit in LTspice for measuring the static properties of the NAND gate.

When the DC analysis is run on the circuit above the voltage transfer curve in figure 6 is generated.

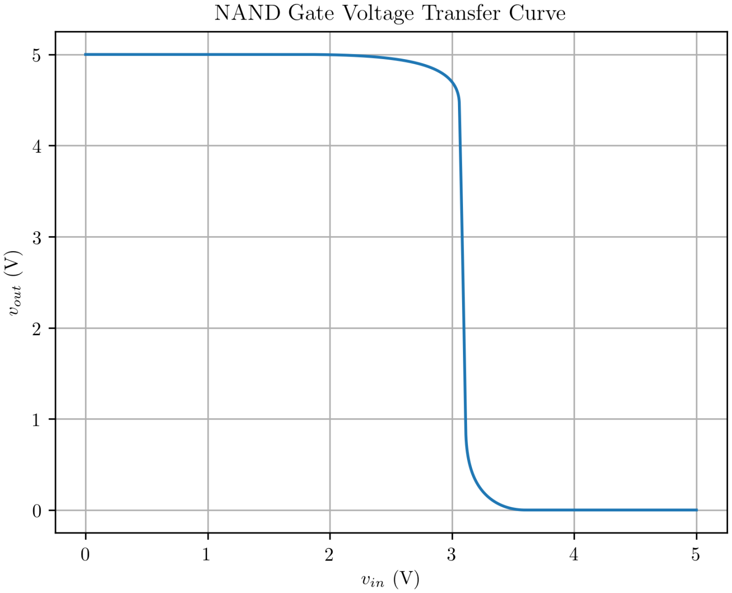


Figure 6: The Voltage transfer characteristics for the CMOS NAND gate.

Then the python code in appendix A is used to caluclate the critical voltage values which are given in table 1.

Table 1: The critical voltages for the CMOS NAND gate.

	Voltage (V)
V_{IL}	2.942
V_{IH}	3.321
V_{OH}	5
V_{OL}	0
V_{INV}	3.055
NM_L	2.942
NM_H	1.679

2.1.2 NOR Gate Measurements

The static measurements of the CMOS NOR gate is done using the circuit setup in LTspice shown in figure 7. Note that the NOR gate use (as with all NOR gates in the lab) is the NOR gate as designed in section 1.

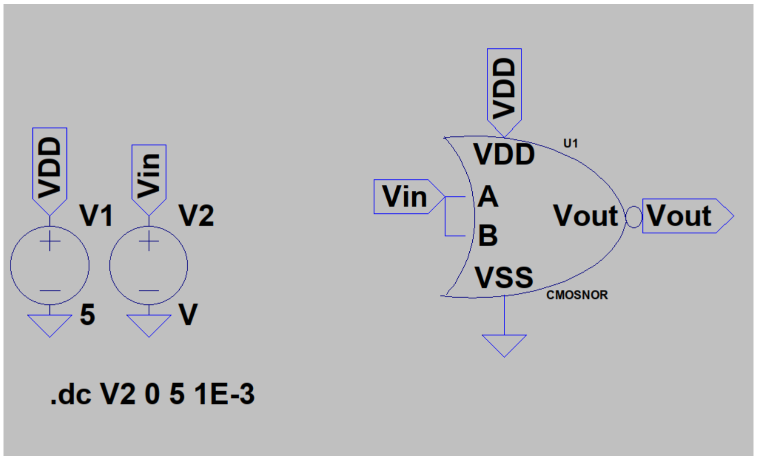


Figure 7: The NOR gate circuit in LTspice for measuring the static properties of the NOR gate.

When the DC analysis is run on the circuit above the voltage transfer curve in figure 8 is generated.

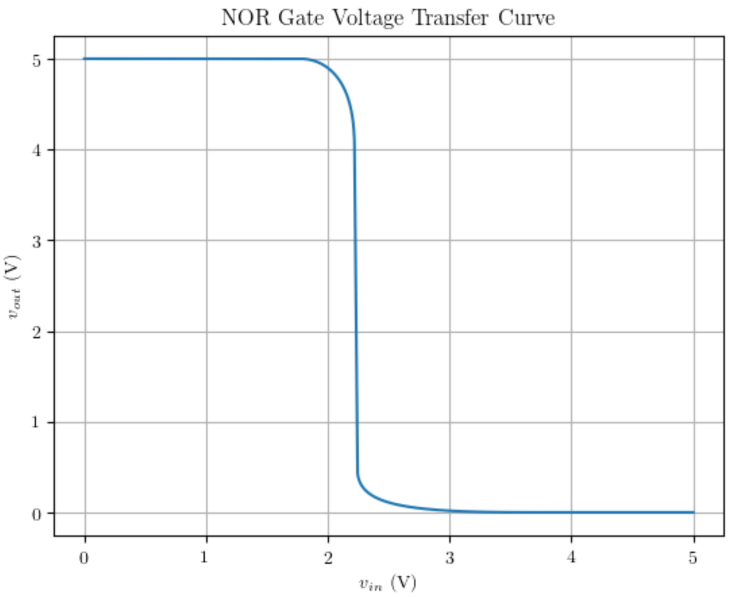


Figure 8: The Voltage transfer characteristics for the CMOS NOR gate.

Then the python code in appendix A is used to caluclate the critical voltage values which are given in table 2.

Table 2: The critical voltages for the CMOS NOR gate.

	Voltage (V)
V_{IL}	1.997
V_{IH}	2.339
V_{OH}	5
V_{OL}	0
V_{INV}	2.226
NM_L	1.997
NM_H	2.661

2.1.3 Static Gate Properties Analysis

Recall that for a CMOS inverter V_{INV} is given by

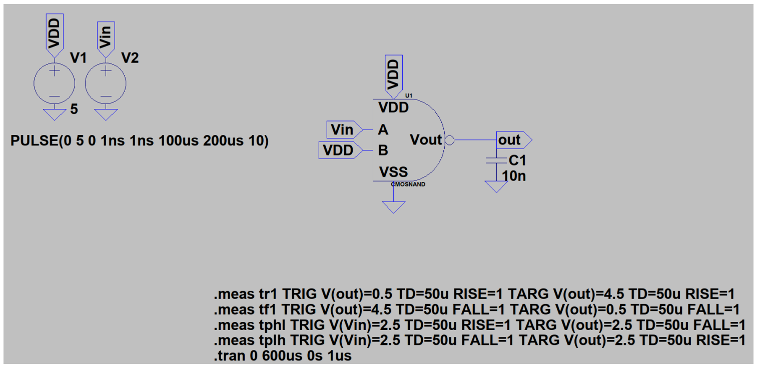
$$V_{INV} = \frac{V_{T0(n)} + \sqrt{\frac{k_p}{k_n}}(V_{DD} - |V_{T0(p)}|)}{1 + \sqrt{\frac{k_p}{k_n}}} \tag{1}$$

From equation (1) we can see that the threshold voltage is related to $\left(\frac{W}{L}\right)_p \left(\frac{L}{W}\right)_n$. We know that for an ideal inverter $W_p = 2W_n$ which roughly corresponds to a $V_{INV} = \frac{V_{DD}}{2}$. If we assume the width of the PMOS transistors used in the circuit is twice that of the NMOS, then we would have a width ratio of $2\frac{2W}{L}$ for the PMOS and $\frac{W}{2L}$ for the NMOS in the NAND gate. This would scale $\frac{k_p}{k_n}$ by a factor of 4 which would increase the inversion voltage which is what we see in the NAND gate. Similarly for the NOR gate, if we assume the width of the PMOS transistor used in the circuit is twice that of the NMOS, then we would have a width ration of $\frac{W}{L}$ for the PMOS transistors and $\frac{2W}{L}$ for the NMOS transistors. This would scale $\frac{k_p}{k_n}$ by a factor of $\frac{1}{4}$ decreasing the inversion voltage which is what we see for the NOR gate. As the other critical voltages are also related to $\frac{k_p}{k_n}$ a similar argument can be made.

2.2 Dynamic Behaviour of CMOS NAND and NOR gates

2.2.1 NAND Gate Measurements

NAND Gate Measurements With Variable `A` Input The dynamic measurements of the CMOS NAND with the variable `A` input is done using the circuit setup in LTspice shown in figure 9.



```
PULSE(0 5 0 1ns 1ns 100us 200us 10)
```

```
.meas tr1 TRIG V(out)=0.5 TD=50u RISE=1 TARG V(out)=4.5 TD=50u RISE=1
.meas tf1 TRIG V(out)=4.5 TD=50u FALL=1 TARG V(out)=0.5 TD=50u FALL=1
.meas tphl TRIG V(Vin)=2.5 TD=50u RISE=1 TARG V(out)=2.5 TD=50u FALL=1
.meas tplh TRIG V(Vin)=2.5 TD=50u FALL=1 TARG V(out)=2.5 TD=50u RISE=1
.tran 0 600us 0s 1us
```

Figure 9: The NAND gate circuit in LTspice for measuring the dynamic properties of the NAND gate with `A` as a variable input

When the transient analysis is run on the circuit above the response in figure 10 is generated.

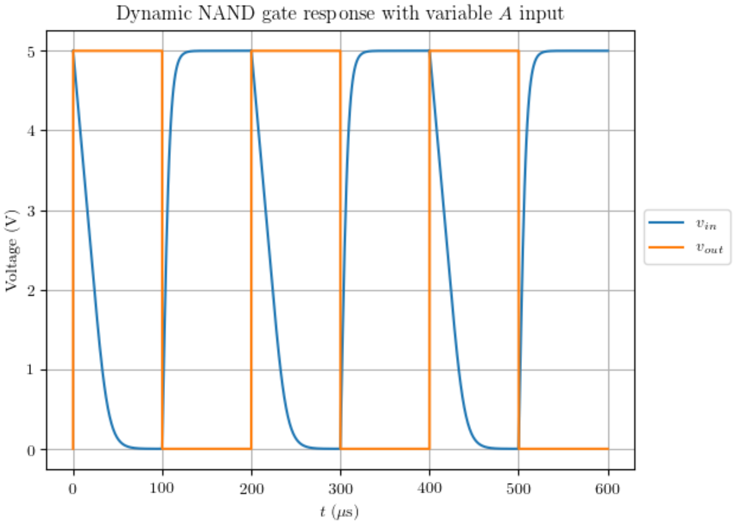


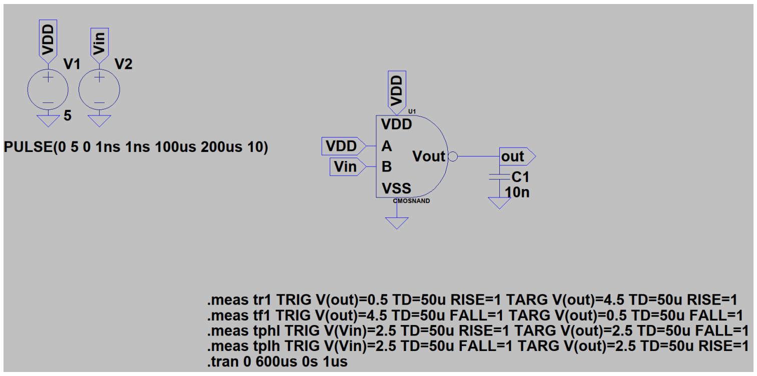
Figure 10: The transient response for the CMOS NAND gate with a variable `A` input and constant `B` input.

Then the measure statements in the circuit are used to determine the timing values given in table 3.

Table 3: The timing values for the CMOS NAND gate with variable `A` input.

	Time (μs)
t_{rise}	11.606
t_{fall}	35.274
t_{PLH}	4.685
t_{PHL}	19.973
t_s	12.329

NAND Gate Measurements With Variable `B` Input The dynamic measurements of the CMOS NAND with the variable `B` input is done using the circuit setup in LTspice shown in figure 11.



```
PULSE(0 5 0 1ns 1ns 100us 200us 10)
```

```
.meas tr1 TRIG V(out)=0.5 TD=50u RISE=1 TARG V(out)=4.5 TD=50u RISE=1
.meas tf1 TRIG V(out)=4.5 TD=50u FALL=1 TARG V(out)=0.5 TD=50u FALL=1
.meas tphl TRIG V(Vin)=2.5 TD=50u RISE=1 TARG V(out)=2.5 TD=50u FALL=1
.meas tplh TRIG V(Vin)=2.5 TD=50u FALL=1 TARG V(out)=2.5 TD=50u RISE=1
.tran 0 600us 0s 1us
```

Figure 11: The NAND gate circuit in LTspice for measuring the dynamic properties of the NAND gate with `B` as a variable input

When the transient analysis is run on the circuit above the response in figure 12 is generated.

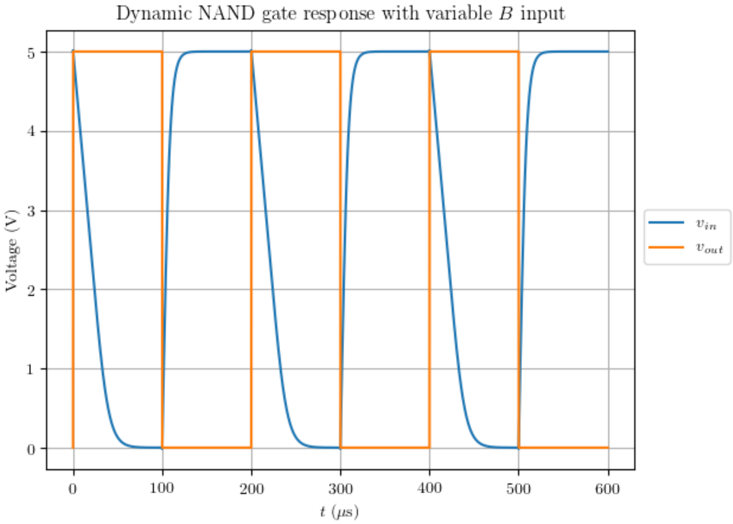


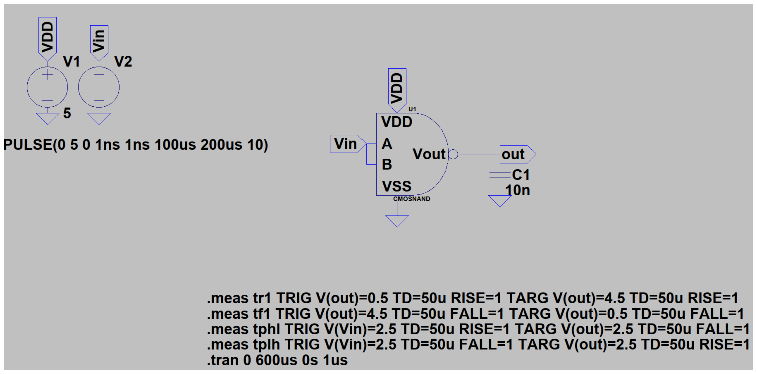
Figure 12: The transient response for the CMOS NAND gate with a variable `B` input and constant `A` input.

Then the measure statements in the circuit are used to determine the timing values given in table 4.

Table 4: The timing values for the CMOS NAND gate with variable `B` input.

	Time (μs)
t_{rise}	11.594
t_{fall}	35.268
t_{PLH}	4.703
t_{PHL}	20.006
t_s	12.355

NAND Gate Measurements With Common Variable Inputs The dynamic measurements of the CMOS NAND with the connected variable inputs is done using the circuit setup in LTspice shown in figure 13.



```
.meas tr1 TRIG V(out)=0.5 TD=50u RISE=1 TARG V(out)=4.5 TD=50u RISE=1
.meas tf1 TRIG V(out)=4.5 TD=50u FALL=1 TARG V(out)=0.5 TD=50u FALL=1
.meas tphl TRIG V(Vin)=2.5 TD=50u RISE=1 TARG V(out)=2.5 TD=50u FALL=1
.meas tplh TRIG V(Vin)=2.5 TD=50u FALL=1 TARG V(out)=2.5 TD=50u RISE=1
.tran 0 600us 0s 1us
```

Figure 13: The NAND gate circuit in LTspice for measuring the dynamic properties of the NAND gate with a common variable input

When the transient analysis is run on the circuit above the response in figure 14 is generated.

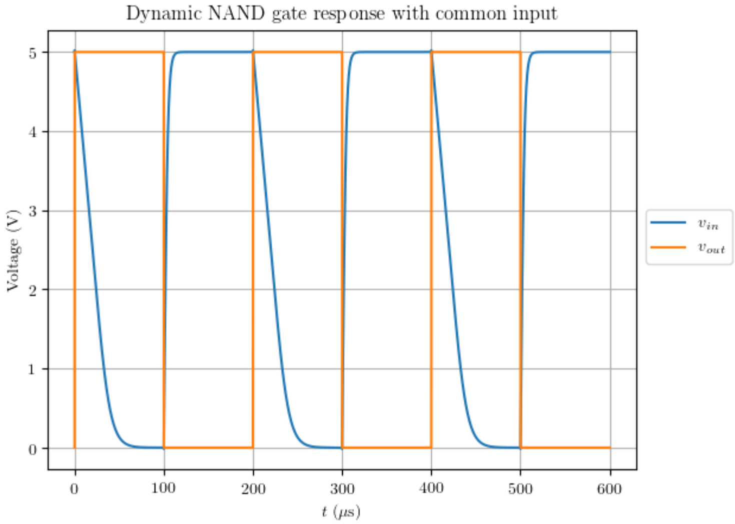


Figure 14: The transient response for the CMOS NAND gate with a common variable input.

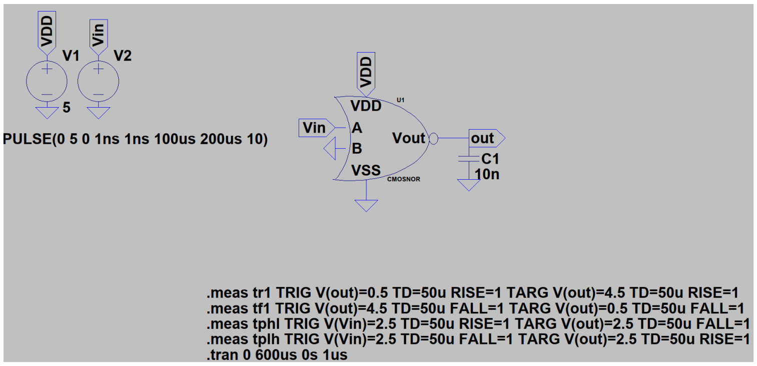
Then the measure statements in the circuit are used to determine the timing values given in table 5.

Table 5: The timing values for the CMOS NAND gate with common variable inputs.

	$Time$ (μs)
t_{rise}	5.895
t_{fall}	35.275
t_{PLH}	2.411
t_{PHL}	20.087
t_s	11.249

2.2.2 NOR Gate Measurements

NOR Gate Measurements With Variable `A` Input The dynamic measurements of the CMOS NOR with the variable `A` input is done using the circuit setup in LTspice shown in figure 15.



```
PULSE(0 5 0 1ns 1ns 100us 200us 10)
```

```
.meas tr1 TRIG V(out)=0.5 TD=50u RISE=1 TARG V(out)=4.5 TD=50u RISE=1
.meas tf1 TRIG V(out)=4.5 TD=50u FALL=1 TARG V(out)=0.5 TD=50u FALL=1
.meas tphl TRIG V(Vin)=2.5 TD=50u RISE=1 TARG V(out)=2.5 TD=50u FALL=1
.meas tplh TRIG V(Vin)=2.5 TD=50u FALL=1 TARG V(out)=2.5 TD=50u RISE=1
.tran 0 600us 0s 1us
```

Figure 15: The NOR gate circuit in LTspice for measuring the dynamic properties of the NOR gate with `A` as a variable input

When the transient analysis is run on the circuit above the response in figure 16 is generated.

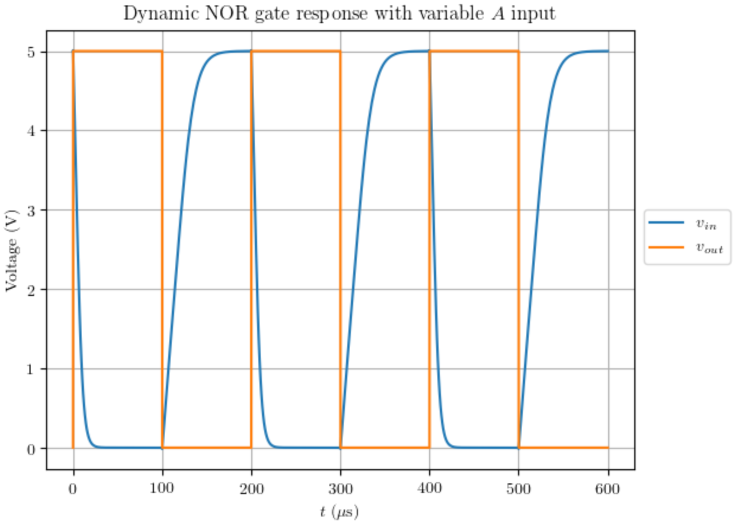


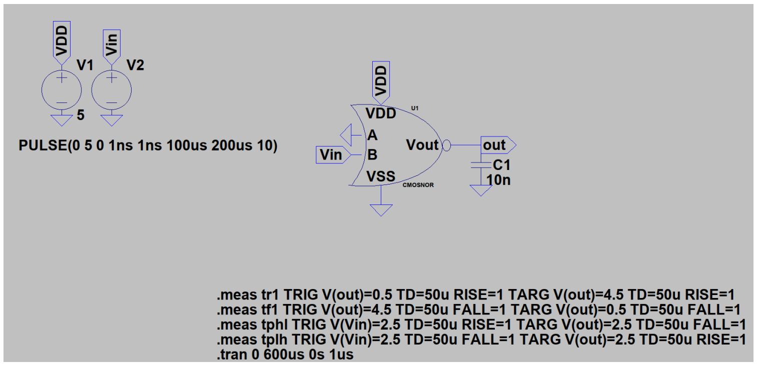
Figure 16: The transient response for the CMOS NOR gate with a variable `A` input and constant `B` input.

Then the measure statements in the circuit are used to determine the timing values given in table 6.

Table 6: The timing values for the CMOS NOR gate with variable A input.

	Time (μs)
t_{rise}	34.327
t_{fall}	11.515
t_{PLH}	17.868
t_{PHL}	5.390
t_s	11.629

NOR Gate Measurements With Variable B Input The dynamic measurements of the CMOS NOR with the variable B input is done using the circuit setup in LTspice shown in figure 17.



```
.meas tr1 TRIG V(out)=0.5 TD=50u RISE=1 TARG V(out)=4.5 TD=50u RISE=1
.meas tf1 TRIG V(out)=4.5 TD=50u FALL=1 TARG V(out)=0.5 TD=50u FALL=1
.meas tphl TRIG V(Vin)=2.5 TD=50u RISE=1 TARG V(out)=2.5 TD=50u FALL=1
.meas tplh TRIG V(Vin)=2.5 TD=50u FALL=1 TARG V(out)=2.5 TD=50u RISE=1
.tran 0 600us 0s 1us
```

Figure 17: The NOR gate circuit in LTspice for measuring the dynamic properties of the NOR gate with B as a variable input

When the transient analysis is run on the circuit above the response in figure 18 is generated.

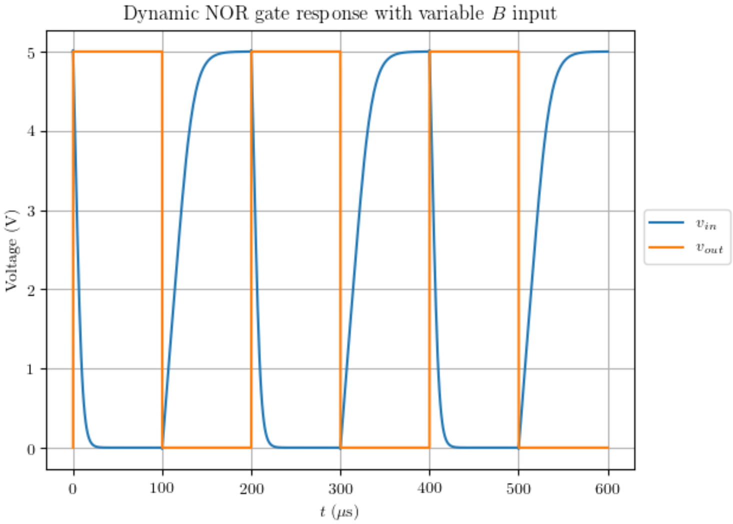


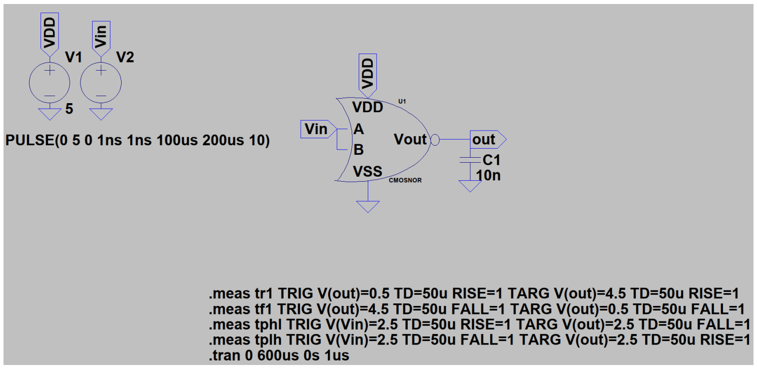
Figure 18: The transient response for the CMOS NOR gate with a variable B input and constant A input.

Then the measure statements in the circuit are used to determine the timing values given in table 7.

Table 7: The timing values for the CMOS NOR gate with variable `B` input.

	Time (μs)
t_{rise}	34.318
t_{fall}	11.498
t_{PLH}	17.837
t_{PHL}	5.372
t_s	11.605

NOR Gate Measurements With Common Variable Inputs The dynamic measurements of the CMOS NOR with the connected variable inputs is done using the circuit setup in LTspice shown in figure 19.



```
.meas tr1 TRIG V(out)=0.5 TD=50u RISE=1 TARG V(out)=4.5 TD=50u RISE=1
.meas tf1 TRIG V(out)=4.5 TD=50u FALL=1 TARG V(out)=0.5 TD=50u FALL=1
.meas tphl TRIG V(Vin)=2.5 TD=50u RISE=1 TARG V(out)=2.5 TD=50u FALL=1
.meas tplh TRIG V(Vin)=2.5 TD=50u FALL=1 TARG V(out)=2.5 TD=50u RISE=1
.tran 0 600us 0s 1us
```

Figure 19: The NOR gate circuit in LTspice for measuring the dynamic properties of the NOR gate with a common variable input

When the transient analysis is run on the circuit above the response in figure 20 is generated.

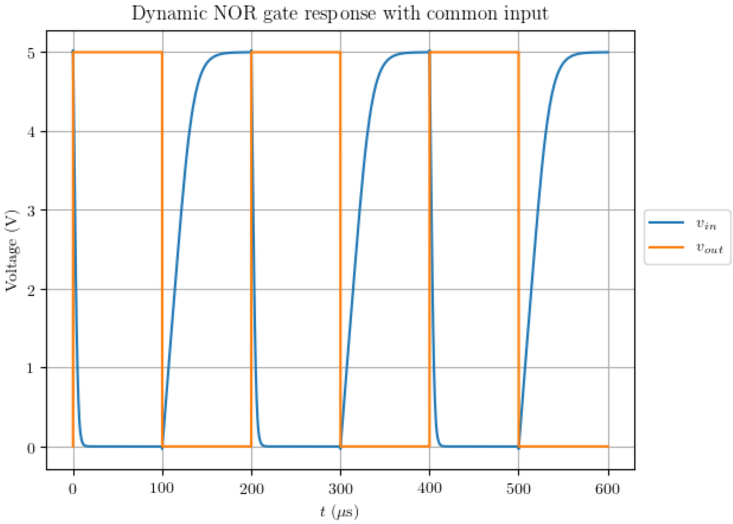


Figure 20: The transient response for the CMOS NOR gate with a common variable input.

Then the measure statements in the circuit are used to determine the timing values given in table 8.

Table 8: The timing values for the CMOS NOR gate with common variable inputs.

	Time (μs)
t_{rise}	34.235
t_{fall}	5.872
t_{PLH}	17.949
t_{PHL}	2.726
t_s	10.338

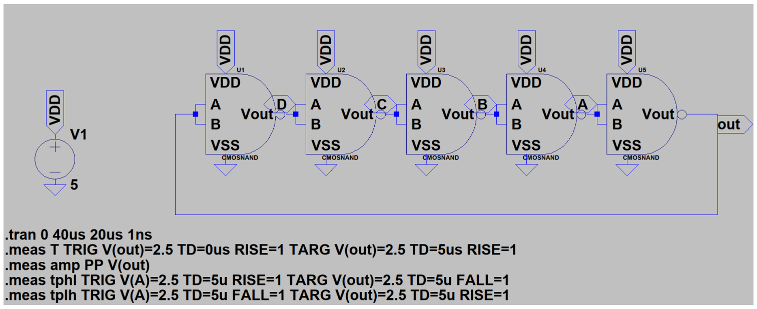
2.2.3 Analysis of Transient Response of CMOS NAND and NOR Gates

As seen from both the graphs and data the NAND gate rises significantly faster then the NOR gate, and the NOR gate falls significantly faster than the NAND gate. If we recall the circuit for the NAND gate in figure 1 we see that for the gate to pull up from a logic 0 to 1 we only need to "go through" one MOSFET. However for the NOR gate in figure 2 to pull up from a logic 0 to 1 we need to "go through" two transistors in series which will take more time to switch due to the added capacitance and resistance. A similar argument can be made as to why the NOR gate falls faster then the NAND gate.

When the NAND gate has both inputs tied to a common voltage it rises about 2 times faster then when only 1 input is switched. When `A` and `B` switch from high to low at the same time both transistors in parallel will begin to pull up. This halfs the resistance of the circuit cutting the RC time constant roughly in half causing the delay to half. A similar argument can be made for why the NOR gate falls roughly 2 times faster when using a common input as opposed to 1 input being switched.

2.3 CMOS Ring Oscillator

The CMOS ring oscillator circuit is built using NAND gates in LTspice as shown in figure 21.



```
.tran 0 40us 20us 1ns
.meas T TRIG V(out)=2.5 TD=0us RISE=1 TARG V(out)=2.5 TD=5us RISE=1
.meas amp PP V(out)
.meas tphl TRIG V(A)=2.5 TD=5u RISE=1 TARG V(out)=2.5 TD=5u FALL=1
.meas tplh TRIG V(A)=2.5 TD=5u FALL=1 TARG V(out)=2.5 TD=5u RISE=1
```

Figure 21: The CMOS ring oscillator circuit built in LTspice.

The circuit above then generates the periodic response shown in figure 22. Note that the graph is from $20\mu s$ to $40\mu s$. The first $20\mu s$ are ignored as the start up is not the oscillation motion we are looking for.

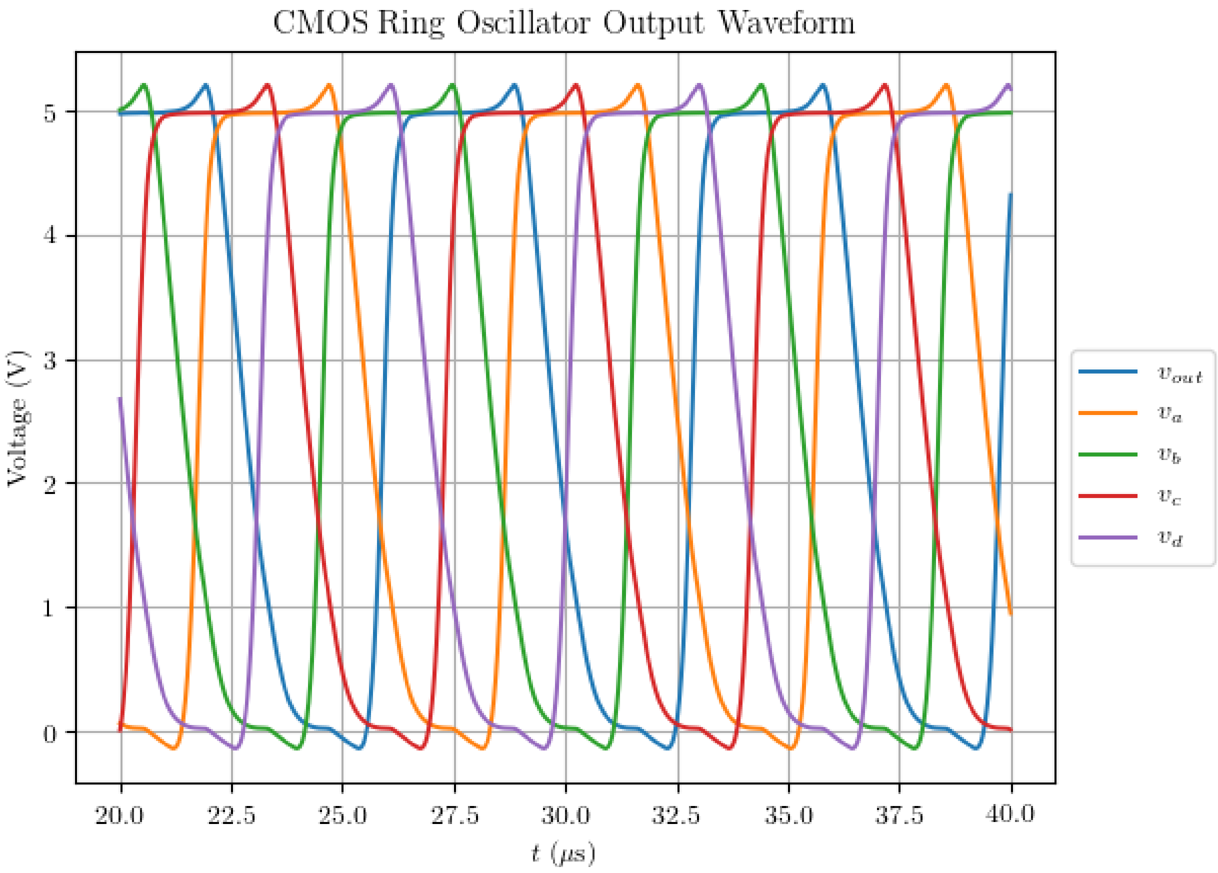


Figure 22: The oscillation of the CMOS ring oscillator circuit.

The measure statements in the LTspice simulation measure the critical values which are shown in table 9.

Table 9: The Measured Values of the CMOS Ring Oscillator.

	Value
t_s	692.928 ns
f	144.311 kHz
A	4.90 V
T	6.929 μs

2.3.1 Analysis of CMOS Ring Oscillator

For the CMOS ring oscillator we find an average propagation delay for the NAND gate of 693 ns compared to the 11.2 μs of the NAND gate with common inputs from section 2.2.1. The reason the NAND gates in the ring oscillator have such a significantly lower propagation delay is due to fan out. We know that

$$t_s = Nt_{s0}\left(1 + \frac{\sqrt[N]{\frac{C_L}{C_{g,1}}}}{\gamma}\right) \tag{2}$$

Assuming that C_L and $C_{g,1}$ are constant between both cases, that $\gamma = 1$ and that the input capacitance is around $20pF$ [1] then t_s will be approximately $25t_{s0}$ for the ring oscillator but is almost $500t_{s0}$ for the stand alone NAND gate. As such we expect that the t_s will be much smaller for the ring oscillator then the NAND gate on its own which is what we see.

Looking at figure 22 we can see that when 1 signal has finished rising the next signal in the chain begins to fall and that this occurs N times in 1 period where N is the number of inverters in the ring. From this we can see that,

$$T = N(t_{PLH} + t_{PHL}) \tag{3}$$

However we can use the fact that t_s is the average of t_{PLH} and t_{PHL} to write this as

$$T = 2Nt_s \tag{4}$$

Using our measured propagation delay and equation (4) we would find our period to be 6.93 μs which is what we measured, experimentally verifying our result.

[1] Based on the gate capacitance from the CD4007 LTspice component.

Appendices

A Python Code for Data Analysis

```python
#!/usr/bin/env python3

from matplotlib import pyplot as plt
import numpy as np

plt.rcdefaults()
plt.figure(dpi=300)
plt.rc('text', usetex=True)
plt.rc('font', family='serif')


def read_data(path, n_cols):
    cols = [np.array([])] * n_cols
    with open(path) as _file:
        _file.readline()
        for line in _file:
            if line == '\n':
                continue
            tmp = line.split('\t')
            for i, col in enumerate(cols):
                cols[i] = np.append(col, np.float(float(tmp[i])))
    return cols


def find_points(data):
    v_in = data[0]
    v_out = data[1]
    dv_out= np.diff(v_out)/(v_in[1] - v_in[0])

    min_dif = np.abs(v_in - v_out)
    index = np.where(np.isclose(min_dif, np.min(min_dif)))
    v_inv = index
    v_ol = v_out[-1]
    v_oh = v_out[0]
    v_il = 0
    v_ih = -1
    set_ih = False

    for i, dv in enumerate(dv_out):
        if not set_ih and dv >= -1:
            v_il = i
        elif not set_ih:
            set_ih = True
        if dv <= -1 and set_ih:
            v_ih = i
    v_il += 1
    v_ih += 1
    print(’Vinv: ’, v_out[v_inv])
    print(’Vol:’, v_ol)
    print(’Voh’, v_oh)
    print(’Vil’, v_in[v_il])
    print(’Vih’, v_in[v_ih])
    print(’NML’, v_in[v_il] - v_ol)
    print(’NMH’, v_oh - v_in[v_ih])
    return v_inv, v_il, v_ih


# Part 21 NAND gate
data = read_data(’./data/part_21_NAND.txt’, 2)
find_points(data)
plt.plot(data[0], data[1])
plt.title(’NAND Gate Voltage Transfer Curve’)
plt.xlabel(’$v_{in}$ (V)’)
plt.ylabel(’$v_{out}$ (V)’)
plt.grid()
#plt.legend(bbox_to_anchor=(1.01 , 0.6), loc=’upper left’, borderaxespad=0.2)
plt.savefig("./figures/part_21_NAND.png", bbox_inches=’tight’)
plt.close()


# Part 21 NOR gate
data = read_data(’./data/part_21_NOR.txt’, 2)
find_points(data)
plt.title(’NOR Gate Voltage Transfer Curve’)
plt.xlabel(’$v_{in}$ (V)’)
plt.ylabel(’$v_{out}$ (V)’)
plt.grid()
plt.plot(data[0], data[1])
plt.savefig("./figures/part_21_NOR.png", bbox_inches="tight")
plt.close()


# Part 22 NAND Gate A in
data = read_data(’./data/part_22_NAND_A.txt’, 3)
plt.plot(data[0]/1E-6, data[1], label=’$v_{in}$’)
plt.plot(data[0]/1E-6, data[2], label='$v_{out}$')
plt.title('Dynamic NAND gate response with variable $A$ input')
plt.xlabel('$t$ ($\mu$s)')
plt.ylabel('Voltage (V)')
plt.grid()
plt.legend(bbox_to_anchor=(1.01, 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig('./figures/part_22_NAND_A.png', bbox_inches='tight')
plt.close()


# Part 22 NAND Gate B in
data = read_data('./data/part_22_NAND_B.txt', 3)
plt.plot(data[0]/1E-6, data[1], label='$v_{in}$')
plt.plot(data[0]/1E-6, data[2], label='$v_{out}$')
plt.title('Dynamic NAND gate response with variable $B$ input')
plt.xlabel('$t$ ($\mu$s)')
plt.ylabel('Voltage (V)')
plt.grid()
plt.legend(bbox_to_anchor=(1.01, 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig('./figures/part_22_NAND_B.png', bbox_inches='tight')
plt.close()


# Part 22 NAND Gate AB in
data = read_data('./data/part_22_NAND_AB.txt', 3)
plt.plot(data[0]/1E-6, data[1], label='$v_{in}$')
plt.plot(data[0]/1E-6, data[2], label='$v_{out}$')
plt.title('Dynamic NAND gate response with common input')
plt.xlabel('$t$ ($\mu$s)')
plt.ylabel('Voltage (V)')
plt.grid()
plt.legend(bbox_to_anchor=(1.01, 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig('./figures/part_22_NAND_AB.png', bbox_inches='tight')
plt.close()


# Part 22 NOR Gate A in
data = read_data('./data/part_22_NOR_A.txt', 3)
plt.plot(data[0]/1E-6, data[1], label='$v_{in}$')
plt.plot(data[0]/1E-6, data[2], label='$v_{out}$')
plt.title('Dynamic NOR gate response with variable $A$ input')
plt.xlabel('$t$ ($\mu$s)')
plt.ylabel('Voltage (V)')
plt.grid()
plt.legend(bbox_to_anchor=(1.01, 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig('./figures/part_22_NOR_A.png', bbox_inches='tight')
plt.close()


# Part 22 NOR Gate B in
data = read_data('./data/part_22_NOR_B.txt', 3)
plt.plot(data[0]/1E-6, data[1], label='$v_{in}$')
plt.plot(data[0]/1E-6, data[2], label='$v_{out}$')
plt.title('Dynamic NOR gate response with variable $B$ input')
plt.xlabel('$t$ ($\mu$s)')
plt.ylabel('Voltage (V)')
plt.grid()
plt.legend(bbox_to_anchor=(1.01, 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig('./figures/part_22_NOR_B.png', bbox_inches='tight')
plt.close()


# Part 22 NOR Gate AB in
data = read_data('./data/part_22_NOR_AB.txt', 3)
plt.plot(data[0]/1E-6, data[1], label='$v_{in}$')
plt.plot(data[0]/1E-6, data[2], label='$v_{out}$')
plt.title('Dynamic NOR gate response with common input')
plt.xlabel('$t$ ($\mu$s)')
plt.ylabel('Voltage (V)')
plt.grid()
plt.legend(bbox_to_anchor=(1.01, 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig('./figures/part_22_NOR_AB.png', bbox_inches='tight')
plt.close()


# Part 23
data = read_data('./data/part_23.txt', 6)
plt.plot(data[0]/1E-6 + 20, data[1], label='$v_{out}$')
plt.plot(data[0]/1E-6 + 20, data[2], label='$v_a$')
plt.plot(data[0]/1E-6 + 20, data[3], label='$v_b$')
plt.plot(data[0]/1E-6 + 20, data[4], label='$v_c$')
plt.plot(data[0]/1E-6 + 20, data[5], label='$v_d$')
plt.grid()
plt.title('CMOS Ring Oscillator Output Waveform')
plt.xlabel('$t$ ($\mu$s)')
plt.ylabel('Voltage (V)')
plt.legend(bbox_to_anchor=(1.01, 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig('./figures/part_23.png', bbox_inches='tight')
plt.close()
plt.plot(data[0]/1E-6 + 20, data[1], label='$v_{out}$')
plt.plot(data[0]/1E-6 + 20, data[2], label='$v_a$')
plt.grid()
plt.title('CMOS Ring Oscillator Output Waveform')
plt.xlabel('$t$ ($\mu$s)')
plt.ylabel('Voltage (V)')
plt.legend(bbox_to_anchor=(1.01, 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig('./figures/part_23_reduced.png', bbox_inches='tight')
plt.close()
```