ENCM 467 Lab 2
Static and Dynamic Behaviour of MOSFET inverters

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1 Static Inverter Measurements

1.1 Static Linearly Loaded Inverter

In LT spice the Linearly loaded inverter is built as shown below,

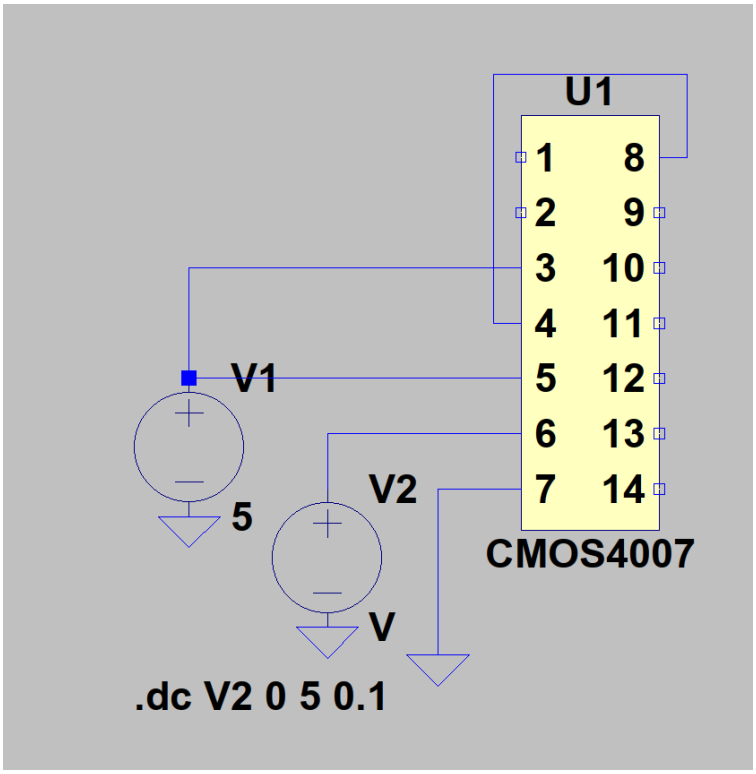

Figure 1: The Linearly Loaded inverter in LT Spice with the load NMOS in Saturation

The following is the voltage transfer characteristic is obtained for the circuit in figure 1.

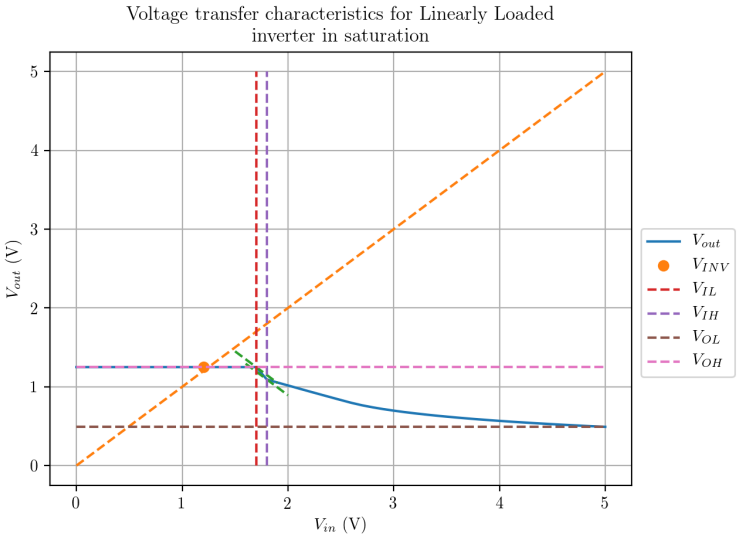

Figure 2: The voltage transfer characteristics for the linearly loaded inverter from figure 1.

The critical points in figure 2 are calculated using the python script in appendix A and are given in the table in appendix B. The python script using the following formulas to calculate the data in the table in appendix B.

$$\left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_{IL}} = -1 \tag{1}$$

$$\left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_{IH}} = -1 \tag{2}$$

$$\left.V_{out}\right|_{V_{in}=0V} = V_{OH} \tag{3}$$

$$\left.V_{out}\right|_{V_{in}=5V} = V_{OL} \tag{4}$$

$$\left.V_{out}\right|_{V_{in}=V_{INV}} = V_{in} \tag{5}$$

$$G = \frac{V_{OL} - V_{OH}}{V_{IH} - V_{IL}} \tag{6}$$

$$NM_L = V_{IL} - V_{OL} \tag{7}$$

$$NM_H = V_{OH} - V_{IH} \tag{8}$$

Next the linearly loaded inverter is modified to have the load nMOS in triode. As the body is grounded, $V_B \neq V_S$ so the body effect must be considered. This raises the threshold voltage for the nMOS so we must raise the gate voltage higher to place the nMOS into triode. I chose to raise the gate voltage to 10V which should be high enough to place the nMOS device in triode. The modified circuit is shown below.

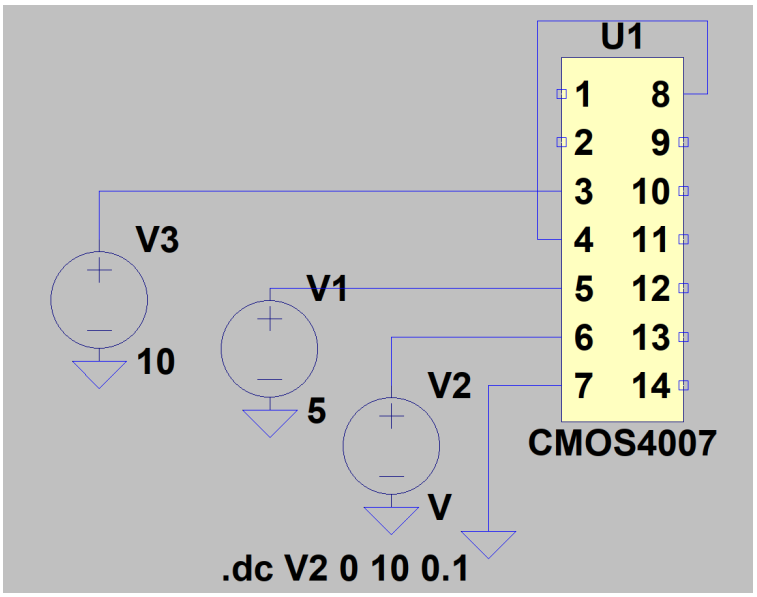

Figure 3: The linearly loaded inverter in LT spice with the load nMOS in triode.

The voltage transfer plot is then given below.

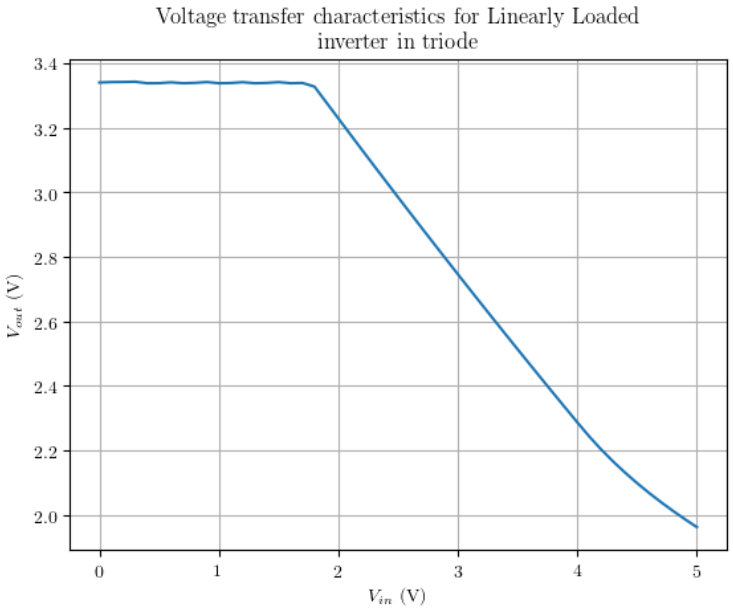

Figure 4: The voltage transfer characteristics for the linearly loaded inverter in triode.

The critical values are calculated again using the python script in Appendix A. However as the slope of the VTC is always greater than -1, the definitions of V_{IL} and V_{IH} can't be met, so 0V and 5V will be used respectively for calculating noise margins and gain.

1.2 Static CMOS Inverter

The CMOS inverter is built in LT spice as shown below.

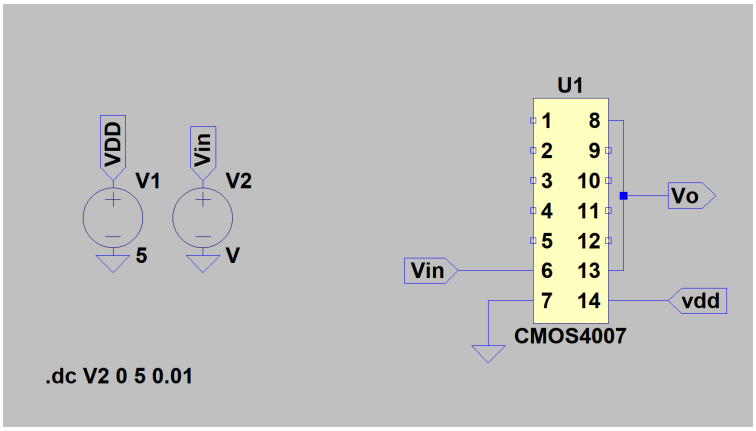

Figure 5: The CMOS inverter in LT Spice

The voltage transfer curve of the circuit in figure 5 is shown below.

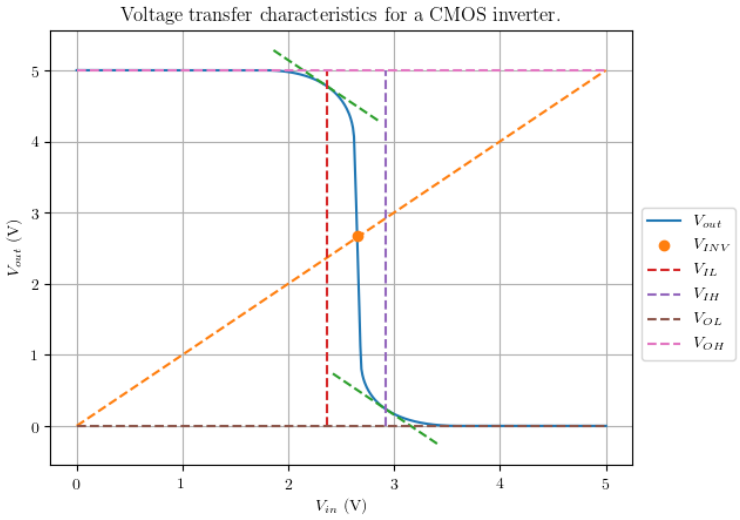

Figure 6: The voltage transfer characteristic of the CMOS inverter from figure 5.

The critical CMOS values are calculated using the python script from appendix A and are given in the table in appendix B.

1.3 Analysis of Static Inverter Behaviour

First we will look at the linearly loaded inverter in saturation. Its two major advantages are a high low noise margin ($NM_L = 1.21V$) and a gain comparable to the CMOS ($G = -7.5$). However its disadvantages far out way its advantages. It drains power when in a static

position of logic 1 or 0, has a negative high noise margin ($NM_H = -0.560V$), and its logic levels are very bad for a 5V logic system.
Next we will look at the linearly loaded inverter in with the load in triode. Its two major advantages over the previous design are a higher max output voltage and the inverter threshold voltage lies is more centered between the min and max output voltages. However again its disadvantages far out way the advantages. This setup requires an external power supply for the gate voltage, and has negative noise margins for both the high and low logic levels.
Finally we will look at the CMOS inverter. The CMOS inverters advantages are clear. It has large noise margins for both the high and low logic levels, has rail to rail operation, doesn't drain power when at a static voltage level (besides from leakage currents), and has a high gain. The disadvantages of the CMOS are much fewer, but it is more expensive to produce and will take more chip area then the saturated linearly loaded inverter as the pMOS needs a larger area.
Neither the saturated or triode linearly loaded inverter are useful as a gate in a digital system. Both designs have negative noise margins making them incredibly prone to logic errors without an additional converter to fix the logic levels.

2 Dynamic Inverter Measurements

2.1 Dynamic Resistively Loaded Inverter Measurements

The resistively loaded inverter built in LT spice shown below is put through a transient response.

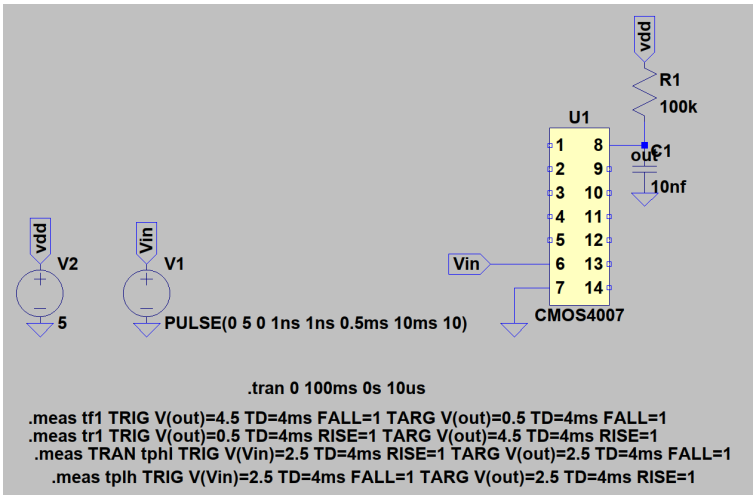

Figure 7: The resistively loaded inverter built in LT Spice

The transient response is shown below.

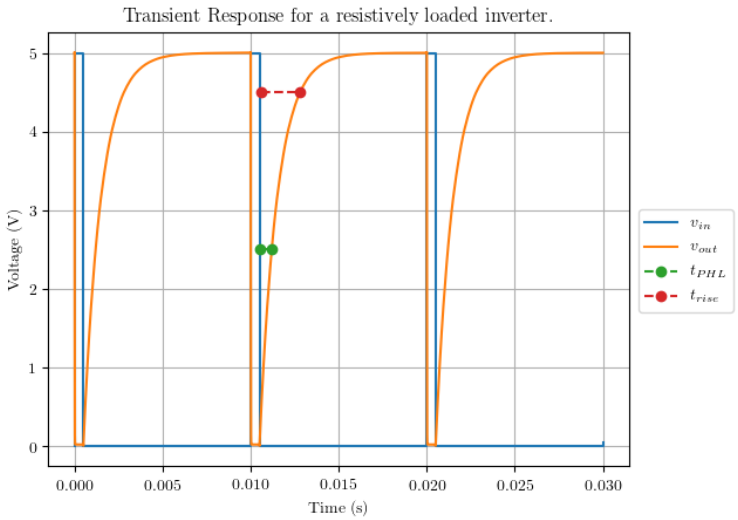

Figure 8: The transient response of the resistively loaded inverter. Note that as t_{fall} and t_{PHL} are both very small compared to t_{rise} and t_{PLH} they aren't shown on the graph.

The critical times are calculated using the measure statements in the LT spice circuit. t_{rise} is the time it takes for the output voltage to rise from 10% V_{DD} to 90% V_{DD}. Similarly t_{fall} is teh time it takes for the output voltage to fall from 90% V_{DD} to 10% V_{DD}. t_{PHL} and t_{PLH} are the times it takes for the voltage to reach $\frac{1}{2}V_{DD}$ when the output is falling and rising respectively. t_s is the average of t_{PHL} and t_{PLH}. The rise and fall times are so drastically different do to the charging and discharging of the capacitor through different paths. When V_{in} goes high the nMOS enters triode. This causes it to act as a resistor with resistance in the $k\Omega$. The charged capacitor then discharges through the nMOS to ground. When V_{in} goes low, the nMOS becomes cut off so the capacitor will start charging through the 100k resistor. Because the 100k resistor is about 2 orders of magnitude greater in resistance then the nMOS in triode, it takes about 100 times as long for the voltage to rise as opposed to fall.

2.2 Dynamic CMOS measurements

The CMOS inverter built in LT spice shown below is put through a transient response.

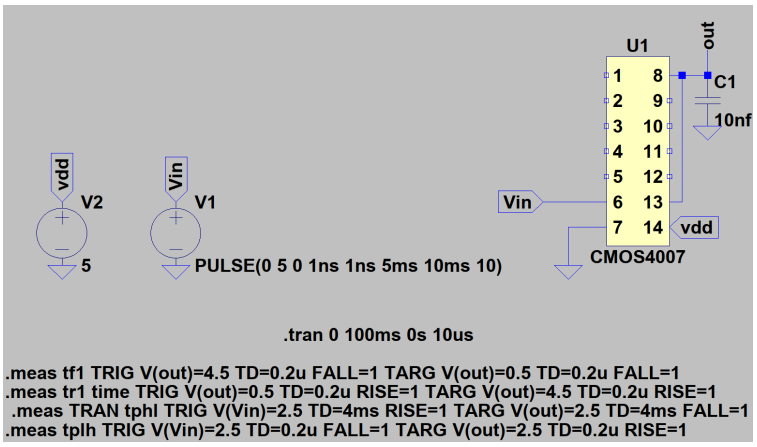

Figure 9: The CMOS inverter circuit with transient analysis

The transient response is then shown below,

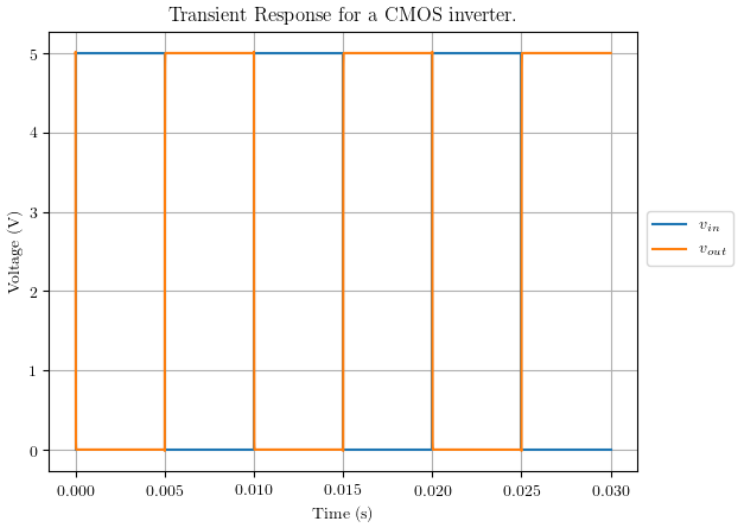

Figure 10: The transient response of the CMOS inverter. Note that as the timings are very small compared to the 100Hz clock they aren't shown on the graph.

The timing values are again calculated using the measure statements in LT spice and are shown in the table in appendix B.

2.3 Analysis of Dynamic response

While the CMOS and resistively loaded inverter have similar fall times, the rise time of the resistively loaded inverter is significantly higher then the CMOS inverter. This makes the CMOS inverter preferable for higher speed applications as it can be switched on and off much faster then the resistively loaded inverter without logic errors occurring.
Both the CMOS and resistively loaded inverters are effected by the internal capacitances of the MOSFETs used to make them and load capacitance in determining the total propagation

delay. However as discussed above the load resistor in the resistively loaded inverter greatly adds to the rise time.

Appendices

A Python Code for Data Analysis

```
#!/usr/bin/env python3

from matplotlib import pyplot as plt
import numpy as np

plt.rcdefaults()
plt.figure(dpi=200)
plt.rc('text', usetex=True)
plt.rc('font', family='serif')


def read_data(path, n_cols):
    cols = [np.array([])] * n_cols
    with open(path) as _file:
        _file.readline()
        for line in _file:
            if line == '\n':
                continue
            tmp = line.split('\t')
            for i, col in enumerate(cols):
                cols[i] = np.append(col, np.float(float(tmp[i])))
    return cols


def find_points(data):
    v_in = data[0]
    v_out = data[1]
    dv_out= np.diff(v_out)/(v_in[1] - v_in[0])

    min_dif = np.abs(v_in - v_out)
    index = np.where(np.isclose(min_dif, np.min(min_dif)))
    v_inv = index
    v_ol = v_out[-1]
    v_oh = v_out[0]
    v_il = 0
    v_ih = -1
    set_ih = False

    for i, dv in enumerate(dv_out):
        if not set_ih and dv >= -1:
```

```
            v_il = i
        elif not set_ih:
            set_ih = True
        if dv <= -1 and set_ih:
            v_ih = i
    v_il += 1
    v_ih += 1
    print(v_out[v_inv], v_ol, v_oh, v_in[v_il], v_in[v_ih])
    return v_inv, v_il, v_ih


# Graph for part 2a Saturation
data = read_data('data/part2a_sat.txt', 2)
plt.plot(data[0], data[1], label='$V_{out}$')
v_inv, v_il, v_ih = find_points(data)
plt.plot((0, 5), (0, 5), '--C1')
plt.plot(data[0][v_inv], data[1][v_inv], 'oC1', label='$V_{INV}$')
plt.plot((data[0][v_il] - 0.2, data[0][v_il] + 0.2),
         (data[1][v_il] + 0.2, data[1][v_il] - 0.2), '--C2')

plt.plot((data[0][v_ih] - 0.2, data[0][v_ih] + 0.2),
         (data[1][v_ih] + 0.2, data[1][v_ih] - 0.2), '--C2')
plt.plot((data[0][v_il], data[0][v_il]), (0, 5), '--C3', label='$V_{IL}$')
plt.plot((data[0][v_ih], data[0][v_ih]), (0, 5), '--C4', label='$V_{IH}$')
plt.plot((0, 5), (data[1][-1], data[1][-1]), '--C5', label='$V_{OL}$')
plt.plot((0, 5), (data[1][0], data[1][0]), '--C6', label='$V_{OH}$')

plt.title('Voltage transfer characteristics for Linearly Loaded\ninverter'
          ' in saturation')
plt.xlabel('$V_{in}$ (V)')
plt.ylabel('$V_{out}$ (V)')
plt.grid()
plt.legend(bbox_to_anchor=(1.01 , 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig("./figures/part_2a_sat.png", bbox_inches='tight')
plt.close()


# Graph for part 2a Triode
data = read_data('data/part2a_tri.txt', 2)
plt.plot(data[0], data[1])
find_points(data)
plt.title('Voltage transfer characteristics for Linearly Loaded\ninverter'
          ' in triode')
plt.xlabel('$V_{in}$ (V)')
plt.ylabel('$V_{out}$ (V)')
```

```
plt.grid()
plt.savefig("./figures/part_2a_tri.png", bbox_inches='tight')
plt.close()


# Graph for part 2b CMOS inverter
data = read_data('data/part2b.txt', 2)
plt.plot(data[0], data[1], label='$V_{out}$')
v_inv, v_il, v_ih = find_points(data)
plt.plot((0, 5), (0, 5), '--C1')
plt.plot(data[0][v_inv], data[1][v_inv], 'oC1', label='$V_{INV}$')
plt.plot((data[0][v_il] - 0.5, data[0][v_il] + 0.5),
         (data[1][v_il] + 0.5, data[1][v_il] - 0.5), '--C2')

plt.plot((data[0][v_ih] - 0.5, data[0][v_ih] + 0.5),
         (data[1][v_ih] + 0.5, data[1][v_ih] - 0.5), '--C2')
plt.plot((data[0][v_il], data[0][v_il]), (0, 5), '--C3', label='$V_{IL}$')
plt.plot((data[0][v_ih], data[0][v_ih]), (0, 5), '--C4', label='$V_{IH}$')
plt.plot((0, 5), (data[1][-1], data[1][-1]), '--C5', label='$V_{OL}$')
plt.plot((0, 5), (data[1][0], data[1][0]), '--C6', label='$V_{OH}$')

plt.title('Voltage transfer characteristics for a CMOS inverter.')
plt.xlabel('$V_{in}$ (V)')
plt.ylabel('$V_{out}$ (V)')
plt.grid()
plt.legend(bbox_to_anchor=(1.01 , 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig("./figures/part_2b.png", bbox_inches='tight')
plt.close()


# Graph for part 3a
data = read_data('data/part3a.txt', 3)
plt.plot(data[0][:460], data[1][:460], label='$v_{in}$')
plt.plot(data[0][:460], data[2][:460], label='$v_{out}$')
plt.title('Transient Response for a resistively loaded inverter.')
plt.plot((10.5E-3, 10.5E-3+0.695822E-3), (2.5, 2.5), '--o', label='$t_{PHL}$')
plt.plot((0.0106056, 0.0128063), (4.5, 4.5), '--o', label='$t_{rise}$')
plt.xlabel('Time (s)')
plt.ylabel('Voltage (V)')
plt.grid()
plt.legend(bbox_to_anchor=(1.01 , 0.6), loc='upper left', borderaxespad=0.2)
plt.savefig("./figures/part_3a.png", bbox_inches='tight')
plt.close()
```

```
# Graph for part 3b
data = read_data('data/part3b.txt', 3)
plt.plot(data[0][:300], data[1][:300], label='$v_{in}$')
plt.plot(data[0][:300], data[2][:300], label='$v_{out}$')
plt.title('Transient Response for a CMOS inverter.')
plt.legend(bbox_to_anchor=(1.01 , 0.6), loc='upper left', borderaxespad=0.2)
plt.xlabel('Time (s)')
plt.ylabel('Voltage (V)')
plt.grid()
plt.savefig("./figures/part_3b.png", bbox_inches='tight')
plt.close()
```

B Data Tables

Table 1: Static Values for the Inverter Voltage Transfer Characteristics

	Linearly Loaded Saturation	Linearly Loaded Triode	CMOS
V_{IL}	1.7	N/A (0)	2.35
V_{IH}	1.8	N/A (5)	2.92
V_{OH}	1.25	3.40	5
V_{OL}	0.49	1.96	0
V_{INV}	1.25	2.84	2.67
Gain at V_{INV}	-7.5	-0.288	-8.77
NM_L	1.21	-1.96	2.35
NM_H	-0.560	-1.6	2.08

Table 2: Dynamic values measured for the resistively loaded inverter and the CMOS inverter.

	Resistively Loaded Inverter	CMOS inverter
t_{rise}	2.20 ms	11.72 μs
t_{fall}	11.69 μs	11.66 μs
t_{PHL}	5.39 μs	5.42 μs
t_{PLH}	0.695 ms	4.77 μs
t_s	350 μs	5.10 μs