ENCM 467 Lab 4
Building Digital Logic Systems

William Doan
Taras Kuzyk
Andreas Smit

December 7, 2020

1 CMOS Digital Logic Gates

There are 4 digital logic gates that will be used throughout this lab, a CMOS NAND gate (figure 1), a CMOS NOR gate (figure 2), a CMOS XOR gate (figure 3) and a CMOS NOT gate (figure 4).

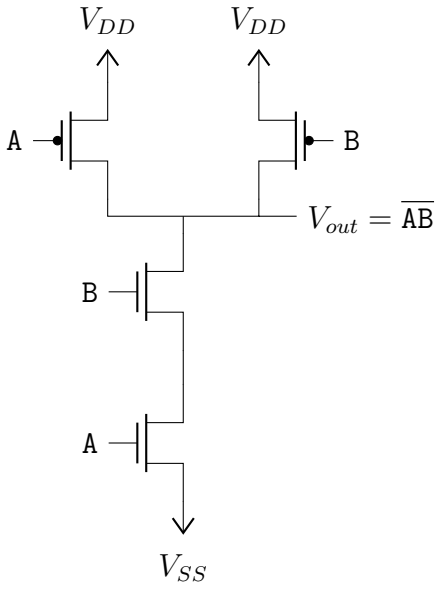

Figure 1: A CMOS NAND Gate

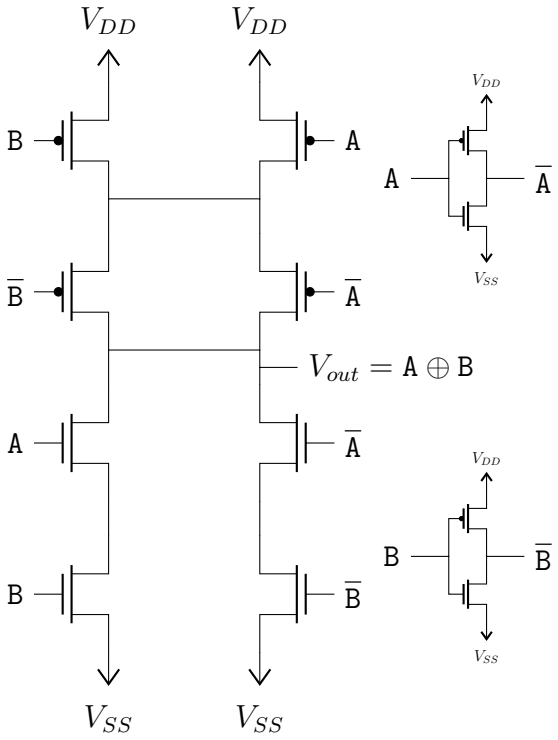

Figure 3: A CMOS XOR Gate

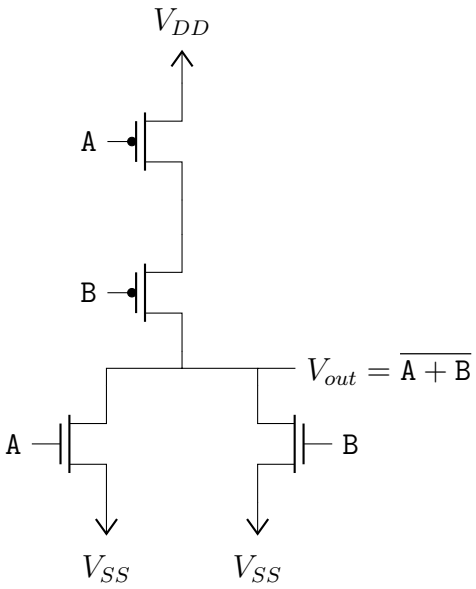

Figure 2: A CMOS NOR Gate

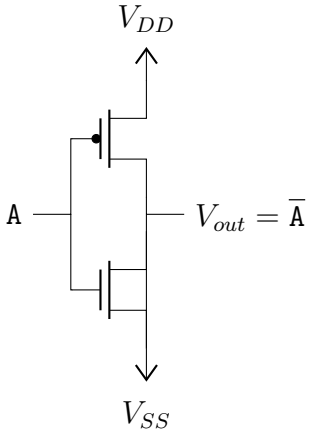

Figure 4: A CMOS NOT Gate

The NAND, NOR, XOR, and NOT gates are implemented in LTspice using the CD 4007 CMOS integrated circuit as shown in figures 5, 6, 7, and 8 respectively. All inputs not used

are tied to ground to prevent floating inputs.

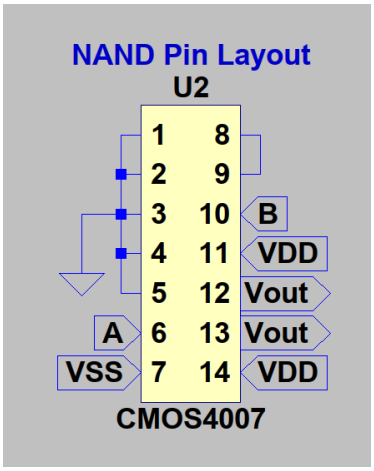

Figure 5: The NAND circuit built in LTspice.

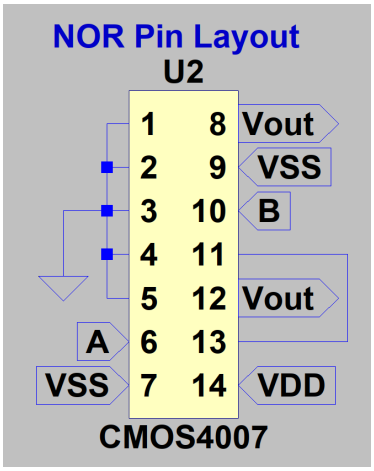

Figure 6: The NOR circuit built in LTspice.

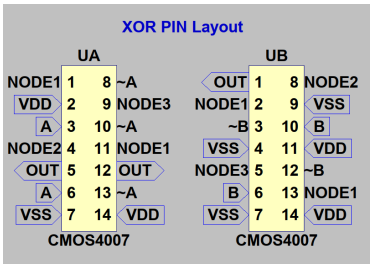

Figure 7: The XOR circuit built in LTspice.

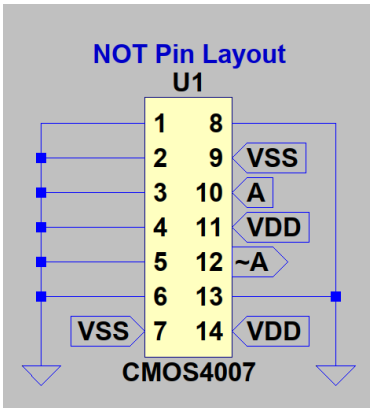

Figure 8: The NOT circuit built in LTspice.

The NAND, NOR, XOR, and NOT circuits are then exported as a sub circuit similar to the CMOS4007 component so that they can be reused throughout the rest of the lab as a discrete component.

2 Two Bit Adder

A two bit adder circuit is built using the components defined in section 1 using LTspice (shown in figure 9.

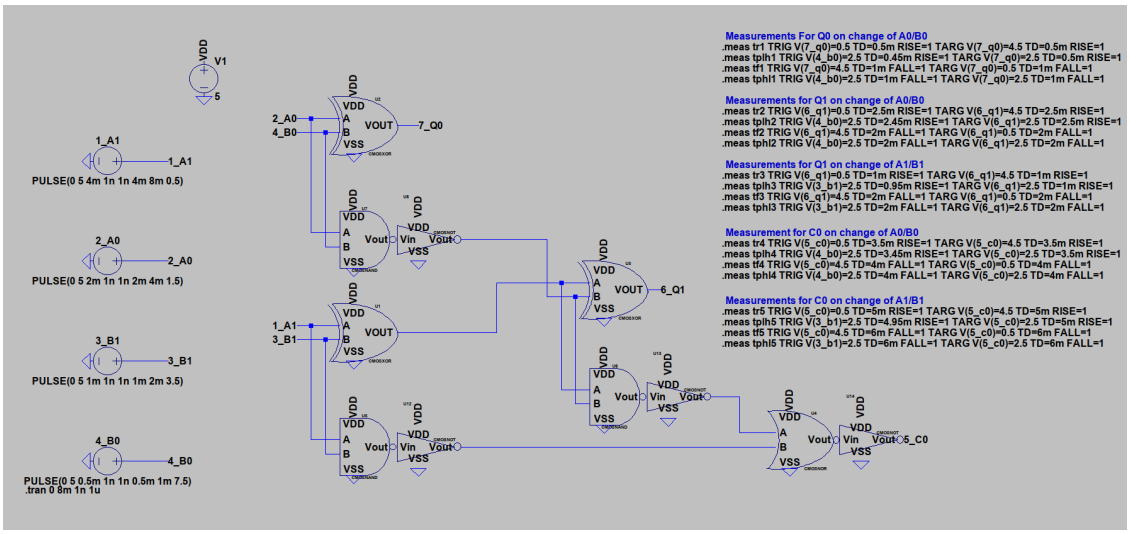

Figure 9: The 2-bit full adder built in LTspice.

2.1 Timing Diagram

The outputs are then measured over the course of 8ms as the inputs are stimulated. The outputs and inputs are shown in the timing diagram in figure 10.

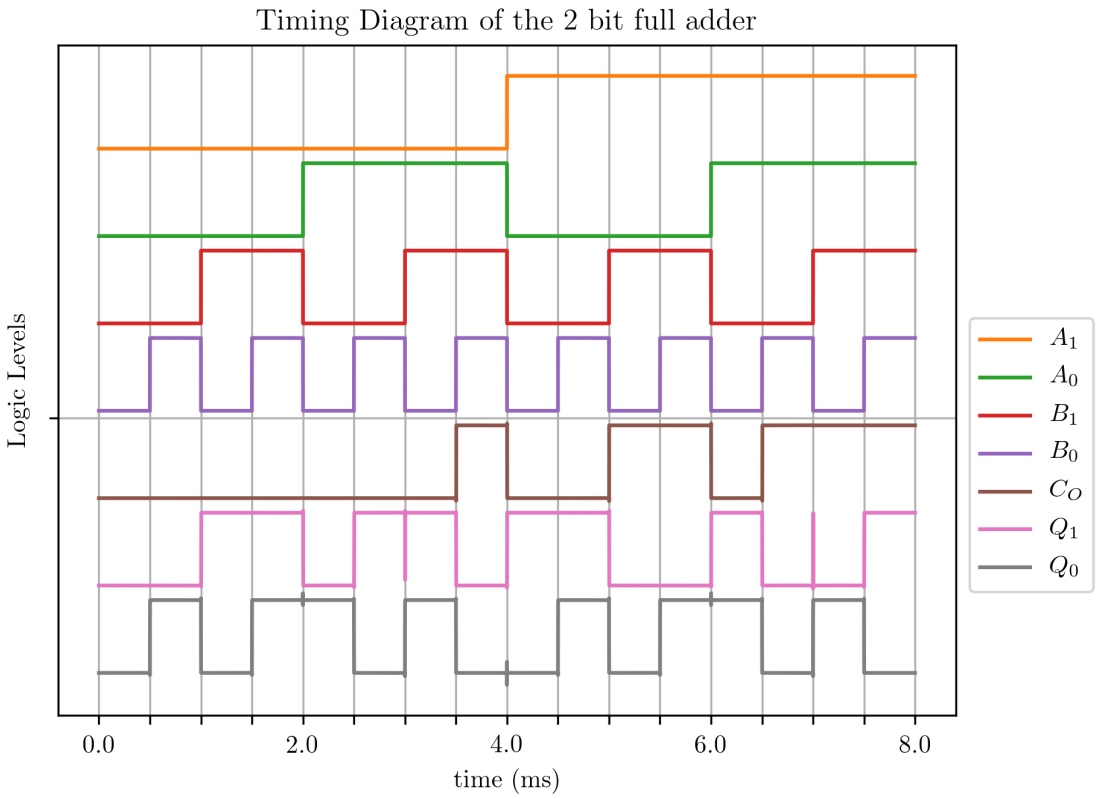

Figure 10: The timing diagram of the 2-bit full adder

In the timing diagram above a high logic level is when the signal is at 5V and a low logic level is when the signal is at 0V. We can see a few glitches in the logic gate due to the timing effects from different inputs. For example at 7ms B_1 goes high and B_0 goes low; When the transition at 7ms occurs, Q_1 briefly starts to go high. This happens as the gate responds first to B_1 going high causing Q_1 to begin to raise, but then the gate responds to B_0 going low causing Q_1 to go low again.

2.2 Truth Table

The stable input and output values from the timing diagram in figure 10 are placed into the truth table, table 1.

Table 1: The truth table for the 2-bit full adder

A_1	A_0	B_1	B_0	C_0	Q_1	Q_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

2.3 Timing Values

Finally the timing values are measured using the measure statements in the circuit shown in figure 9 and are given in table 2.

Table 2: Timing values for the 2-bit full adder.

Case	Change in Q_0 due to A_0/B_0	Change in Q_1 due to A_0/B_0	Change in Q_1 due to A_1/B_1	Change in C_0 due to A_0/B_0	Change in C_0 due to A_1/B_1
τ_{PLH}	546ns	1.837μs	2.184μs	2.184μs	1.344μs
τ_{PHL}	596ns	2.216μs	2.216μs	1.791μs	1.175μs
t_s	571ns	2.027μs	2.200μs	1.988μs	1.260μs
t_{rise}	612ns	629ns	610ns	175ns	169ns
t_{fall}	525ns	544ns	544ns	248ns	251ns

As we can see in table 10 the propagation delay is generally much longer than the rise and fall time for the 2-bit full adder. This is because the signal takes longer for it to propagate through the gate then it does for the output to fall. For example for the output C_0 to respond to a change in A_0 or B_0 the signal from A_0 or B_0 has to travel through 2 NAND gates, a NOR gate and 3 NOT Gates. This takes a significant amount of time. However when the signal reaches the final not gate, the gate takes only a few nanoseconds to rise or fall accordingly causing the rising and falling of the signals to be much faster than the propagation times.

This effect can clearly be seen in the graph in figure 11.

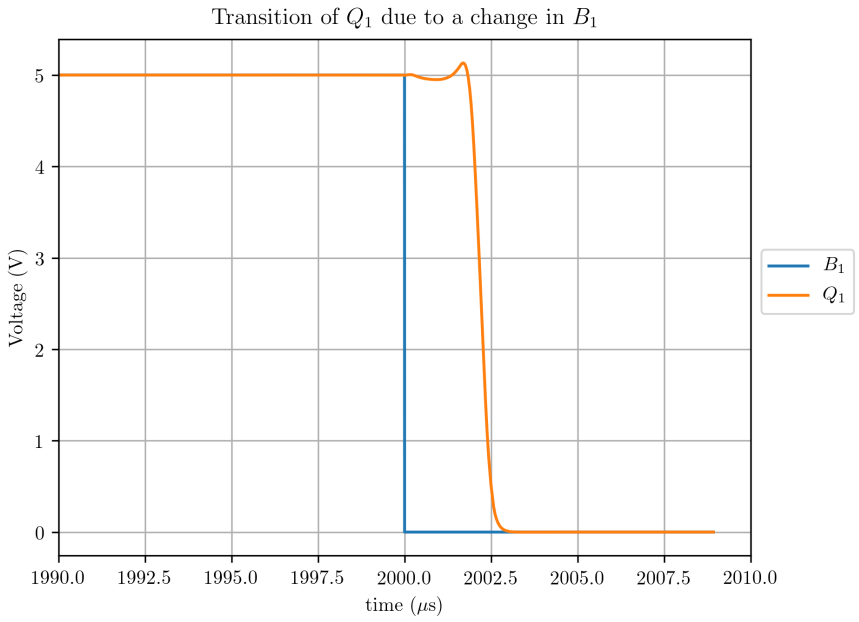

Figure 11: The delay in the output Q_1 due to a change in B_1 is clearly present in this graph.

The output Q_1 doesn't begin to fall due to the input B_1 for almost 1.5μs after B_1 falls. But when Q_1 starts to fall it falls to 0V in around than 0.5μs. The graph also verifies the data for the fall times of Q_1 from B_1 in table 2. If we were to look at the rest of the transitions we would see a similar effect where the gate changes with a quick rise or fall time after a longer propagation delay.