Introduction to Computer Architecture (Lab)

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Instructor's Contact Information:	**Course Information:**
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Course Description

Hands-on computer architecture project aiming to familiarize students with instruction set architecture, design of processor, and control and memory systems, and I/O systems. This is a computer architecture project course.

Course Objectives

By the end of this course, students will be able to:

- 1) Learn correct hardware design practices suitable for FPGA and VLSI digital design.
- 2) Learn how to write Synthesizable Verilog, and to use the tools to turn it into a circuit.
- 3) Design, Implement and Test your own processor, all the way to an FPGA bitstream.
- 4) Write assembly and machine code for your own processor.
- 5) Learn about computer architecture in the best way -- by doing.
- 6) Learn how programs and algorithms are implemented in hardware.
- 7) Work in a team, building a large, complex system using design principles that apply to both software and hardware.
- 8) Help your classmates and exercise your creativity.

Prerequisites

CSE 110, CSE 140, and CSE 140L.
CSE 141 should be taken either before or concurrently.

Required Texts

None. Note recommended readings and website tutorials listed on TED.

Expectations

Course format is a 2-hour lecture one day per week, plus independent work in the CSE basement labs (B250, B260, B270) or at home on own computers. Attendance is strongly recommended, but not required, and all lectures are podcast.

Discussions, Q&A, peer-to-peer instruction, etc. take place on our Piazza website. You are encouraged to post questions, help answer other students' questions, and provide feedback and suggestions to your instruction staff.

What is important to me is that students put forth an honest effort and treat one another, and the instructors, courteously. Constructive criticism is always welcome.

Assignments

Students shall work in teams of one to three members each.
There are four lab reports, due at the starts of the 4th, 6th, 8th, and 11th (finals) weeks. See TED for specifics. Reports shall be submitted on Gradescope.

Policies

Grading Scale

This is shown in detail on TED. Each team shall design a microprocessor -- its hardware, its firmware (machine code), and its software (assembly code). These will be tested on three program assignments, and final course grades will depend on how many programs a given processor can run successfully.

A+: all three programs run properly; high-performance processor
A-/A: all three programs run properly;
B/B+: two programs run properly;
C+/B-: one program runs properly;
C: programs do not run properly, but design compiles and shows some thought/effort
D, F: rarely given, reserved for those who do not apply themselves

Statement on Academic Integrity

This is a collaborative course, but students are expected to do their own work and to refrain from taking credit for the work of others.

Late Papers

Habitually late submissions may lower your course grade by one notch (e.g. , A to A- or A- to B+),

Accommodations for Students with Disabilities

If you have a disability for which you are or may be requesting accommodations, please contact Office for Students with Disabilities. You must have documentation from the the Office before accommodations can be granted.

Logistics

Submit lab reports on Gradescope. Instructions to follow.

Schedule

Week	Topics	Readings and Assignments
1	Intro	ISA basics
2	ISAs	ISAs
3	Assembly Language	
4	Machine Code	Lab 1 DUE
5	System Verilog Design	SystemVerilog
6	System Verilog Verification	Lab 2 DUE
7	Debuggging	SystemVerilog
8		Lab 3 DUE
9	Debugging	
10	Project Demos	
11	Project Demos	Lab 4 DUE