CSE 141L Lab 3. 9-bit CPU: Write an Assembler

Due 11:59pm .

1. Write an assembler which converts your assembly code from Lab 1 into 9-bit binary machine code.
2. Write a **top-level** Verilog model of your design, instantiating the ALU, fetch (program counter) unit, instruction memory (either inside fetch or separate, as we discussed in class), register file, data memory, control decoder, and any other blocks you need. This does not need to solve the three problems -- that will be lab 4 -- but it should compile cleanly in both ModelSim and Quartus II.
3. Submit these files on GradeScope.