CSE140 - HW #5

Due Monday June 5, 11:59PM

For the first two problems, we analyze the timing of sequential machines to practice the concept of clock period, skew and retiming. For the rest three problems, we practice the usage of standard interconnect components.

1. Given the circuit in Figure 1, each two-input AND, OR gate has a propagation delay of 60 ps and a contamination delay of 40 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q propagation delay of 70 ps, and a clock-to-Q contamination delay of 50 ps.
(a) If there is no clock skew, what is the maximum operating frequency of the circuit?
(b) How much clock skew can the circuit tolerate before it might experience a hold time violation?

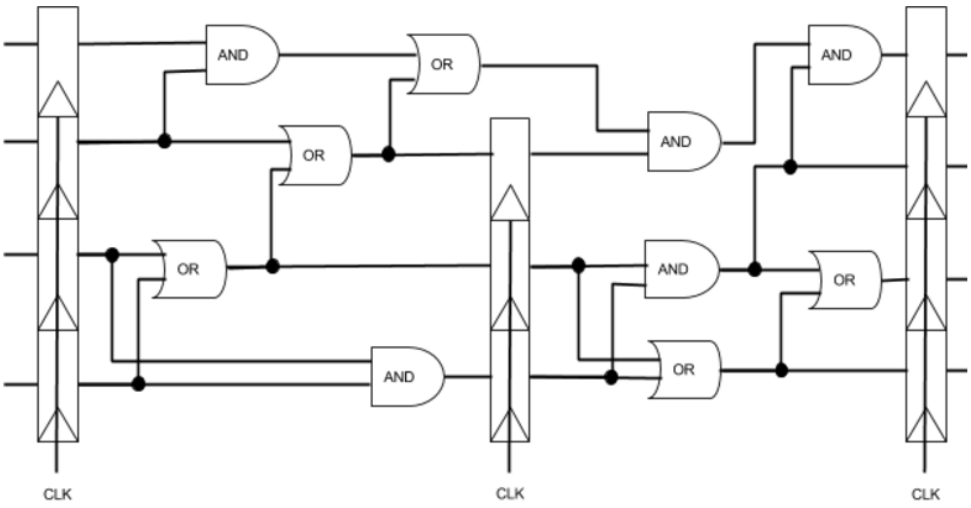

Figure 1: a sequential circuit with 11 Flip-Flops and 10 logic gates

2. A cascaded priority encoder is built with two two-input priority encoder. The encoders used prioritize the most significant inputs over the least significant inputs. In other words I_1 is more significant than I_0, so the output will correspond to I_1 if both inputs are high. The top two-input encoder has its OE signal feed into the IE input of the bottom two-input encoder and the outputs are collected to logic gates as shown in Figure 2. The machine has input and output registers and must complete the priority encoding in one

clock cycle. Each two-input encoder has the following propagation delays: 10, 15, 20 ps from I_0 to $A0$, GS, OE; 12, 17, 20 ps from I_1 to $A0$, GS, OE; and 10, 11 ps from IE to GS, OE, respectively. The two-input encoder has the contamination delay: 5, 10, 15 ps from I_0 to $A0$, GS, OE; 7, 12, 15 ps from I_1 to $A0$, GS, OE; and 5, 6 ps from IE to GS, OE, respectively.

Each logic gate (AND, OR) takes 10 ps propagation delay and 5 ps contamination delay. Each flip-flop has a setup time of 30 ps, a hold time of 10 ps, a clock-to-Q propagation delay of 35 ps, and a clock-to-Q contamination delay of 25 ps.
(a) If there is no clock skew, what is the maximum operating frequency of the circuit?
(b) If there is retiming using designated skew, what is the maximum operating frequency of the circuit?

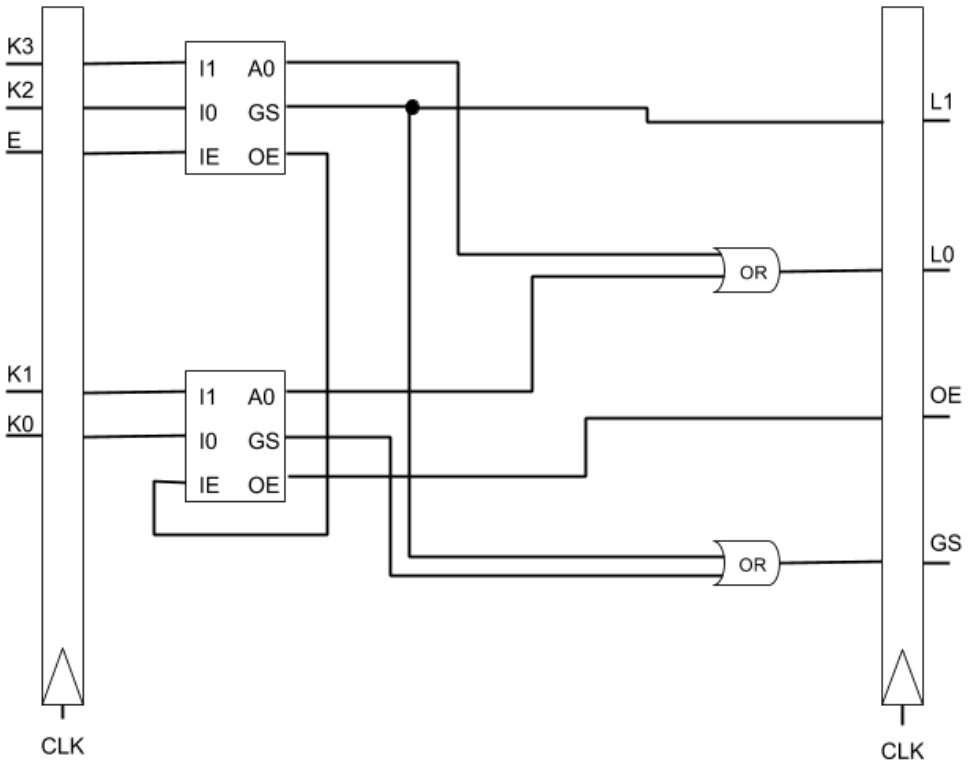

Figure 2: A cascaded priority encoder.

3. (Decoders) Given three four-input Boolean functions
$f_1(a,b,c,d) = \sum m(2,4,9,10) + \sum d(1,3,7)$,
$f_2(a,b,c,d) = \sum m(1,2,11) + \sum d(3,15)$,
$f_3(a,b,c,d) = \sum m(3,8,9,12) + \sum d(11,13)$.
3.1. Implement the functions using a minimal network of 4:16 decoders and OR gates.
3.2. Implement the functions using a minimal network of 3:8 decoders and OR gates.
3.3. Implement the functions using a minimal network of 2:4 decoders and OR gates.

4. (Multiplexers) Assume a dual-railed system, where you have access to any variable and its complement. Implement the following four-input Boolean function as indicated in each of the following subproblems.

$f(a, b, c, d) = \sum m(1, 2, 3, 6, 9, 13) + \sum d(0, 8, 11, 15)$.

4.1. Implement the function using a minimal network of 8:1 multiplexers.
4.2. Implement the function using a minimal network of 4:1 multiplexers.
4.3. Implement the function using a minimal network of 2:1 multiplexers.

5. Assume a dual-railed system, where you have access to any variable and its complement. Given a four-input Boolean function

$f(a, b, c, d) = \sum m(1, 3, 4, 7, 10, 13) + \sum d(6, 11, 15)$.

5.1. Implement the function using a minimal network of 2:4 decoders and OR gates.
5.2. Implement the function using a minimal network of 4:1 multiplexers.
5.3. Implement the function using a minimal network of 2:1 multiplexers.