Andrew Zheng

andrew.zheng1@uwaterloo.ca | in/andrewzheng2007 | github.com/awzheng | awzheng.me | Portfolio

Education

University of Waterloo | *BASc, Computer Engineering* | GPA: 3.9 — Sep 2025 – Apr 2030

Skills

Languages: C, C++, Python, Golang, Verilog, Java, SQL, HTML, CSS, JavaScript, TypeScript, Bash
DevOps/Tools: AWS (Lambda, S3, IAM), Docker, Git, Jupyter, Virtualization, VMWare Fusion, Linux
Libraries/Frameworks: FastAPI, React, MongoDB, Streamlit, NoSQL, REST API, MLOps, XGBoost, Tailwind CSS, Next.js
Embedded/Hardware: Altium Designer, KiCad, FPGA, STM32, ST-LINK, CAN, UART, I2C, SPI, Multimeter, Oscilloscope, Logic Analyzer

Experience

Software Engineering (Device Management) Intern | Miovision | Waterloo, ON — May 2026 – Aug 2026

- Selected to engineer scalable IoT infrastructure and distributed microservices for production-grade global traffic systems

Embedded Systems Developer | Waterloo Rocketry | Waterloo, ON — Sep 2025 – Present

— **Remote Arming Board** | *Safety-critical Avionics Recovery PCB* — GitHub

- Engineered 4-layer KiCad PCB with PMOS high-side switching to arm remote recovery parachute via RocketCAN bus signal
- Architected hardware fail-safe via passive gate biasing to ensure dual-altimeter redundancy during MCU Hi-Z faults
- Implemented low-level **C** firmware for **PIC18** to bridge UART altimeter telemetry onto the RocketCAN bus via MCP2562

— **Fuel Injector Sensor Hub** | *Real-Time Propulsion Telemetry Firmware* — GitHub

- Developed **STM32** drivers in **C** to acquire pressure telemetry via ADC and log to RocketCAN and SD Card mid-flight
- Validated signal integrity and CAN/I2C communication protocol effectiveness using oscilloscopes and logic analyzers

— **Recovery System Integration** | *Polaris Launch 2026 Avionics Assembly*

- Executed integration of Polaris' most safety-critical avionics to construct unified dual-redundant system architecture
- Validated and debugged hardware using NI automated test equipment and custom EGSE to certify flight readiness

Hardware Designer | UW Biomechatronics | Waterloo, ON — Sep 2025 – Jan 2026

— **EMG Bionic Arm** | *Bionic Arm PCB in KiCad and Altium Designer* — GitHub

- Spearheaded Altium migration and Git repository initialization to engineer **ESP32** control system with USB-C connectivity
- Verified PCB design constraints in Altium and SolidWorks to validate electromechanical integration for production

Case Competition Coach | Self-employed — Jun 2024 – Present

- Scaled self-founded coaching business from contract work to fully independent to achieve **5-figure revenue**
- Coached **150+** high school students from **10+** schools to produce **50+** international qualifiers and **30+** international finalists

Projects

SageWall | MLOps Cloud Security System | *AWS, Python, Streamlit, Machine Learning* — GitHub

- Architected serverless IDS on **AWS SageMaker** (**XGBoost**) to analyze network traffic with **99.9%** accuracy and <**100ms** latency
- Automated Lambda ETL pipeline to transform **125,000+** NSL-KDD records in S3, provisioning infrastructure via Boto3
- Deployed Streamlit web dashboard secured with AWS IAM, CloudWatch, and SNS for real-time system observability alerts

CrawlStars | Concurrent Search Engine | *Golang, JavaScript, MongoDB, REST API, Concurrency* — GitHub

- Engineered concurrent crawler using **Golang** producer-consumer architecture to process **2000+ pages**/min in <**15MB** memory
- Optimized deduplication via sync.Map to enable O(1) lookup for **50,000+** URLs and to filter **70%** of redundant crawls
- Developed relevance algorithm using **MongoDB Atlas** aggregation pipelines to map SEO metrics to 5-star rating system

Mangaroo | PDF-to-Manga AI Illustrator | *FastAPI, Python, JavaScript, REST API, Gemini/Imagen API* — GitHub

- Architected async FastAPI for **10x** concurrent session handling to process **50MB** PDFs (**1000+** pages) in <**50ms**/page
- Engineered Story Bible state manager to reduce token usage by **97%** and cost from $24 to **$0.70** per 10K panels
- Deployed **3-layer** error architecture with singleton pattern and Vertex AI account authentication for production-grade security

FPGA Logic Processing Unit | *FPGA, Verilog, Intel Quartus Prime* — GitHub

- Developed 4-bit ALU (ripple carry adders + multiplexers) on Altera MAX10 to route calculations to real-time 7-segment displays
- Designed logic processor for bit-wise operations and signal concatenation in Verilog to validate design in ModelSim Altera

Awards

1st Place World Champion (Marketing – Product Management) | *DECA ICDC 2024 in Los Angeles, California* — Apr 2024

7x National Honour Roll | *University of Waterloo CEMC Mathematics Contests* — 2020 – 2024