MIN-YAN HSIEH

Electrical Engineer

Contact

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No. 275, Guangming 9th Rd.,
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302048, Taiwan

Revelant Skills

- Programming
  C/C++, MATLAB, Python
- EDA TOOL
  Quartus, Modelsim, HSPICE, Finesim, Virtuoso, Spectre, Verilog, Callibre
- Equipment Expertise
  Oscilloscope, VOM meter, Function Generator, Hall Transducer, FPGA

Major

- Analog Circuit Design
- Digital Circuit Design
- Communication systems Design and signal processing
- RF Microelectronics
- All Digital Phase-Locked Loop
- Analog to Digital Converter

Education

Sep 2022 - June 2026(ESTIMATED)
National Yang Ming Chiao Tung University
- Doctor's Degree in Electrical and Computer Engineering

Sep 2019 - June 2022
National Yang Ming Chiao Tung University
- Bachelor's Degree in Electrical and Computer Engineering

Experience

Sep 2022 - August 2024
All Digital Phase-Locked Loop Program
Novatek Microelectronics Corp.
Matlab, Simulink, Virtuoso, Spectre, Tapeout
- Research about fractional Digital Phase-Locked Loop
- Low power and low noise ADPLL apply to RF systems

July 2022 - August 2022
Summer Internship Program in IC Design
RICHTEK Technology
HSPICE, Finesim, Virtuoso, Spectre, Oscilloscope, Hall Transducer
- Two-stage OP, Folded-cascoded OP, LDO analysis and simulation
- Oscillator and bandgap reference circuit analysis
- IC Measurement

June 2022
Assistant Engineer in controlling FPGA
Iredium Medical Technology
Quartus, Modelsim, Verilog
- Control the microelectrode array by FPGA

March 2022
Integrated Circuits Design Contest
Taiwan Semiconductor Research Institute(TSRI)
HSPICE, Virtuoso, Spectre, Matlab, Calibre
- Bootstraped switch design, layout and verification

Sep 2020 - June 2022
Special Projects and NYCU ECE Projects Competition
National Yang Ming Chiao Tung University
HSPICE, Virtuoso, Spectre
- LDO with ESR Compensation Design and simulation
- Low-power low-noise CMOS amplifier design

Sep 2020 - June 2022
Computer Organization
National Yang Ming Chiao Tung University
Quartus, Modelsim, Verilog
- Processor Design(Pipelined/Nonpipelined)