Computer Organization, Spring 2021

Lab 5: Pipeline CPU I

Due : 2021/06/27 23:55

1. Goal

In this lab, please modify the single cycle processor designed in lab4 to a pipelined processor. And you **don't** have to consider the hazard issue.

2. Demands

A. Please use **iverilog** as your HDL simulator.

B. Submit all *.v source files and report(pdf) on new e3.
The type of compressed file must be "zip" (Ex. Lab5_0816000.zip)
Other form of file will get -10%.

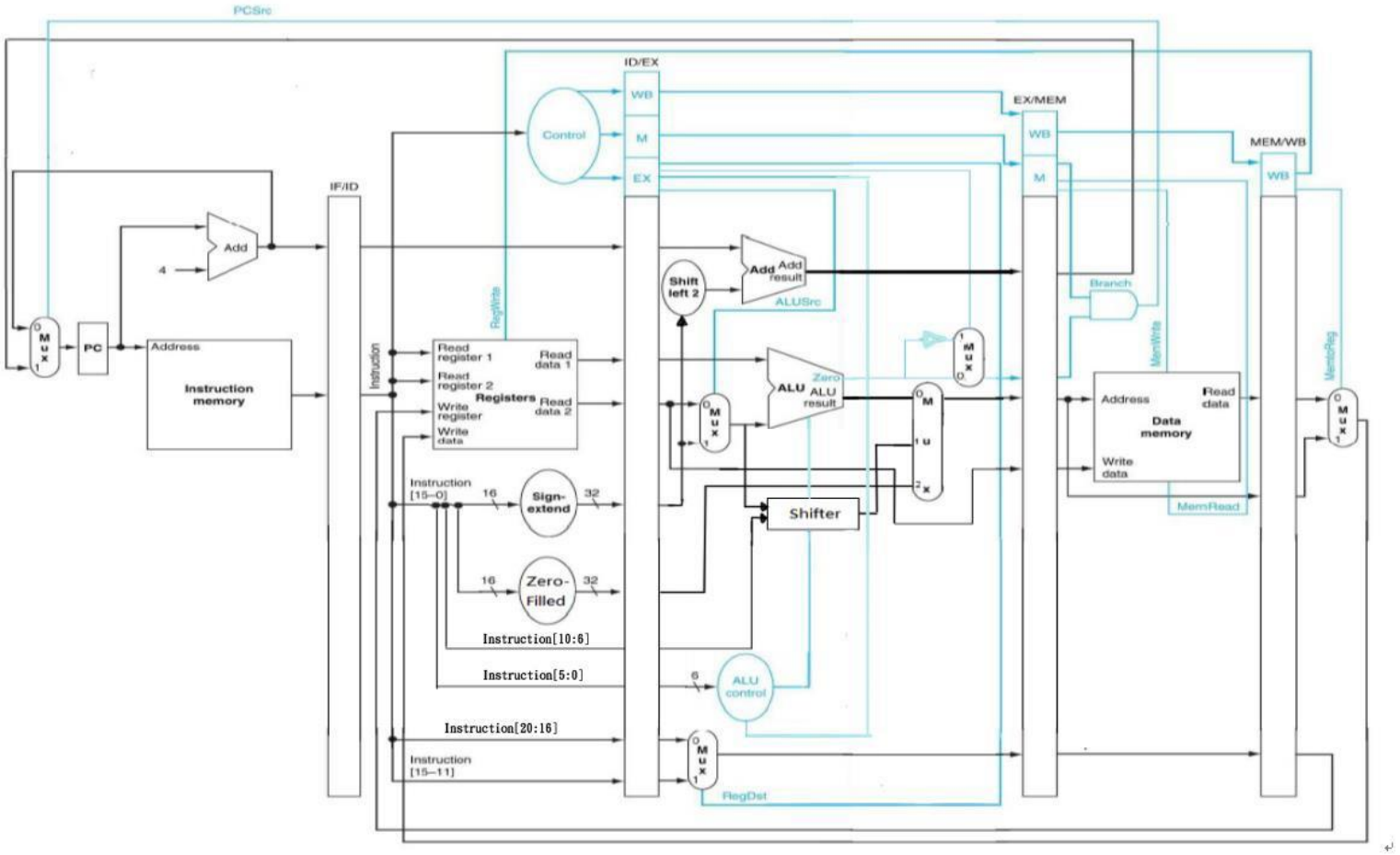
C. Reg_file(negative-edge triggered), Program_Counter, and TestBench are supplied.
Please use these modules and modules in Lab 3 to accomplish the design of your CPU.
Remember to change the "`include" region in "TestBench.v"

D. For each pipeline register, it should contain the fields for **data** and **control signals**.

E. Instruction set: we will test part of the instructions which have been implemented in previous lab :
add, sub, and, or, nor, slt, sll, srl, addi, lw, sw, beq, bne.
We will **NOT** test "jump", "jal", and "jr" instruction.
You may remove the circuits for jump, jr and jal in your design.

3. Pipelined CPU

A. Architecture diagram



According to the above diagram, in this lab you should implement a five stage pipelined processor with IF, ID, EX, MEM, and WB stages.

You should insert a pipeline register between each two stages.

Each pipeline register should contain the fields for **data** and **control signals**.

The pipeline registers are written when the positive clock edge occurs.

B. **The description of pipeline stage**

The function of each stage is described as follows:

- **IF stage:**
  In this stage, the processor fetches an instruction from the instruction memory and performs PC + 4.

- **ID stage:**
  In this stage, the processor decodes the instruction to generate the control signals, reads two source registers, and generates the sign extended immediate value.

- **EX stage:**
  In this stage, ALU_Ctrl generates control signals for function units according to ALUOp. At the same time, Register Write ID and branch target are also determined in this stage.

- **MEM stage:**
  In this stage, the processor accesses data memory according to the control signals. The modification of PC from branch taken instruction is also performed in this stage.

- **WB stage:**
  In this stage, the processor will write the value into register file according to the control signal when negative clock edge occurs.

C. **Description of pipeline register**

Please design four pipeline registers. Each pipeline register must be "positive-edge triggered", has default value 0.

Then, insert these pipeline registers into your single-cycle CPU designed in Lab4 to accomplish the pipelined CPU required in this lab.

DO NOT set any delay time for the sequential circuits of the pipelined registers designed by you.

4. Test

Modify line 43 of TestBench.v to read different test data.

There are 2 test files, CO_P5_test_data1.txt and CO_P5_test_data2.txt.

Corresponding instructions and output answer are in data1_result.txt and data2_result.txt

5. Grade

A. Total score: 100pts. **COPY WILL GET A 0 POINT!**

B. Instruction score: 80 pts.

C. Report: 20 pts - format is in StudentID_report.pdf.

D. Late Submission:

10 points off per day, if you are late over 3 days you will get 0 points.

6. Hand in your assignment

Please upload the assignment to the E3.

Put all *.v source files and report(pdf) into same compressed file.

(Use Lab5_student ID.zip to be the name of your compressed file, please make sure your files are correct)

7. Q&A

If you have any question, just send email to all TAs via new E3 platform.