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WM-N-BM-09 Application Note

SOURCE ORGANIZATION:	USI WP / RD / HW1

Prepared by	Scarrie	Date: 2012/07/09
Checked by	Mike	Date: 2012/07/09
Approved by		Date:
Concurrence		Date:

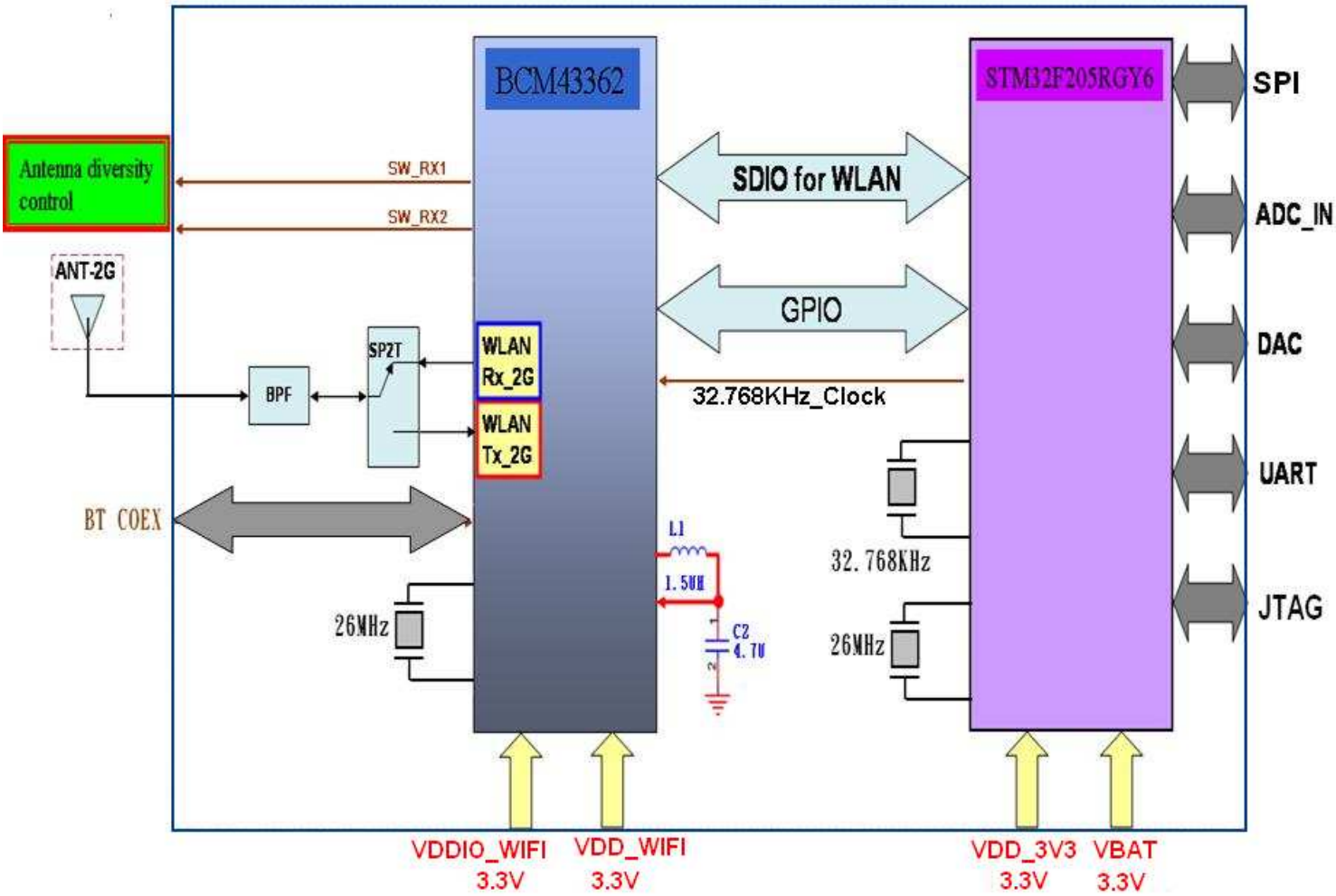
Update History

History	Revision	Description	Originated or Modified by
2012/06/22	1.0	Initial release	Scarrie
2012/07/09	1.01	Add JTAG interface	Scarrie

HW Application note for WM-BN-BM-01

1. Introduction

WM-N-BM-09 is a WICED module that is includes WIFi and Micro-processor. The WLAN is 2.4G single band that includes 802.11b/g/n function. In this application will show Module power plan, reference schematic description and the layout guide line for this module.

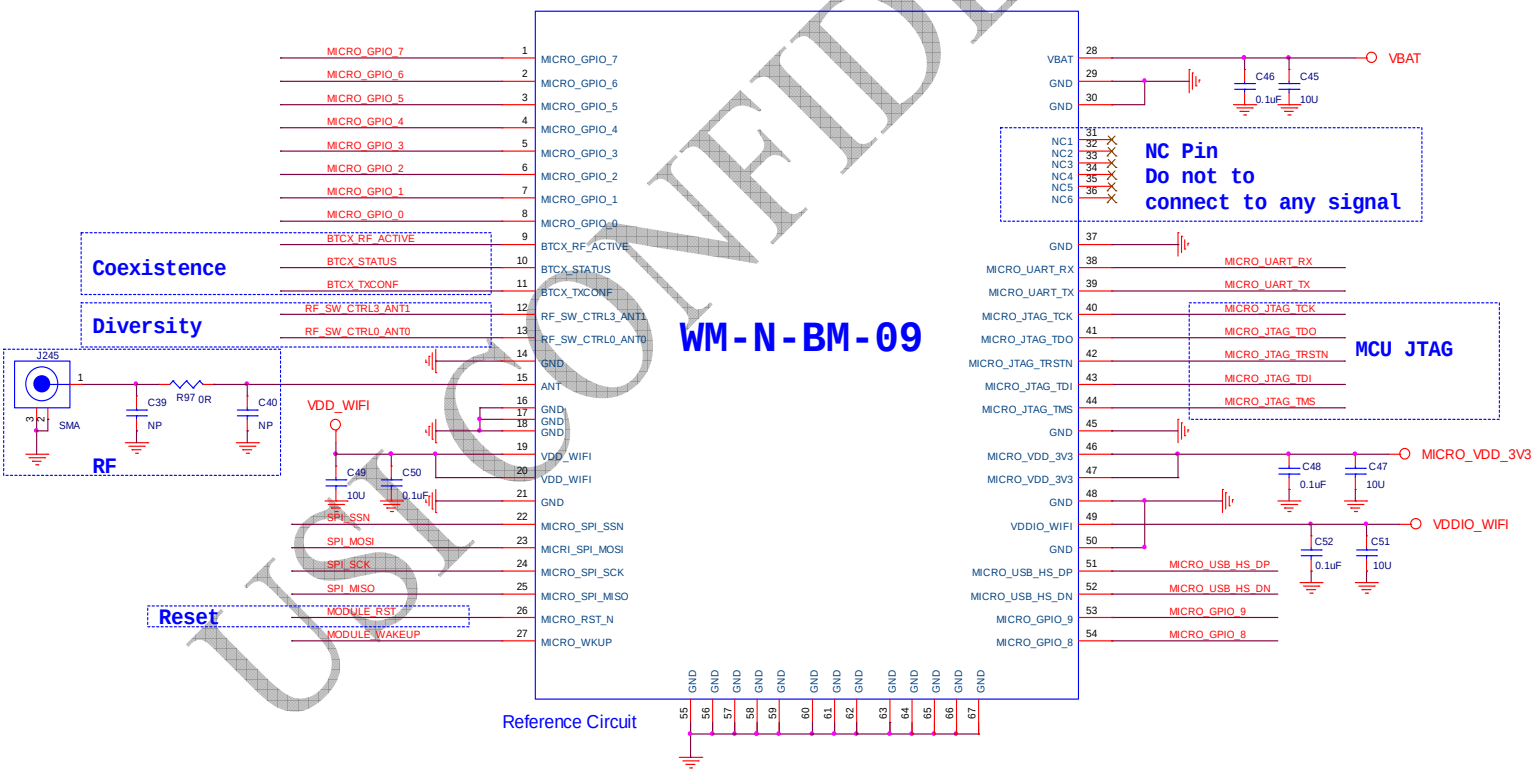


2. Power Request

Module operational requirements voltage have VDD_WIFI, VDDIO_WIFI, VDD_3V3, VBAT all of these powers need supply 3.3V voltage.

Symbol	Parameter	Min	Typ	Max	Unit
VDD_WIFI	Power Supply for BCM43362	3.0	3.3	3.6	V
VDDIO_WIFI	Host Interface Power Supply	3.0	3.3	3.6	V
VBAT	Backup operating voltage	3.0	3.3	3.6	V
VDD_3V3	power Supply for MCU	3.0	3.3	3.6	V

3. Reference Circuit



4. Layout suggestion:

DC power

Use wide traces for power supply lines. Know the maximum currents being carried on each power supply trace, and make the trace widths proportionate to the current (especially for long trace lengths). Where possible, fill large areas with copper to distribute the highest currents. These measures minimize IR drops, line inductance, and switching transients.

- Use several plated via holes to connect power supply traces between layers. The number of vias used should be proportional to the current being routed.
- Avoid loops in the supply distribution traces. Current-carrying loops are essentially antennas radiating electromagnetic fields that may corrupt transceiver performance or cause regulatory electromagnetic interference (EMI) test failures

- Capacitor for power line, please close to module pin out
- For power line capacitor, if you have 2 capacitor, one is for low frequency noise bypass, another is for high frequency noise by pass, please let high frequency noise bypass capacitor be the most close to module pin.

WM-N-BM-09 maximum current as the Table1. below:

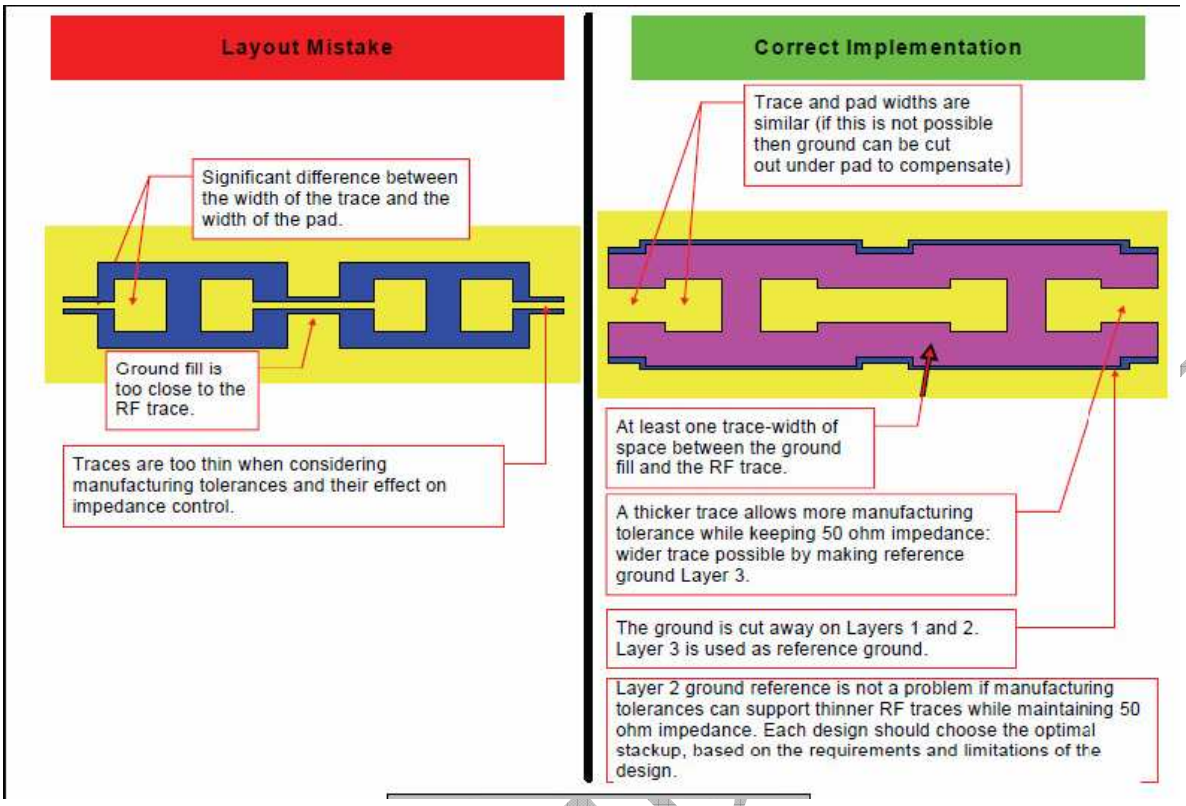
Power consumption	Max
VDD_WIFI	500 mA
VDDIO_WIFI	150 mA
VDD_3V3	120 mA
VBAT	50 mA

Table1.

RF Signal

General guidelines for routing RF signals of WLAN Antenna port

RF signals require controlled-impedance lines to minimize mismatch losses and efficiently transfer energy from source to load. The line impedance depends upon several variables — trace width and thickness, co-planar ground spacing, height of dielectric material between the trace and ground plane(s), and dielectric constant of the PCB material. Given the PCB material selected, the geometry of the micro-strip, strip-line, or co-planar grounded waveguide (CGW) elements must be designed properly to provide the desired 50-Ω impedance. Design of micro-strip, strip-line, and CGW elements is well documented and supported in many microwave software applications



Additional RF-specific PCB design guidelines include:

• Keep the RF traces on the component sides (top or bottom layer) using micro-strip or CGW techniques where possible.
• Screen these traces to avoid electromagnetic interference.
• Use internal layers with strip-line techniques if necessary.
• Maintain continuous ground below micro-strip traces, beside CGW traces, and above and below strip-line traces.
• Keep traces short and direct, to minimize loss and undesired coupling.
• Front-end losses increase the system noise figure — keep traces before the first gain stage as short as possible and use low-loss capacitors and inductors.
• Clear internal layer (or layers) of metal. This improves micro-strip, CGW, and strip-line geometries, allowing wider traces.
• Fill the areas along both sides of traces with ground to improve isolation, but provide adequate clearance to minimize co-planar capacitance and leakage. These ground-filled areas are integral to CGW designs.
• Use several ground vias along both sides of the signal traces to connect RF ground-fill areas to the internal RF ground plane.
• Avoid crossing RF traces if possible.
Ground of RF trace it is better to use it's own ground on top layer.

5. Host Interface

PIN 22/23/24/25 pins for SPI interface. Table2. describes the SPI pins.

Table2. SPI Interface

Pin Number	Symbol	Pin Type	Description
22	MICRO_SPI_SSN	I	SPI_SS
23	MICRI_SPI_MOSI	I	SPI_MOSI
24	MICRO_SPI_SCK	I	SPI_SCK
25	MICRO_SPI_MISO	O	SPI_MISO

PIN 38/39 pins for UART interface. Table3. describes the UART pins.

Table3. UART Interface

Pin Number	Symbol	Pin_Type	Description
38	MICRO_UART_RX	I/O	UART_RX
39	MICRO_UART_TX	I/O	UART_TX

PIN 51/52 pins for USB interface of optional. Table4. describes these USB pins.

Table4. USB Interface

Pin Number	Symbol	Pin_Type	Description
51	MICRO_USB_HS_DM	I/O	USB_HS_DM
52	MICRO_USB_HS_DP	I/O	USB_HS_DP

6. JTAG Interface

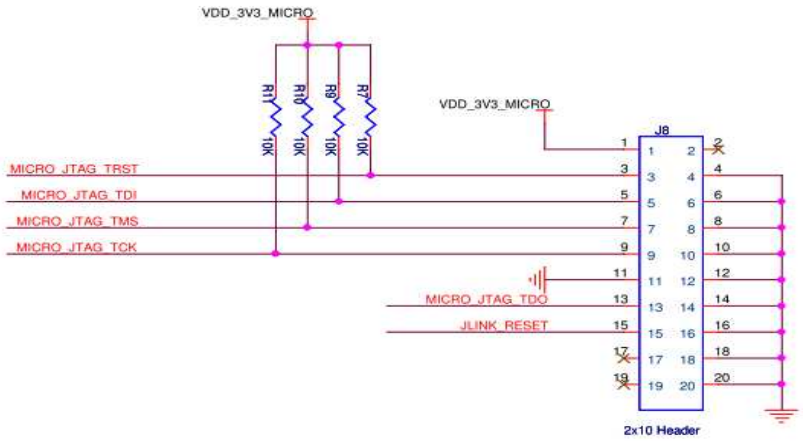
PIN 40/41/42/43/44 pins for JTAG interface that can be used for programming MCU.

Table5. describes these JTAG pins.

Table5. JTAG Interface

Pin Number	Symbol	Pin_Type	Description
40	MICRO_JTAG_TCK	I/O	JTAG_TCK
41	MICRO_JTAG_TDO	I/O	JTAG_TDO
42	MICRO_JTAG_TRSTN	I/O	JTAG_TRSTN
43	MICRO_JTAG_TDI	I/O	JTAG_TDI
44	MICRO_JTAG_TMS	I/O	JTAG_TMS

We suggest customer could follow our EVB design , All JTAG signals connect to 2x10 header, And then they can use OLIMEX ARM-USB-TINI-H cable to program MCU.



Jlink Header

Please find detail information from link as below,

https://www.olimex.com/dev/arm-usb-tiny-h.html

7. Characteristic Option

7.1 External Coexistence Interface

WM-N-BM-09 support for coexistence with Bluetooth or other external radios.

To manage wireless medium sharing for optimal performance, an external coexistence interface is provided one or two external collocated wireless devices such as Bluetooth or WiMax. Table5. describes these coexistence pins.

Table5. coexistence status

Pin Number	Symbol	Pin Type	Description
9	BTCX_RF_ACTIVE	I	Coexistence signal indicating that Bluetooth is active. This pin is multiplex and can be changed to a GPIO via software.
10	BTCX_STATUS	I	Coexistence signal indicating Bluetooth priority status and TX/RX direction. This pin is multiplex and can be changed to a GPIO via software.
11	BTCX_TXCONF	O	Coexistence output giving Bluetooth permission to transmit. This pin is multiplex and can be changed to a GPIO via software.

Multiplexed BT_Coex pins. When programmed are high impedance on power up and reset. Subsequently, they can be individually programmed to become inputs or outputs through software control. They can also be programmed to have internal pull-up or pull-down resistor.

7.2 Antenna Diversity Controller

WM-N-BM-09 supports per packet RX antenna diversity.

The RF control lines for antenna diversity as show Table6. below:

Table6. diversity controller status:

Pin Number	Symbol	Pin Type	Description
12	RF_SW_CTRL3_ANT1	O	RF switch control line. Default at this pin is low.
13	RF_SW_CTRL0_ANT0	O	RF switch control line. Default at this pin is high..

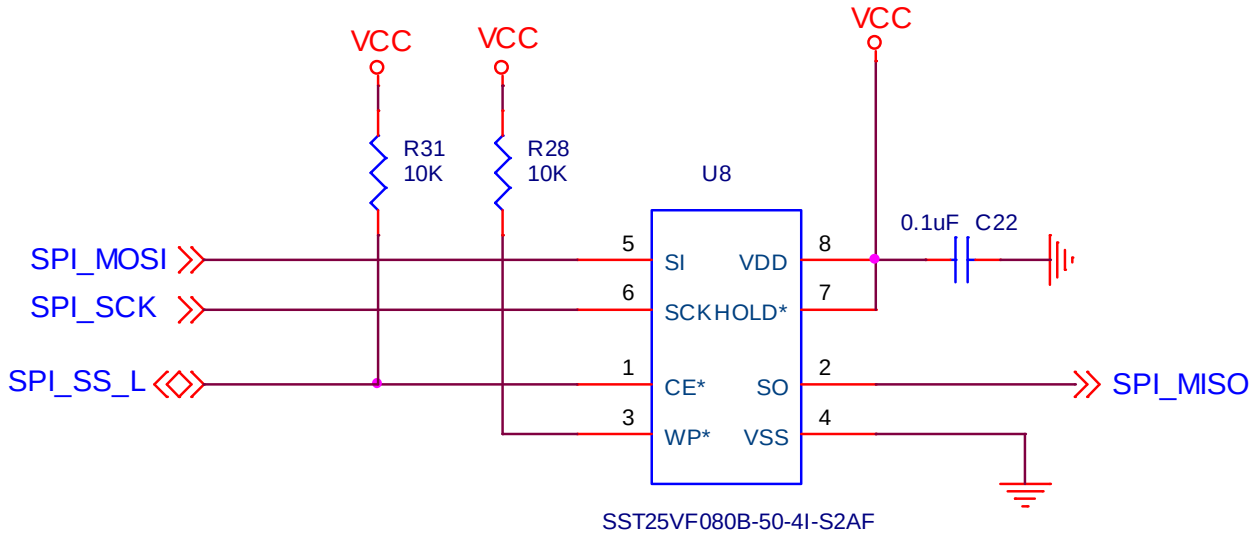
7.3 External Flash memory

WICED devices embed a 128-bit wide Flash memory of 1 Mbytes available for storing programs and data. It also features 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

If user need more memory, they can use pin22/23/24/25 to expand the flash memory. The Table7. describes these pins.

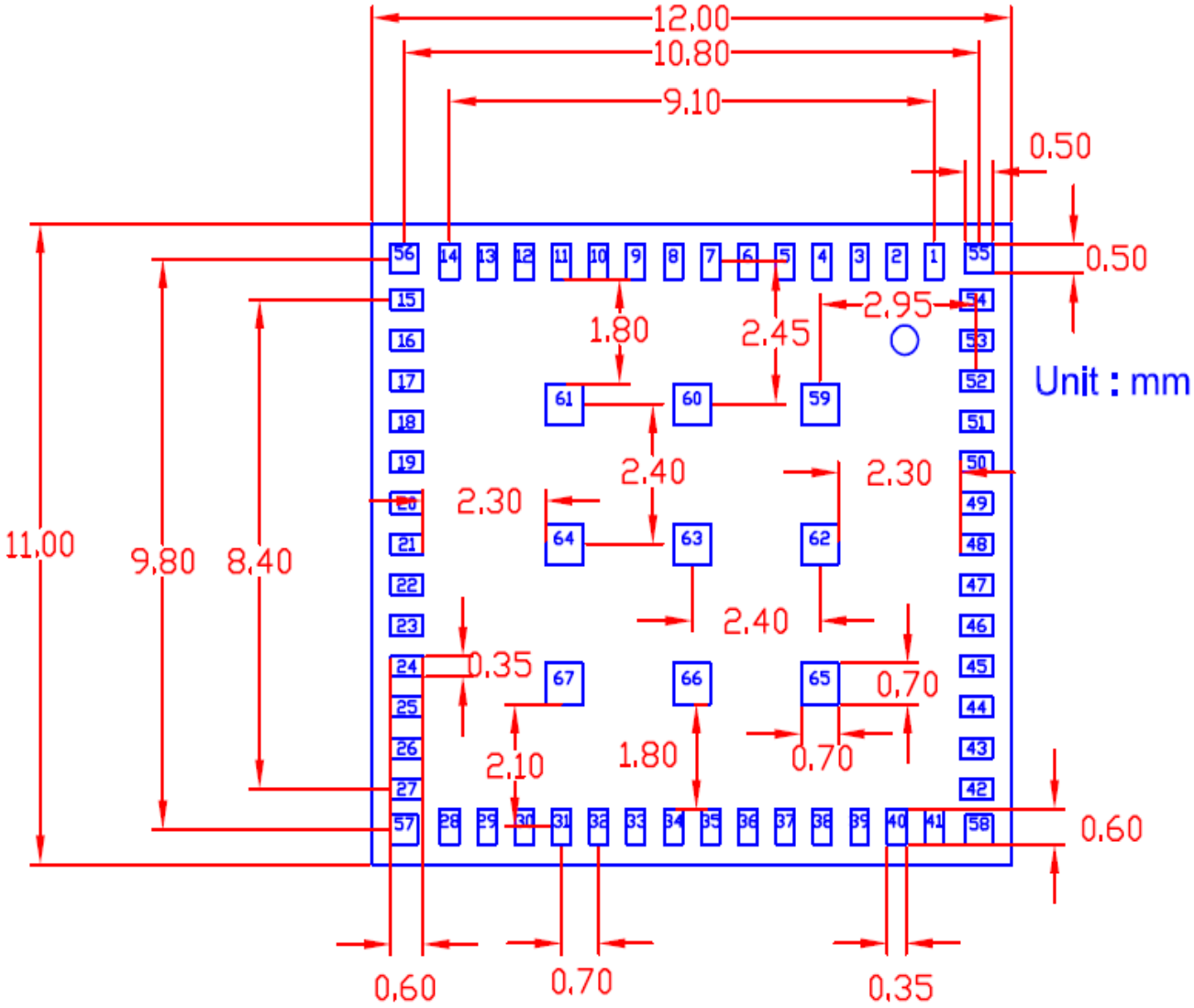
Table7. flash memory lines:

Pin Number	Symbol	Flash Define	Type
22	SPI_SSN	CE#	I/O
23	SPI_MOSI	SI	I
24	SPI_SCK	SCLK	I
25	SPI_MISO	SO	O

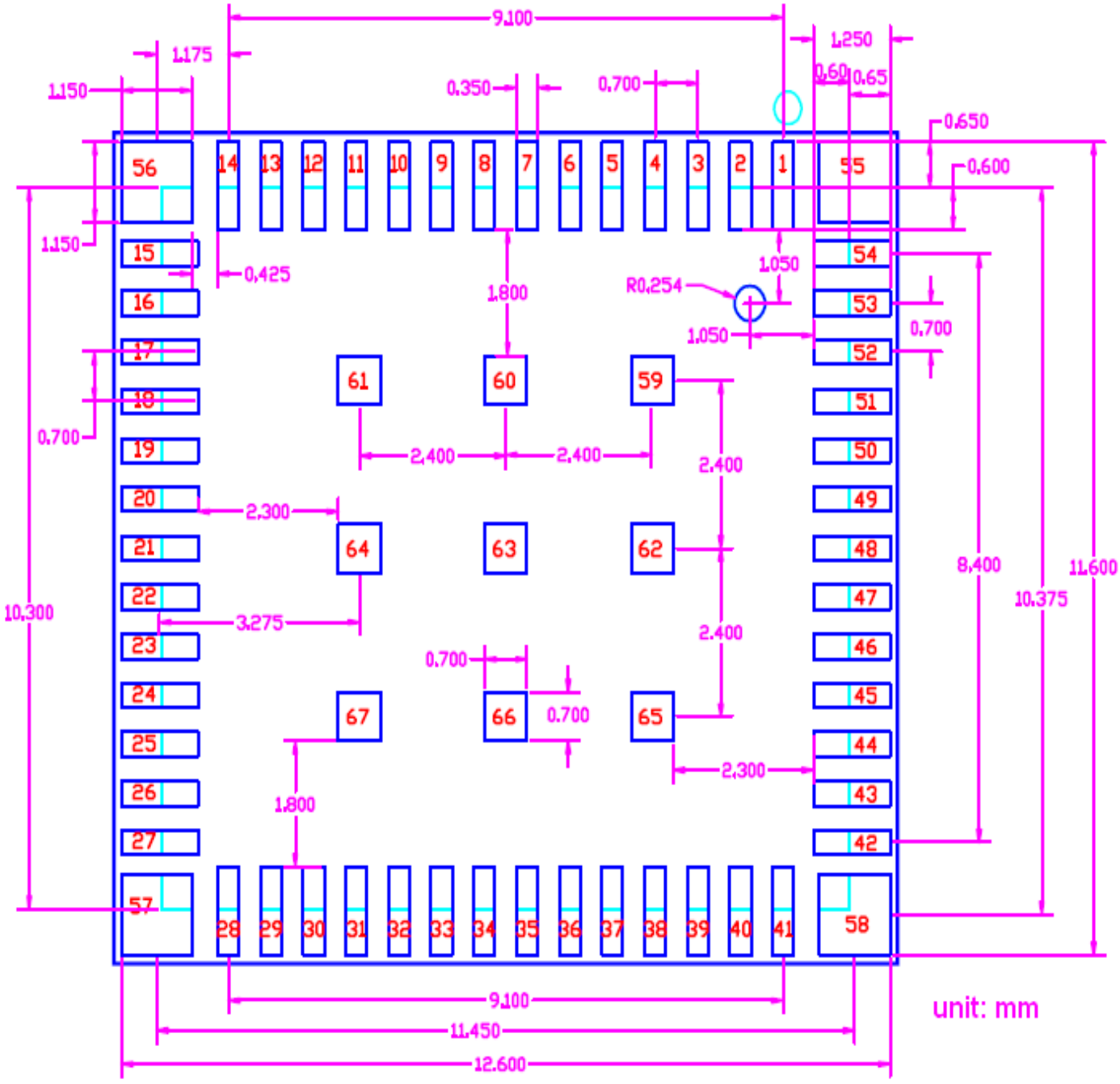


8. Module Dimension

12 mm (W) X11 mm (L) X1.3 mm (H) (Including Metal Shielding)



9. Recommend Footprint



10. Reflow Profile Guideline

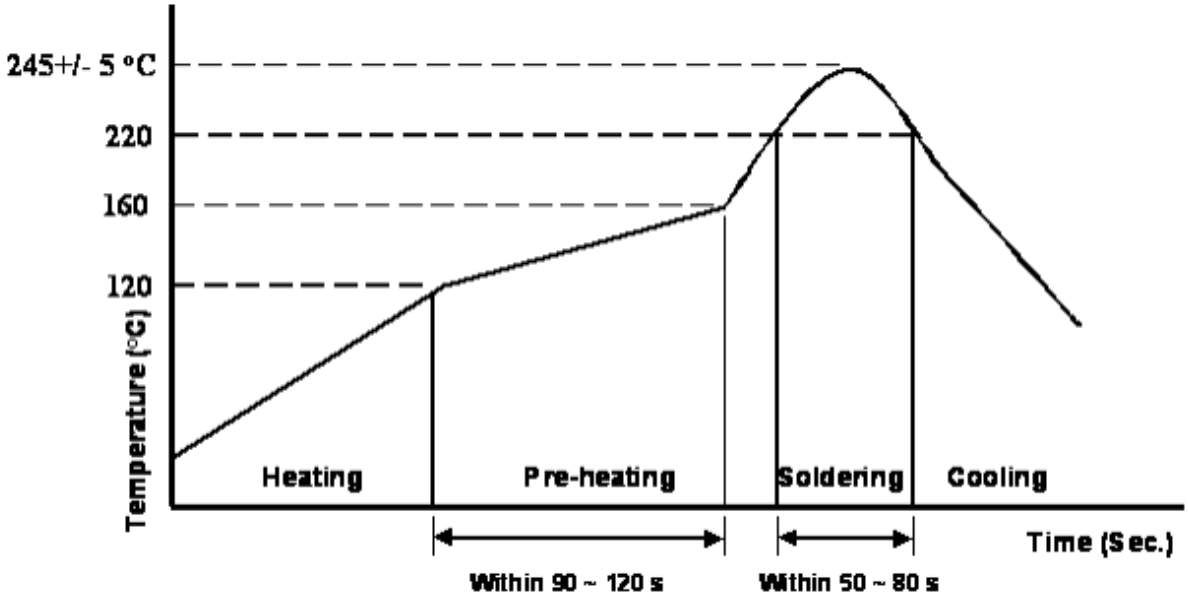
The reflow profile is dependent on many factors including flux selection, solder composition and the capability of user's reflow equipment.

USI does not request a specific reflow profile but provides the following general guidelines:

- The solder composition typically sets the peak temperatures of the profile. Recommend lead free solder pastes SAC305: Type 4, water soluble or no clean are acceptable.
- Reflow equipment needed at least nine heater zones. Recommend forced air type reflow oven with Nitrogen.
- It is recommended that the peak temperature at the solder joint be within 240℃ ~ 250℃ and the maximum component temperature should not exceed 250℃.
- It is recommended that time above 220℃ for the sol der joints is between 50-80s, and with a minimum of 50s.
- Excessive ramp/cooling rates (>3℃/s) should be avo ided.
- To develop the reflow profile, it is recommended that the user place thermocouples at various locations on the assembly to confirm that all locations meet the profile requirements. The critical locations are the solder joints of SiP Module.

When developing the reflow profile, it is recommended that the actual fully loaded assembly be used to make sure that the total thermal mass is accounted for.

11. Recommended Reflow Profile



(1) Solder paste alloy : SAC305 (Sn96.5/Ag3.0/Cu0.5) (Lead Free solder paste.)
(2) Peak temperature 245+/- 5 °C.
(3) Above melting point 220 °C, 50 ~80 Seconds.
(4) Pre-heat 120 to 160 °C, 90 ~120 Seconds.
(5) Nine heater zones at least for Reflow equipment.
(6) Nitrogen usage is recommended and be controlled the value less than 1500 ppm.
Note: Need to inspect solder joint by X-ray post reflow.