# FHE reading guide

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Vinod Vaikuntanathan and Daniele Micciancio both keep a webpage with important (theoretical) FHE papers https://people.csail.mit.edu/vinodv/FHE/FHE-refs.html & http://cseweb.ucsd.edu/~daniele/LatticeLinks/FHE.html. The following ones are ones I am reading, I tried to substitute theoretical papers with ones that look at the schemes from an implementational point of view wherever possible.

# 1 Papers

### 1.1 Pre-FHE & Gen-I FHE

This is mostly historical. The assumptions and techniques used are different than those used today, and these schemes are very inefficient.

### 1.2 Gen-II FHE

These are still widely-used and implemented. They are based on (R)LWE assumptions.

- BGV [BGV12] (based on ideas from [BV11])
- (B)FV [FV12] (a port from LWE to RLWE of [Bra12])

These schemes allow *packing* (also *batching*, SIMD) of multiple plaintexts in ciphertext *slots* for higher throughput. There is an approach based on the CRT for RLWE schemes [SV14] and a different approach for LWE schemes [BGH12].

BGV was used to homomorphically evaluate the AES circuit [GHS12]. The paper describes some optimisations of BGV that are implemented in most libraries.

There are two separate approaches to implement (B)FV in full-RNS representation. This paper [BPA+18] talks about implementing both of them in PAL-ISADE.

The LTV [LATV12] and YASHE [BLLN13] second generation schemes based on NTRU were quite popular as well, but have since been broken. This paper [LN14] compares (B)FV with YASHE from an implementational point of view.

### 1.3 Gen-III FHE

The third-generation starts with GSW, which uses a different approach than the second-generation schemes. GSW is quite inefficient, but remarkably simple and allows advanced constructions. GSW is often used in tutorials on FHE due to its simplicity. GSW ciphertexts are used by FHEW and TFHE during bootstrapping.

FHEW introduced the "gate bootstrapping" idea which allows for fast bootstrapping by bootstrapping after every single gate. In a way, TFHE can be seen as porting FHEW, which uses both normal LWE and ring-GSW, to the Torus. One of the merits of FHEW is that is quite easy to understand and implement, whereas TFHE appears to be much more complicated.

- GSW [GSW13]
- FHEW [DM15]
- TFHE ([CGGI18], journal version combining multiple works)

A recent paper compares FHEW with TFHE (if TFHE would use the ternary instead of binary secrets) and implements this in PALISADE [MP20]. The PALISADE team seems really opposed to the binary secret distribution used in TFHE.

### 1.4 Gen-IV FHE

The HEAAN/CKKS approach [CKKS17], which encrypts approximate numbers, is either seen as a new generation or a variant of Gen-II.

There have been several RNS and bootstrapping optimisations [CHK<sup>+</sup>18, CHK<sup>+</sup>19, CCS19].

# 2 Tutorials

There are a number of more tutorial-like resources for FHE.

The most extensive one is probably this one from Halevi [Hal17], it describes GSW in detail. There is also this overview by Brakerski [Bra], also describes GSW in detail. There is this general introduction to lattice-based crypto from Peikert [Pei16], also describes GSW near the end.

### 2.1 Videos

There are a lot of video lectures and seminars on FHE out there. Some of the best ones I found.

- The videos from the Simons lattice semester in 2020. They are quite down-to-earth.
  - A talk about BV11 (the precursor of BGV) (https://simons.ber keley.edu/talks/advanced-lattice-based-cryptography-fheabe-etc)
  - Tutorial on GSW (https://simons.berkeley.edu/talks/tutorial-encrypted-computation-lattices)
  - Ilaria on FHE and TFHE (https://simons.berkeley.edu/talks/intro-fhe-and-tfhe)
  - CKKS/HEAAN (https://simons.berkeley.edu/talks/heaan-fhe)
  - PALISADE (https://simons.berkeley.edu/talks/palisade-l
    attice-library)
  - ... much more on lattice-based crypto
- See (http://cseweb.ucsd.edu/~daniele/LatticeLinks/FHE.html, at the bottom) for a collection of more videos.

# 3 Standard

The FHE standard describes BGV, (B)FV and GSW https://homomorphicencryption.org/standard/.

### 4 Libraries

A full list of all the FHE libraries is maintained here [Sch19]. Looking at the manual of the libraries can sometimes quickly give you an understanding of the implementational aspects of a scheme. These are the most popular ones.

- Microsoft SEAL implements BFV and CKKS. There is only a real manual for an older version 2.3.1 of the library [Lai]
- HElib implements BGV and CKKS. Comes with two reports that describe the algorithms and bootstrapping used in the library [HS14a, HS14b]
- PALISADE implements BFV, BGV, CKKS, TFHE, FHEW. There is a manual at [noaa]
- FHEW. This is more like a proof-of-concept. It is a very small library, due to the simplicity of FHEW. [Duc20]
- TFHE [noab]

### 5 Hardware

The following is copied from my FWO proposal.

Naturally, the first FHE hardware architectures implement first-generation FHE schemes. Cao et al. [CMO<sup>+</sup>14] implement a variant of the van Dijk scheme using integer-NTT on FPGA, but assume unlimited bandwidth to off-chip memory. Wang et al. develop a 768K-bit multiplier<sup>1</sup> for a variant of Gentry's scheme and implement the result on both FPGA and ASIC [WH13, WHEW14]. Doröz et al. similarly proposed a million-bit integer multiplier [D13], and integrate it into an ASIC implementation of the same scheme [D15]. There are several implementations of the second-generation NTRU-based YASHE and LTV schemes [SRJV<sup>+</sup>15, PNPM15, DS15, CRS17], but the underlying FHE schemes have since been broken.

(R)LWE-based implementations remain secure to date. Migliore et al. [MSR<sup>+</sup>17] implemented a Karatsuba variant of the second-generation FV scheme. While computationally slower than NTT, this approach benefits from easier integration of second-generation packing techniques. The design is presented as a software library using AVX2 instructions, coupled with a fully pipelined hardware accelerator over PCIe. In a series of two works, Roy et al. [SRJV<sup>+</sup>18, SRTJ<sup>+</sup>19] accelerate the NTT variant of FV. The first work targets a large parameter

 $<sup>^1{\</sup>rm The}$  multiplier can take inputs up to  $2^{768}.$  In comparison, modern CPUs can efficiently handle inputs up to  $2^{64}.$ 

set, incurring massive off-chip data transfers. In the second work, the authors target less complex cloud applications, such that sufficient on-chip memory is available and data transfers are minimized. This last design is implemented on an ARM+FPGA MPSoC. Finally, HEAX [RLPD19] is an NTT implementation of HEAAN on FPGA. The employed platform connects a host CPU and FPGA over PCIe, as well as requiring off-chip DRAM memory. To the best of our knowledge, no hardware implementations of third-generation schemes have appeared in the open literature.

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