**Report**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| *Implementation* | *Area (um^2)* | *Critical Path (ns)* | *Maximum Operating Frequency (MHz)* | *Number of Cycles for program* | *Minimal time to execute the program (sec)* |
| *Single Cycle*  *(program: mult1)* | *253613.408462* | *30.01* | *33.32* | *1183* | *0.0000355* |
| *Single Cycle with Multiplication Support*  *(program: mult2)* | *259646.401129* | *39.93* | *25.04* | *37* | *0.000001477* |
| *Pipelined*  *(program: mult2)* | *263133.783221* | *23.25* | *43.01* | *41* | *0.000000953* |
| *Pipelined with data hazard resolution*  *(program: mult3)* |  |  |  |  |  |
| *Pipelined with performance optimization (program: optional)* |  |  |  |  |  |

*Questions:*

* *For the single cycle processor, which kind of instruction would stimulate the critical path found?*

*The instructions with memory access, like a store and a load.*

* *For the single cycle processor, which resources constitute most part of the gates? What is your explanation for this distribution?*

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* *What are the disadvantages of using a single cycle processor compared with more advanced implementations?*

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* *Is the critical path affected when hardware support for multiplication is added to the single cycle processor? What is your explanation for this?*

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* *Is adding hardware support for multiplication a good choice for every microprocessor?*

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* *How much larger is the pipelined implementation compared to the single cycle processor? What is the main cause for its increase?*

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* *How the critical path is affected when we pass from a single cycle processor to a pipelined implementation?*

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* *Taking into account the critical path found for the pipelined processor, how would be possible to increase the performance of the system?*

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* *Is the addition of hardware improvements, like pipelining, correlated with higher power consumption? How can we assess if a specific modification to our processor improve or diminish the energy efficiency of the system?*

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* *What other microarchitecture techniques (besides pipelining) could be implemented in our microprocessor in order to improve performance, under what circumstances?*

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