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Research Article

Improved Design of Bit Synchronization Clock Extraction in Digital Communication System

Huimin Duan, Hui Huang, and Cuihua Li

Department of Electronic and Electrical Engineering, Hefei University, Hefei, China

Correspondence should be addressed to Huimin Duan; duanhuimin@foxmail.com

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An improved method is proposed in this design to reduce the phase jitter after the synchronization or the random noise induced phase jitter in a bit synchronization clock extraction circuit. By using a newly added digital filter between the phase detector and the controller, the phase difference pulses from the phase detector are counted and processed, before being transmitted to the controller for adjusting the phase of the output clock. The design is completed by using FPGA chip and VHDL hardware description language and performs the simulation verification on Quartus II. The results show that the improved system performs the accurate extraction of bit synchronized clock, reduces the phase jitter problem, improves the system running efficiency and the ability of anti-interference, and guarantees the synchronization performance of the digital communication system.

1. Introduction

In digital communication systems, information is transmitted in a series of code sequences; the receiver must know the starting and ending time of each code [1, 2], so it needs to have a bit timing pulse sequence for the sampling decision, which has the same repetition frequency as the code rate of transmit end and the same phase as the optimal decision time. The process of extracting the timing pulse sequence is called bit synchronization [3], which is implemented by an external or a self-synchronization method. The self-synchronization method extracts the synchronization information from the code in the receiving end without inserting the pilot signal at the transmitter end, making it the most commonly used method in modern digital communication [4, 5].

In the self-synchronizing digital communication system, the methods to extract the bit synchronized signal mainly includes filtering method, enveloping "collapse" method, and DPLL (Digital Phase-Locked Loop) method. The DPLL method is mature and widely used [6–8]. At present, the system that uses phase-locked loop to extract bit synchronous clock has complex extraction process, slow running speed, or lack of ability to resist random noise. This work is to present an improved DPLL based design for bit synchronized clock extraction in digital communication system. The main idea is to implement a digital filter between the PD (Phase Detector) and the control module, which is used to process the leading or lagging control pulses corresponding to the phase difference of the PD output before sending them to the control module for a phase adjustment to its clock. This implementation can be used to avoid the alternation of leading and lagging pulses after the synchronous locking and to improve the phase jitter problem caused by the random noise effect [9–13]. In this paper we omit rigorous mathematical proof of local and global stability of proposed circuit. Local and global analysis can be done with reference to classic PLL-based circuit [14, 15].

2. The Principle of Bit Synchronization Clock Extraction Based on DPLL

The idea of DPLL method to extract bit synchronized clock is shown in Figure 1, which includes four main steps of crystal oscillator signal shaping, frequency division, phase detection, and control. The output of crystal oscillator is transmitted into two clock signals with a duty ratio of about 1/4 and a phase difference of π, which are used together with the

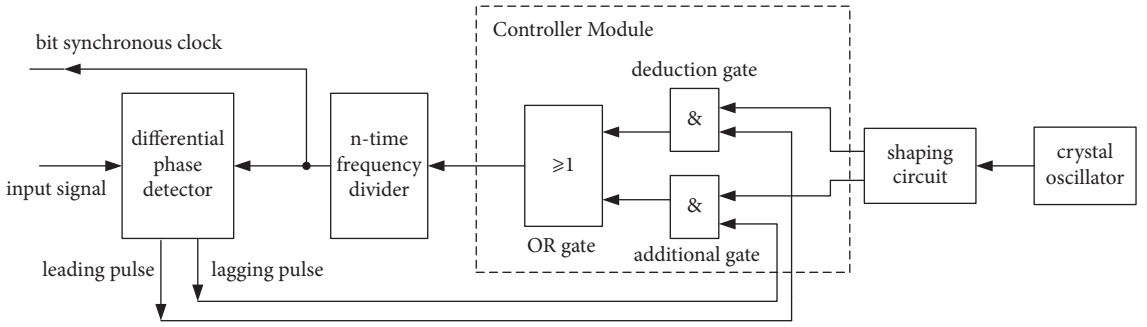

Figure 1: Structure diagram of DPLL.

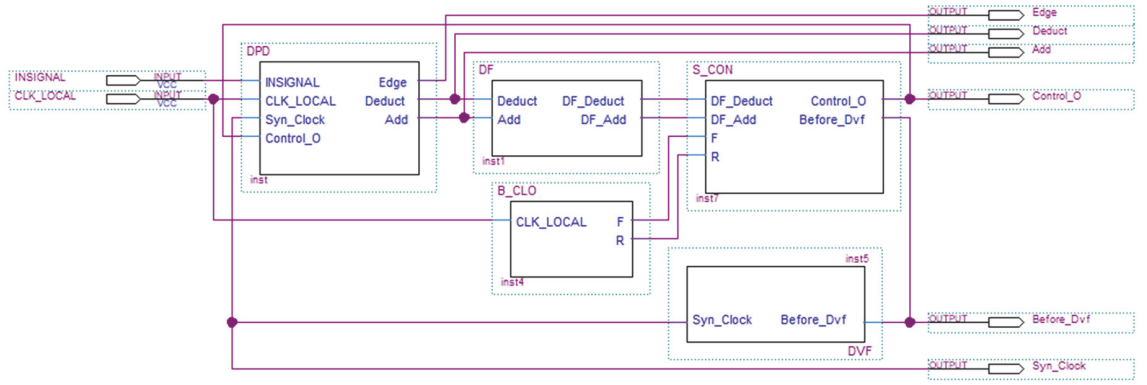

Figure 2: Schematic of bit synchronization clock extraction system based on DPLL.

leading and lagging control pulses as input signals to the control module. The controller in the figure consists of a deduction gate, an additional gate, and an OR gate circuit. The output of the control module is sent to the n-time frequency divider for frequency division. The final generated bit synchronized clock signal is used both for the sampling decision of the receiver of the digital communication system and as the feedback signal input to the differential PD [6, 16].

If the Baud rate of the receiving code is F Baud, the frequency of the bit synchronized clock sequence must also be F Hz. As shown in Figure 1, if the oscillation frequency of crystal oscillator is set as nF Hz, the frequency of the narrow pulses after shaping is $nF/2$ Hz, and the frequency of the adjusted signal after the controller is nF Hz; after n-time frequency division, the bit synchronous clock signal with a frequency of F Hz is obtained. If the clock signal is not exactly in the same frequency and phase as the receiving signal, we have to use the controller to adjust the input of the frequency divider according to the phase difference signal generated from the PD. In this way, the phase of the bit synchronized clock can be changed and adjusted constantly in the phase-locked loop until the accurate synchronization signal is obtained [3].

3. The Implementation of Bit Synchronous Clock Extraction System Based on FPGA

According to the principle mentioned above, the typical extraction circuit requires four parts for bit synchronized signal extraction. In order to reduce the jitter problem after synchronization, a digital filter module is implemented is this design, and VHDL (Very-high-speed Integrated Circuit Hardware Description Language) with FPGA (Field-Programmable Gate Array) is used for the system design and performs the simulation verification on Quartus II [17–20]. The top layer schematic of the system, as shown in Figure 2, consists of five modules: differential phase detector (DPD), digital filter (DF), biphasic clock source (B_CLO), controller (S_CON), and frequency divider (DVF).

3.1. Differential Phase Detector Module. The differential phase detector circuit consists of a differential circuit and a PD circuit, as shown in Figure 3. The input digital sequence (INSIGNAL) is transformed into the corresponding rising edge detection narrow pulse signal (Edge) after the differential circuit., which is then added to the deduction gate (AND2) and the additional gate (AND3), respectively.

If the phase of the bit synchronized clock (Syn_Clock) is ahead of the edge detection signal, or the input sequence, the additional gate closes, and the deduction gate outputs at the same time a control signal (Deduct) to the follow-up circuit to deduct a clock pulse before frequency division and therefore to weaken the leading state. The simulation result is shown in Figure 4.

On the contrary, if the Syn_Clock is lagging behind, then the deduction gate closes, and the additional gate

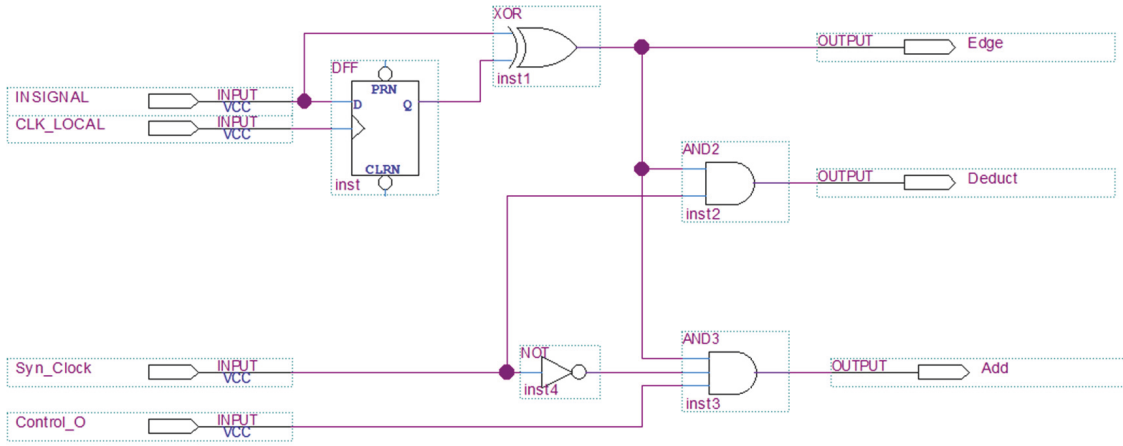

Figure 3: Schematic of differential phase detector.

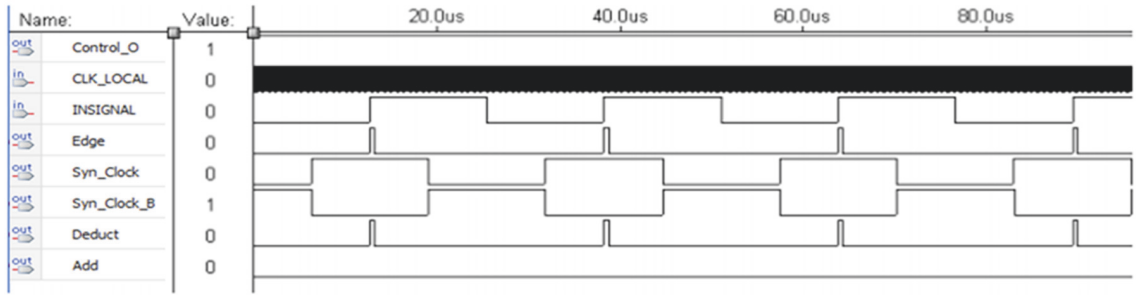

Figure 4: Simulation result of differential phase detector in phase lead.

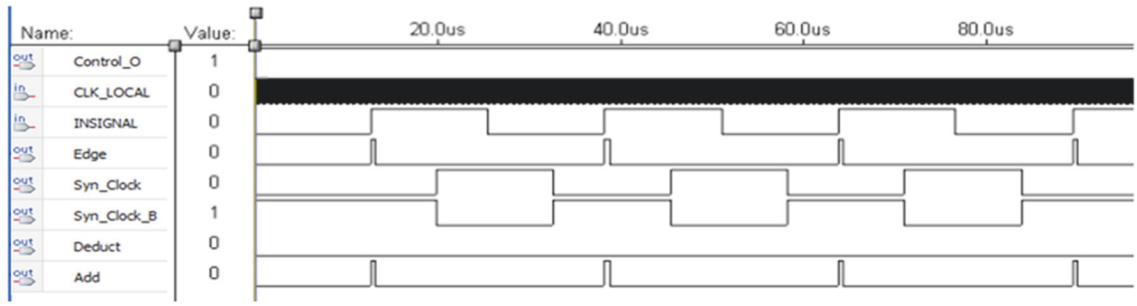

Figure 5: Simulation result of differential phase detector in phase lag.

generates a control signal (Add) to the follow-up circuit to add a clock pulse before frequency division to weaken the lagging state. The simulation result is shown in Figure 5.

3.2. Biphasic Clock Source Module. The circuit schematic of the biphasic clock source module is shown in Figure 6. On the one hand, this module is used to shape the crystal oscillator outputs to be with an output duty ratio of about 1/4. On the other hand, this module is used to generate two clock signals (F and R) which have a half frequency of the crystal oscillator output signal and with a phase difference of π. The simulation result is shown in Figure 7.

3.3. Control Module. The circuit schematic of the control module implemented by FPGA is shown in Figure 8, which mainly includes D flip-flop, constant-opened deduction gate (inst5), and constant-closed add gate (inst4).

When the phase of the synchronized clock is ahead, the leading control signal (DF_ Deduct) is a positive pulse, which is converted into low level after passing the trigger and NOT gate, making the constant-opened gate closed for one trigger period and deducting a pulse from the F signals, as shown in Figure 9. To the contrary, when the phase of the synchronized clock is lagged, the lagging control signal (DF_ Add) is a positive pulse, and a high level is generated by

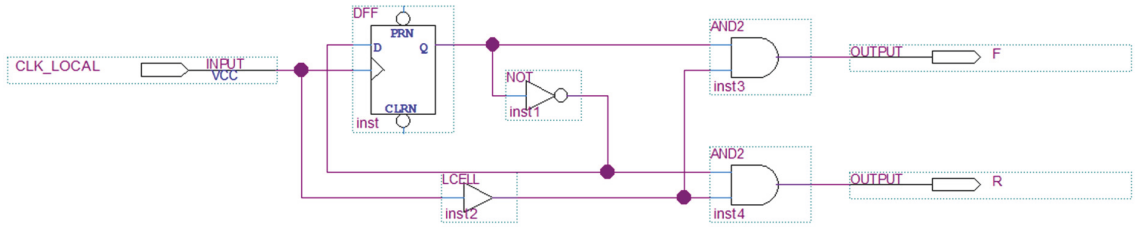

Figure 6: Schematic of biphasic clock source circuit.

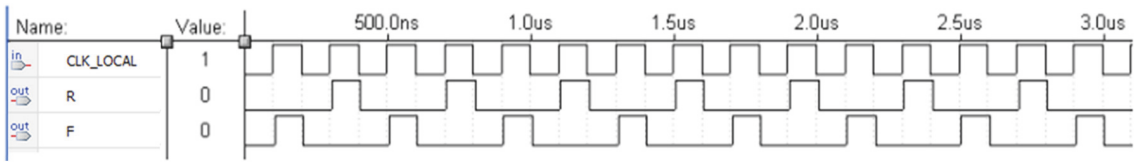

Figure 7: Simulation result of biphasic clock source circuit.

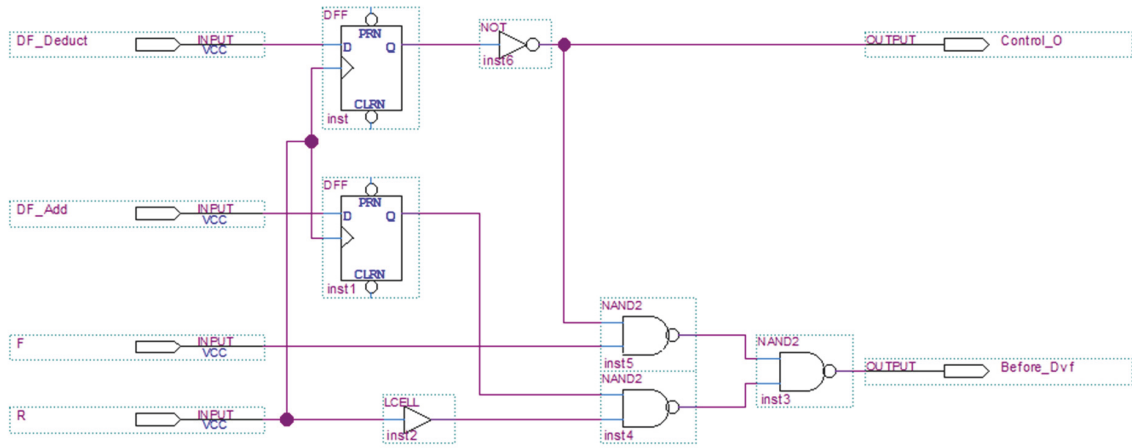

Figure 8: Schematic of the control module.

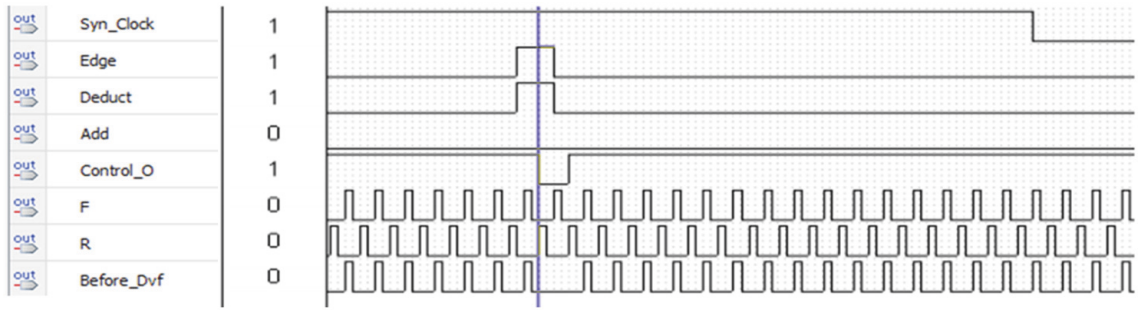

Figure 9: Simulation result of control module in phase lead.

the trigger, making the constant-closed gate opened for one trigger period and adding a pulse to the R signals, as shown in Figure 10.The adjusted biphasic clock (Before_ Dvf) is then sent to the divider after the OR gate, to achieve the goal of phase adjustment.

In this part of the design, an antiphase control signal (Control_O) output is added in the circuit to avoid the fake synchronization. When the descent edge of the bit synchronization signal is aligned with the edge detection signal, the input signal and the local synchronized clock signal are of the same frequency but reversed phase, making a synchronous illusion that the leading and lagging control pulses appear alternately in turns as shown in a real synchronization. In this case, the control module first deducts a pulse and then adds another, causing the phase of the Before_Dvf clock signal to be unchanged, therefore making it impossible to adjust the phase of the bit synchronized clock. This situation can be avoided by the Control_O signal output from the controller, with a

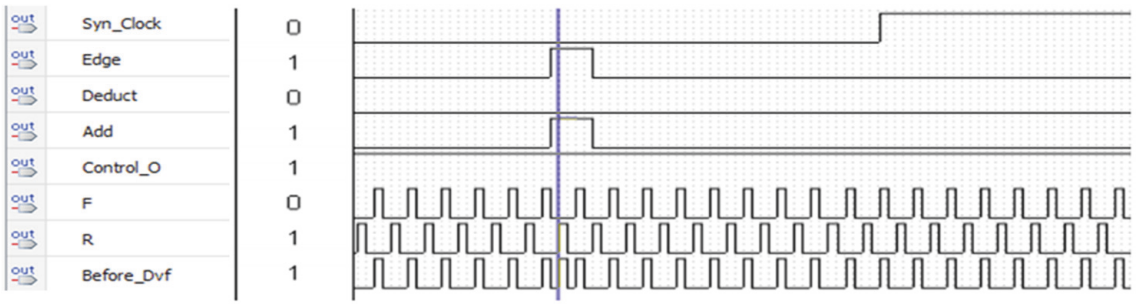

Figure 10: Simulation results of control module in phase lag.

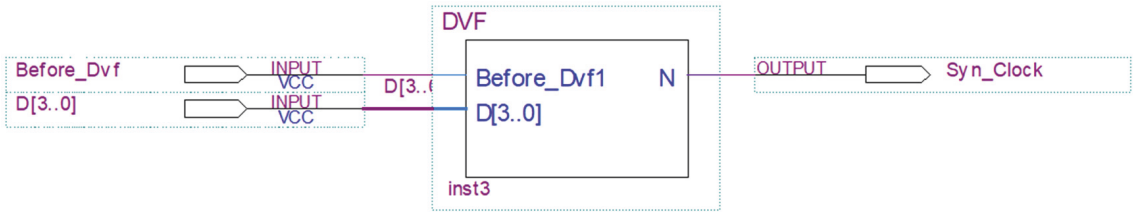

Figure 11: Schematic of numerically controlled frequency divider circuit.

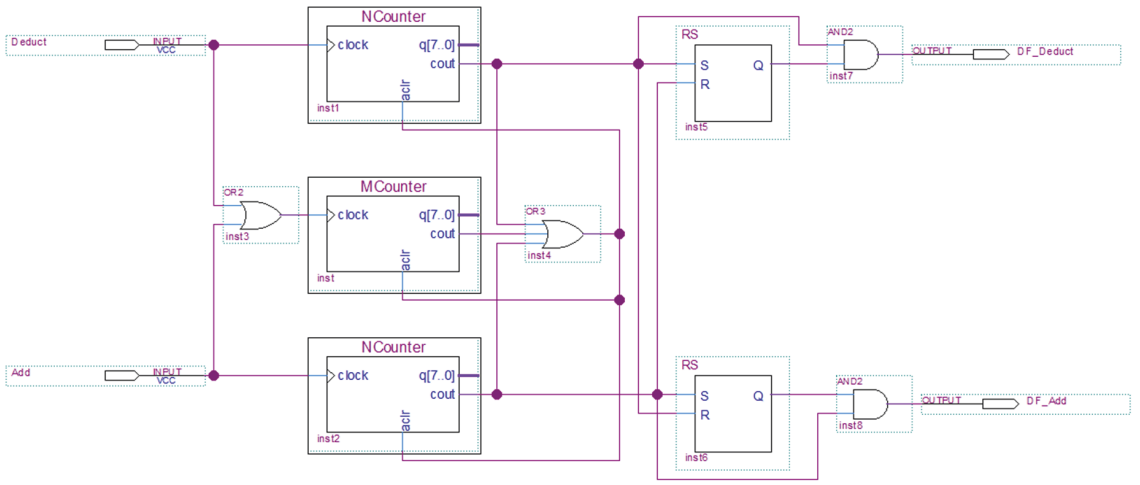

Figure 12: Schematic of digital filter circuit.

working process of the following: once the leading control signal (DF_Deduct) is sent into the controller, Control_O is turned to low level and the signal is fed back to stop adding gate (AND3) in the differential PD, so that control pulses with added pulses (ADD) are not generated, making the entire phase-locked loop continue to work properly.

3.4. Frequency Division Module. The numerically controlled frequency divider module is shown as in Figure 11, Before_Dvf is the input clock, d[3..0] is the port for setting the frequency divider's coefficient, and n is the clock signal after frequency division, or the required bit synchronized clock.

3.5. Digital Filter Module. Without this implementation of a digital filter module, the output leading control signal (Deduct) and lagging control signal (Add) from the differential PD will be sent directly to the corresponding port of the control module, to perform a deducting or an adding to the biphasic pulse. When a digital filter module is added, the leading and lagging control signals are first processed by the digital filter before being transmitted to the controller [21]. The details are described below.

As shown in Figure 12, the digital filter module sends the receiving leading and lagging controls signals to their respective N counters and sends their sum to the M counter, so that N and M satisfy the $N \leq M \leq 2N$. When any of the three counters is full, the carry pulse is output to the asynchronous zero end of the three counters. The three counters are cleared to zero at the same time and the counting restarts.

If the phase of the bit synchronized clock is ahead of the input signal, the continuous output of differential PD will

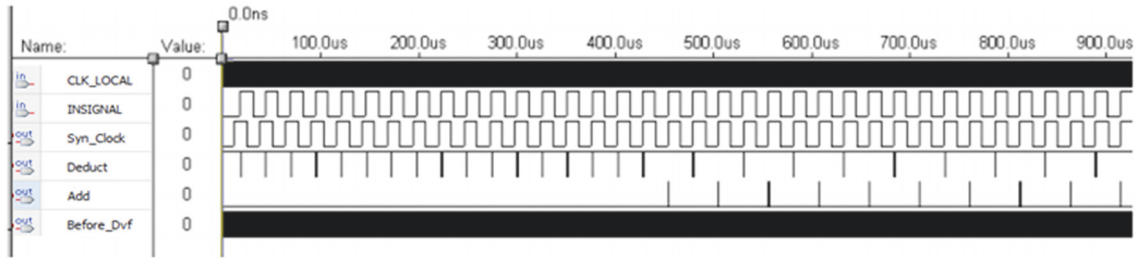

Figure 13: System simulated results without digital filter. CLK_LOCAL: the local clock, INSIGNAL: the input signal, Syn_Clock: the synchronization clock, Deduct: the leading control pulse of PD, Add: the lagging control pulse of PD, and Before_Dvf: control module output/frequency divider input.

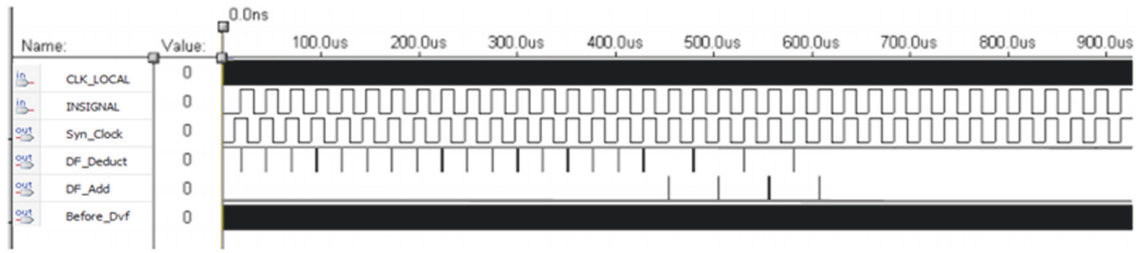

Figure 14: System simulated results with adding digital filter. CLK_LOCAL: the local clock, INSIGNAL: the input signal, Syn_Clock: the synchronization clock, DF_Deduct: the leading control pulse of digital filter module, DF_Add: the lagging control pulse of digital filter module, Before_Dvf: control module output/frequency divider input.

fill the N counter with the number of leading control pulse first. Then the trigger inst5 outputs high level and opens the AND gate inst7, through which the leading control pulse is output to the control module. If the filter continues to receive the leading control pulse, these leading pulses (DF_Deduct) will be continuously output as the inst7 gate is in the open state. Similarly, if the phase of the bit synchronized clock dose lags behind the input signal, the continuous output of differential PD will fill the counter with the number of lagging control pulse first. The trigger inst6 outputs high level and opens the AND gate inst8, and the lagging control pulse passes through inst8 gate to the control module. If the filter continues to receive the lagging control pulse, these lagging pulses (DF_Add) will be continuously output as the inst8 gate is in the open state.

When it is in the synchronous (locked) working state, as the phase difference between the input signal and the synchronized clock is small, the DPLL is toggling in both the leading and lagging states, as shown in Figure 13 for the Deduct and Add pulses. In addition, when a phase difference is observed between the input signal and the synchronized clock due to the noise, a leading state or a lagging state caused by the random errors will be observed with the same probability. It will also lead to the DPLL toggles in both the leading and lagging states, leading to the phase jitter of the bit synchronized clock. In both cases, either of the two N counters is not full, but three counters will be cleared as the M counter is already full, so the digital filter module dose not output any leading and lagging control pulses, and the subsequent controller does not make any adjustment to the phase of the local clock. As a result, the adjustment to the phase of the synchronized clock in the dynamic stability state is relieved and the jitter problem is avoided. The simulation results are shown in Figure 14.

4. System Simulation Results and Analysis

The system simulation results without and with a digital filter are shown in Figures 13 and 14, respectively. By comparing the results shown in these two figures, we can see that the use of a digital filter eliminates the problem of the alternate occurrence of the leading and lagging control pulses after synchronous locking.

In Figure 13, a dynamic balance status is reached in the latter half of the simulation diagram. As the edge detection pulse has a fixed width, the jump edge of Syn_Clock is located in the middle of the edge detection pulse when compared to Syn_Clock. Therefore, the leading and lagging control pulses circulate alternately. The system deducts a pulse before the leading pulse is received and adds a pulse after lagging pulse is received, causing the entire system to be in a dynamic balance state, or a synchronous locking state, or the bit synchronized state that our design is pursuing.

However, when it is locked in the synchronous working state, the DPLL is just toggling in both leading and lagging states as the phase difference between the input signal and the bit synchronized clock is small. In addition, when a phase difference is observed between the input signal and the synchronized clock due to the noise, a leading state or a lagging state caused by the random errors will be observed with the same probability. It will also lead to the DPLL toggles in both the leading and lagging states, leading to the phase

jitter of the bit synchronized clock. The above two conditions make the system inefficient and increase system consumption [22, 23].

In Figure 14, the required synchronization state is also reached in the latter half of the simulation diagram, but the toggling no longer occurs and the phase jittering of bit synchronized clock caused by the toggling is therefore avoided.

5. Conclusion

In this paper, the digital phase-locked technique is implemented in our design of extraction of the phase synchronization clock. The phase difference information of the phase detector is firstly processed with an improved method and then sent to the controller to adjust the phase of the output clock. As a result, accurate synchronization pulse extraction is obtained, while at the same time the jitter phenomenon is reduced, the system anti-interference ability is increased, and the operating efficiency is improved. Furthermore, antiphase control signals are also added in our design to prevent the fake sync state and ensure that the DPLL is able to work properly. FPGA chip, VHDL hardware description language, and Quartus II are used to perform the system design and simulation. The results show that this bit synchronous extraction circuit achieves the expected goal of improvement, which is expected to be better applied in the actual digital communication system.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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