KU LEUVEN

P&D Electronics and Chipdesign GMSK100

Group 4:

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- Jasper Depuydt
- Ruben Heyrman
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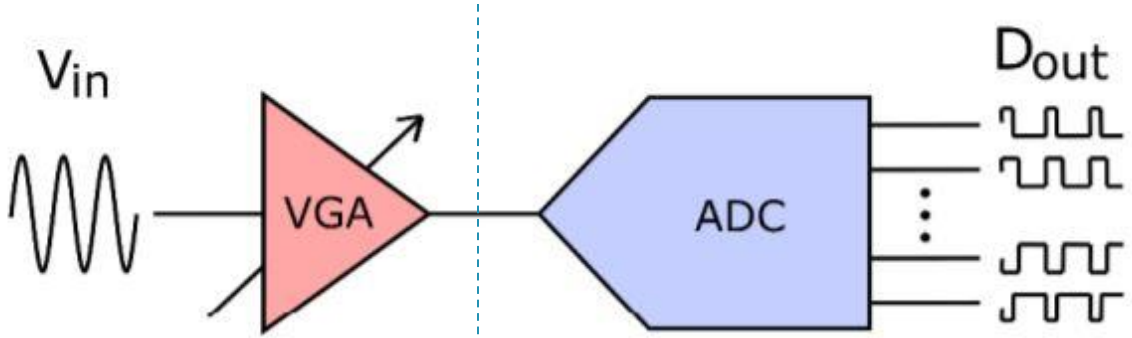
Midterm Presentation

Analog



- Variable gain amplifier: amplifies 1..100 mV input signal to desired level for ADC

- ADC: converts analog input to digital N-bit output
- SNR = 6.02N+1.76dB

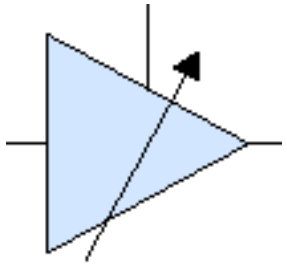
- Sampling at certain Fs

Variable Gain Amplifier

Specifications

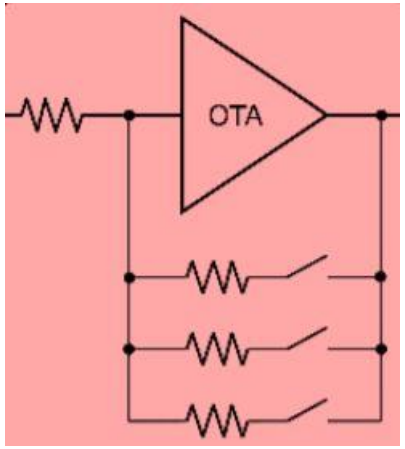
- Input = 1..100mV, output = 500 mV

  -> Closed Loop gain = 5..500



Solution 1.0

- Telescopic OTA
- 85 dB gain, 25 kHz BW
- Resistorbank feedback
- Gain = -Rf/Rin (ideal)

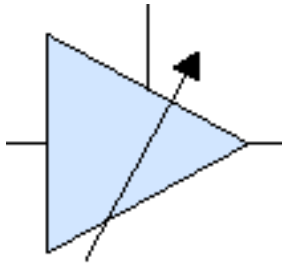


Variable Gain Amplifier

Specifications

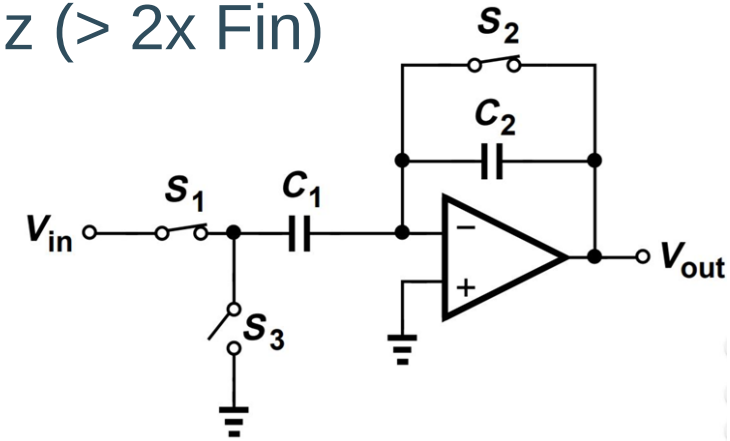
- Input = 1..100mV, output = 500 mV

  -> Closed Loop gain = 5..500



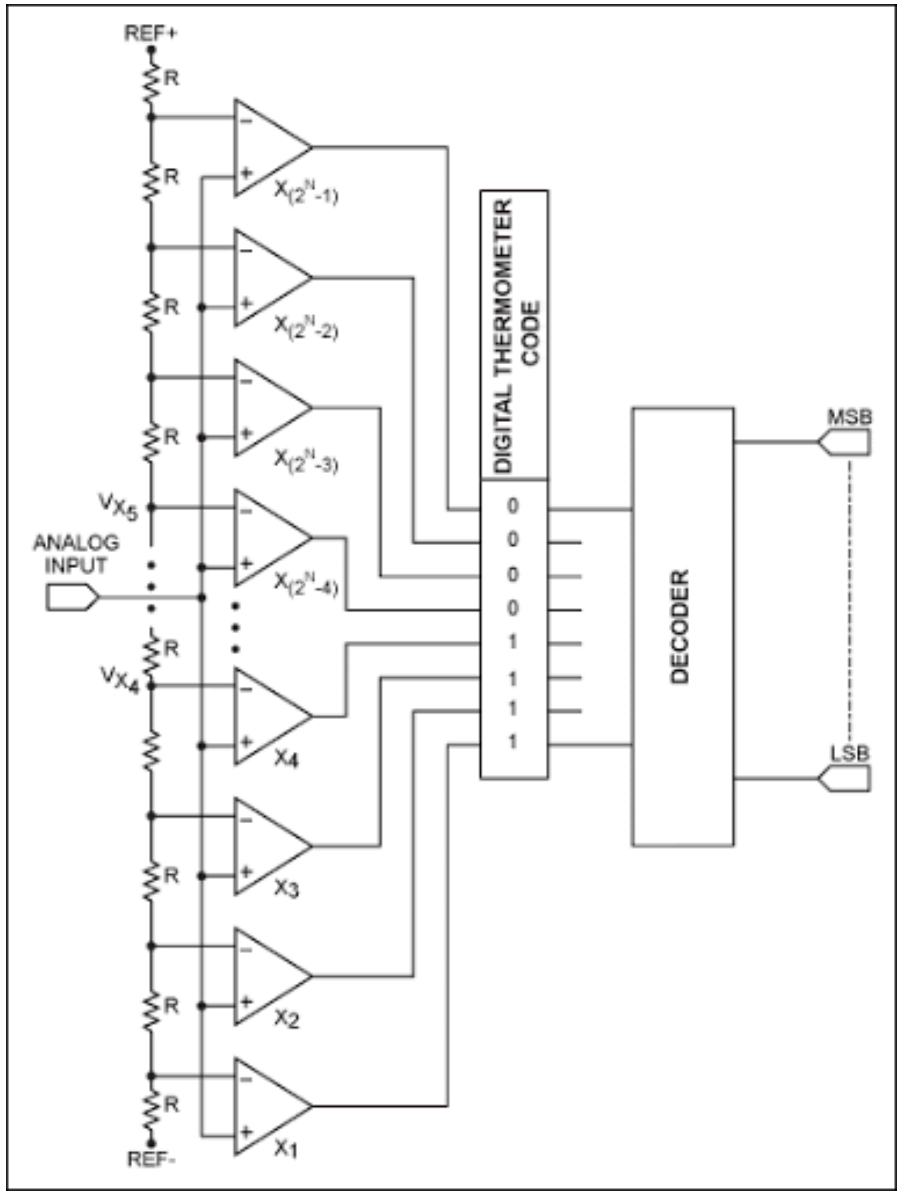
Solution 2.0

- S&H amplifier
- Capacitorbank feedback
- Gain = -C1/C2 (ideal)
- Fs = 60 kHz (> 2x Fin)



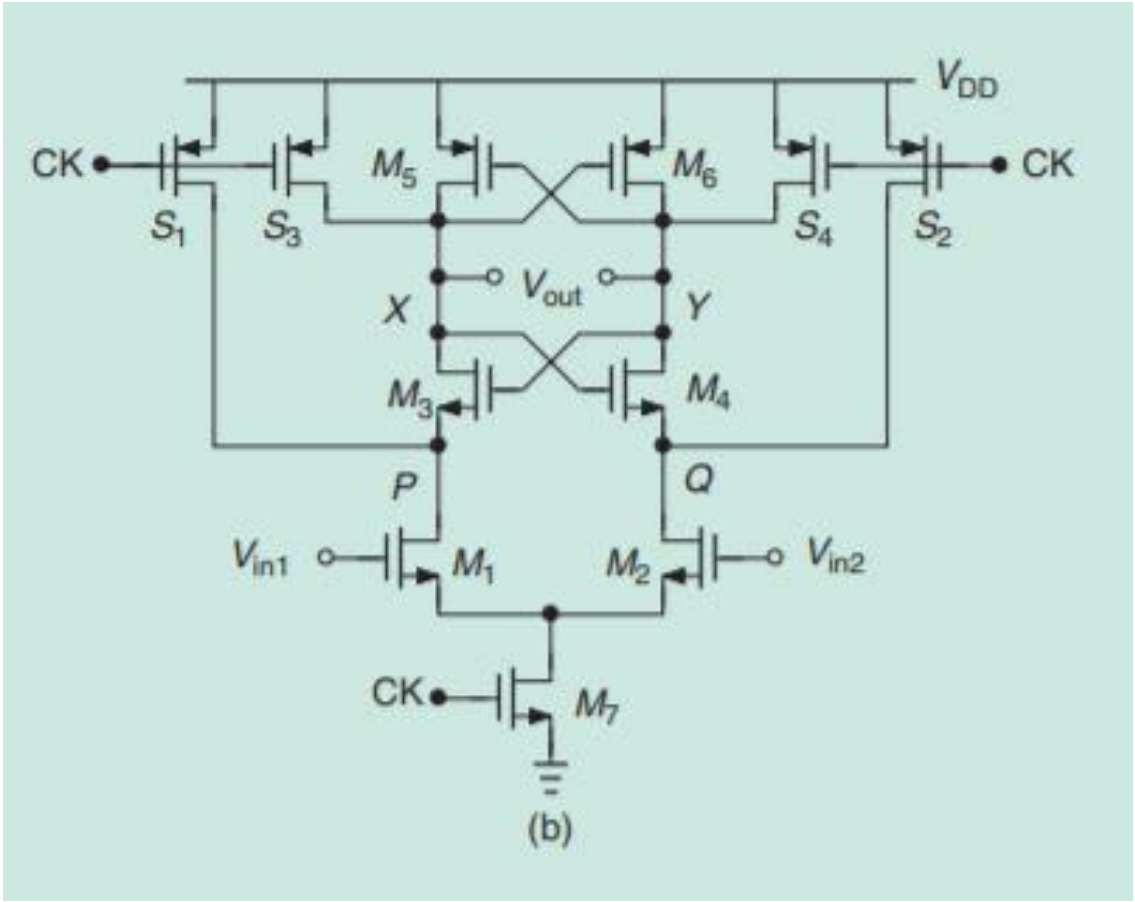
Flash ADC

- 3-bit -> SNR = 6.02N+1.76 dB = 20 dB
- Thermometer code
- Mux-based decoder = easy to implement and small enough delay for Fs
- Resistorchain for Vref
- 7 StrongArm comparators (see next slide)
- Vref decoupled



StrongArm Comparator

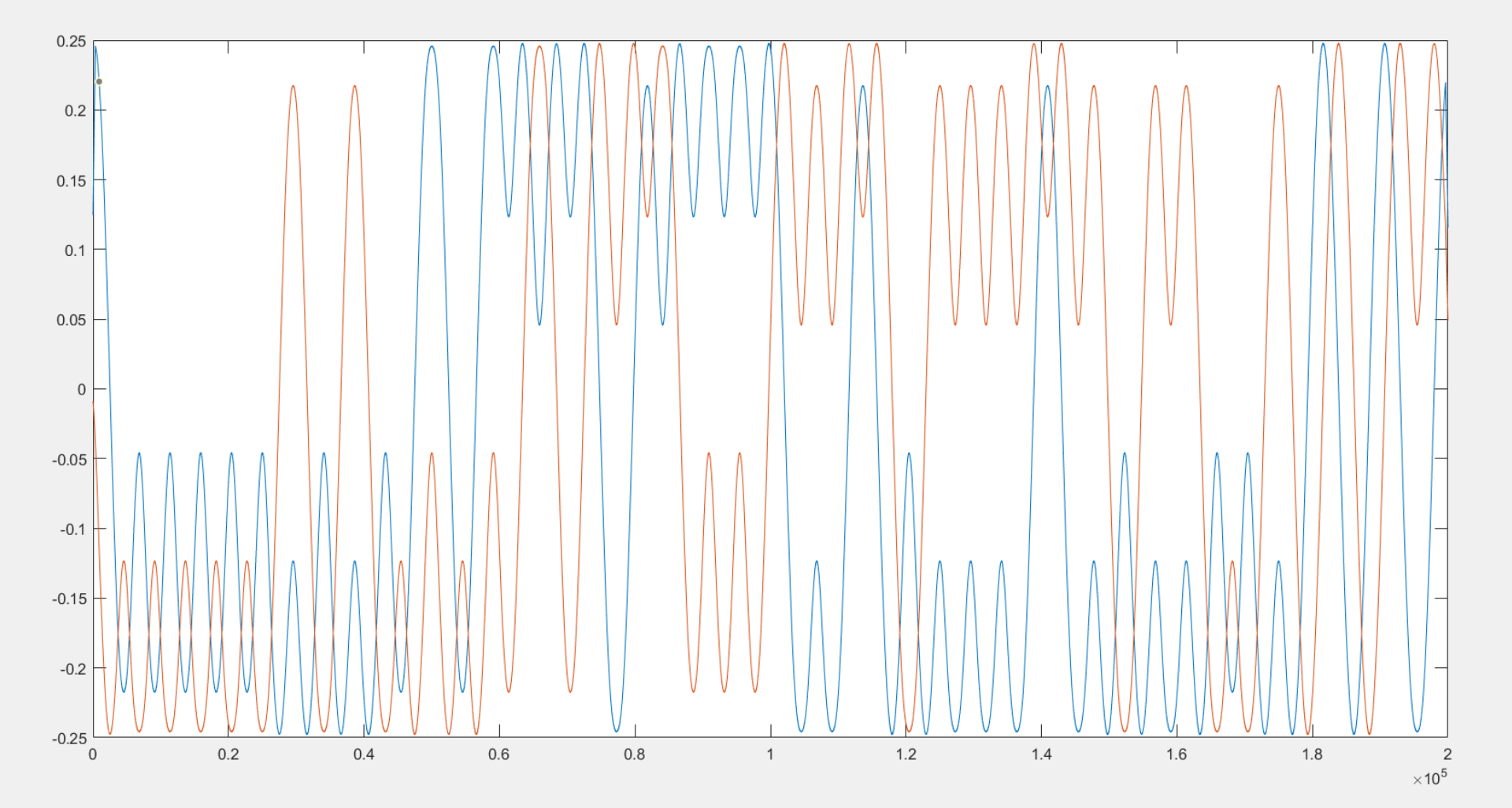
- Vin2 = input
- Vin1 = Vref
- Combines functionality of comparator and latch
- Capacitive load matching with invertors at X and Y



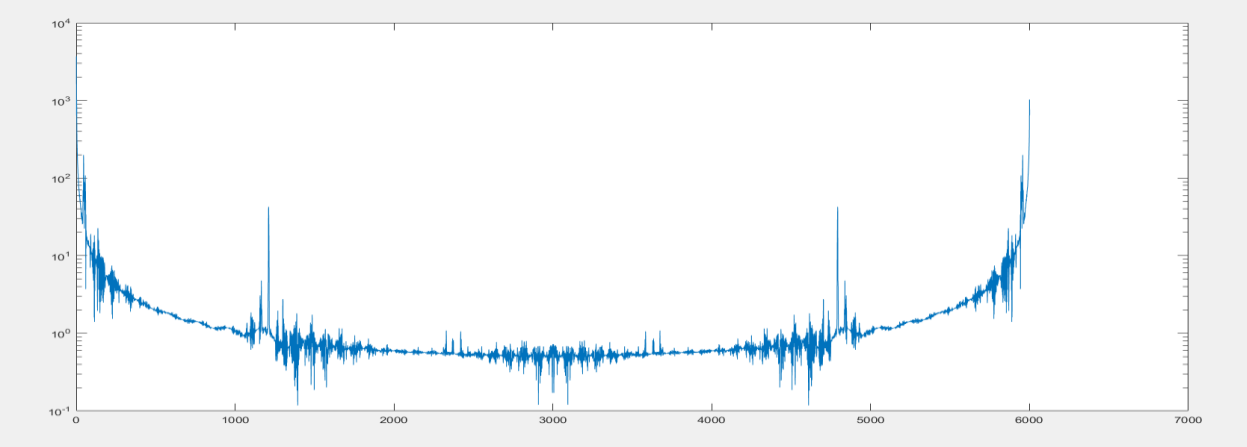
To do

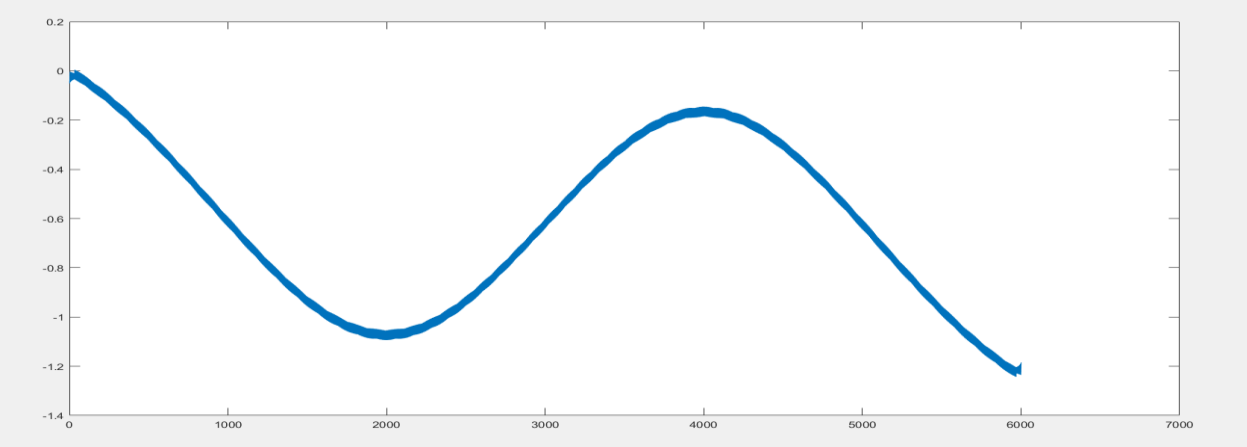
- Design new OTA
- Implement S&H switchcap circuit
- Optimize ADC

Digital

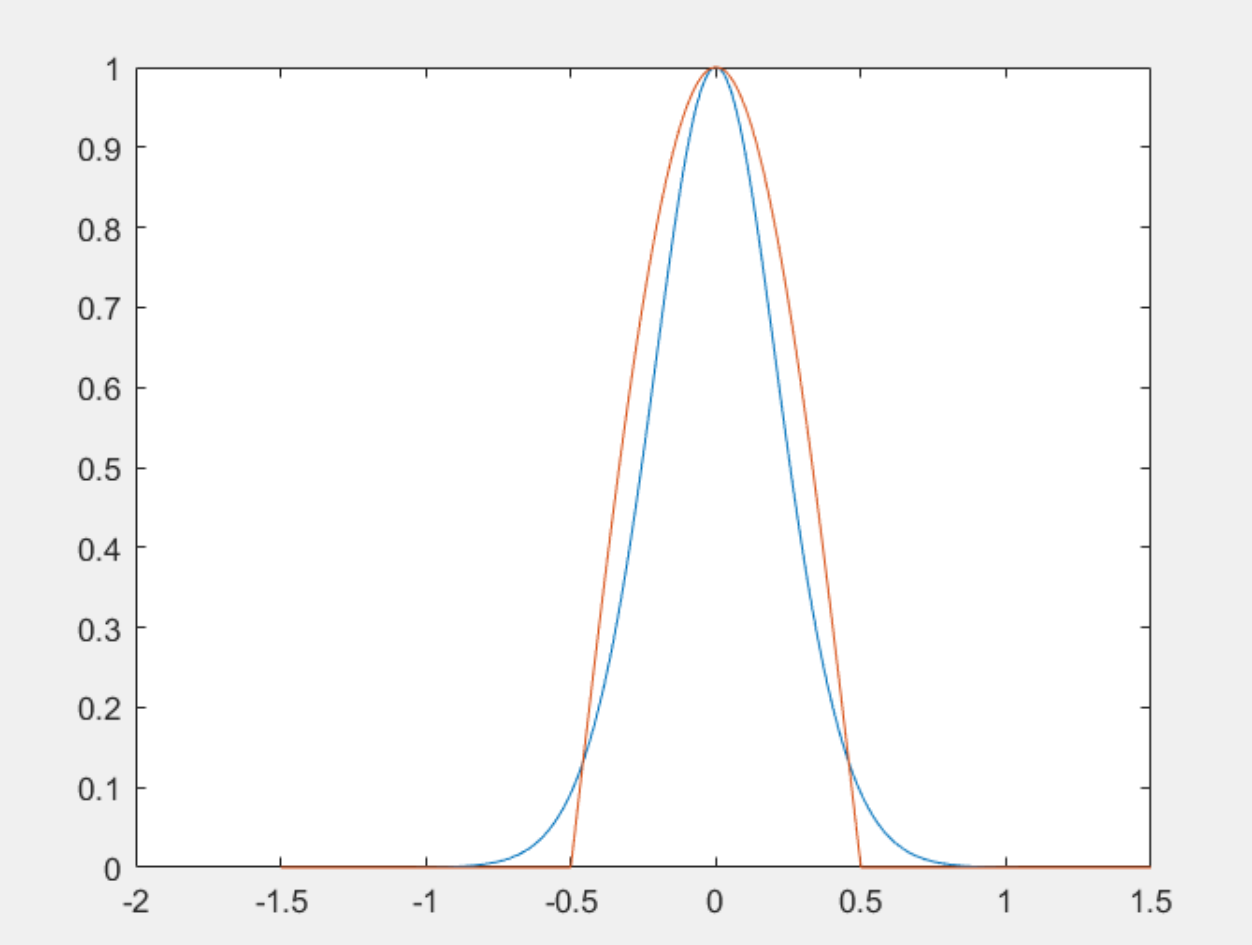


Finding the perfect matched filter in Matlab

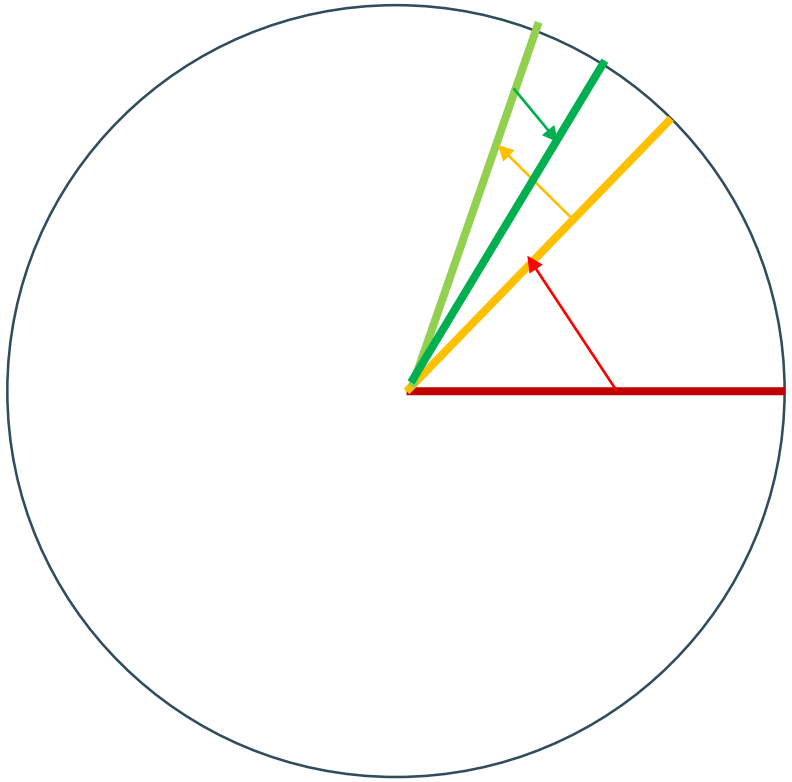


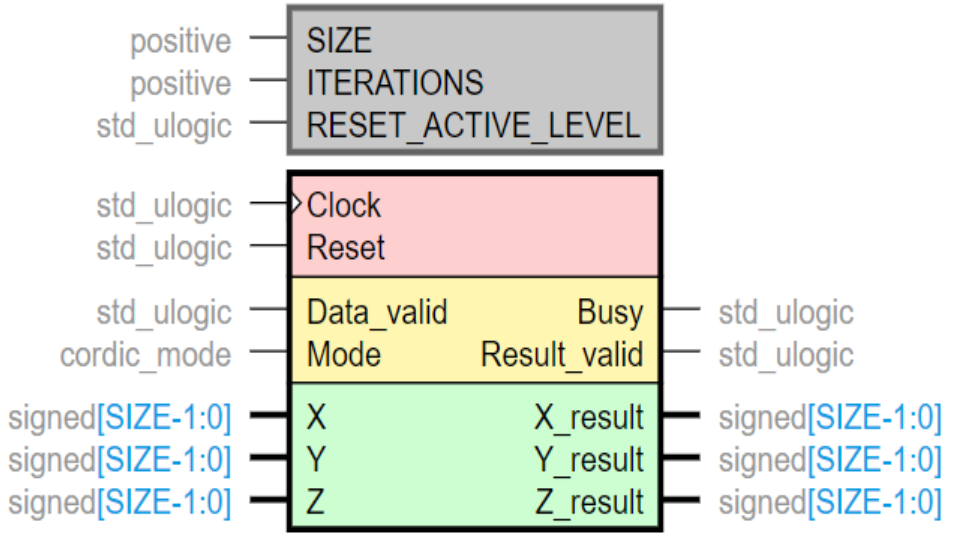


Matched filter pulse shape vs regular MSK

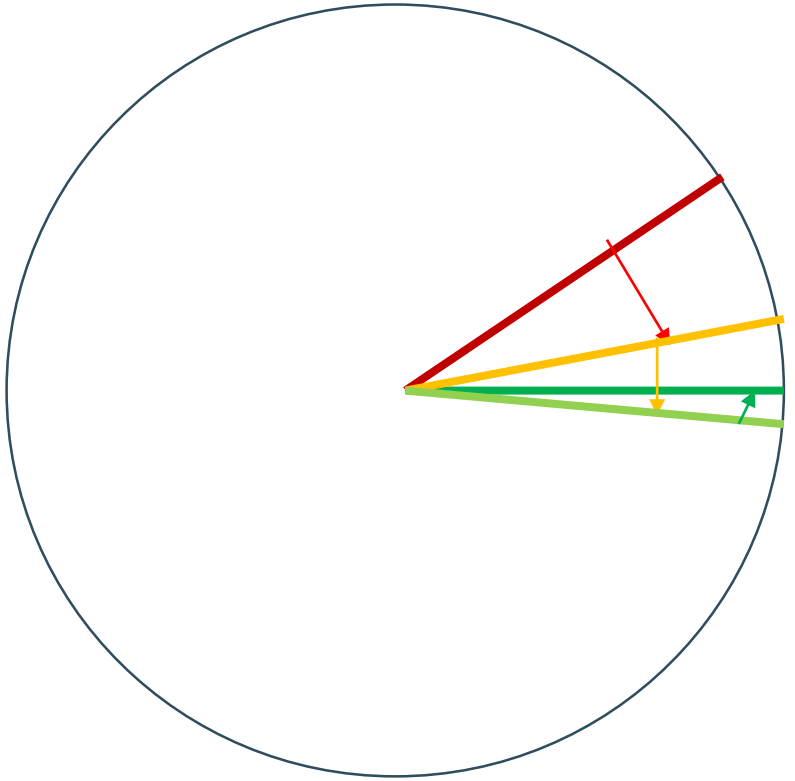


CORDIC:

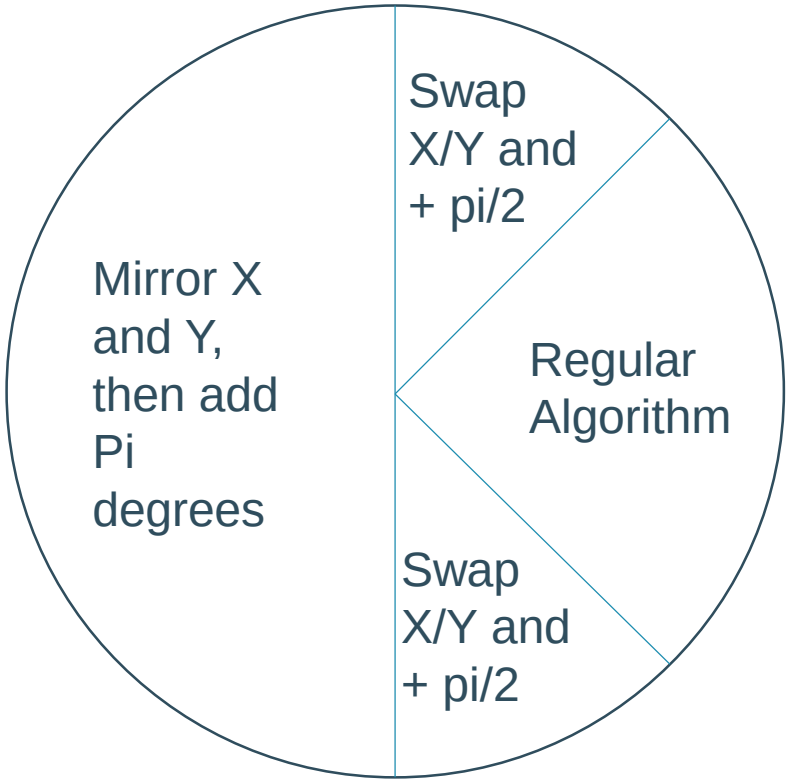



positive
positive
std_ulogic
SIZE
ITERATIONS
RESET_ACTIVE_LEVEL
std_ulogic
std_ulogic
Clock
Reset
std_ulogic
cordic_mode
Data_valid
Mode
Busy
Result_valid
std_ulogic
std_ulogic
signed[SIZE-1:0]
signed[SIZE-1:0]
signed[SIZE-1:0]
X
Y
Z
X_result
Y_result
Z_result
signed[SIZE-1:0]
signed[SIZE-1:0]
signed[SIZE-1:0]

VHDL: CORDIC ARCTAN ROTATE UNTIL (1,0)



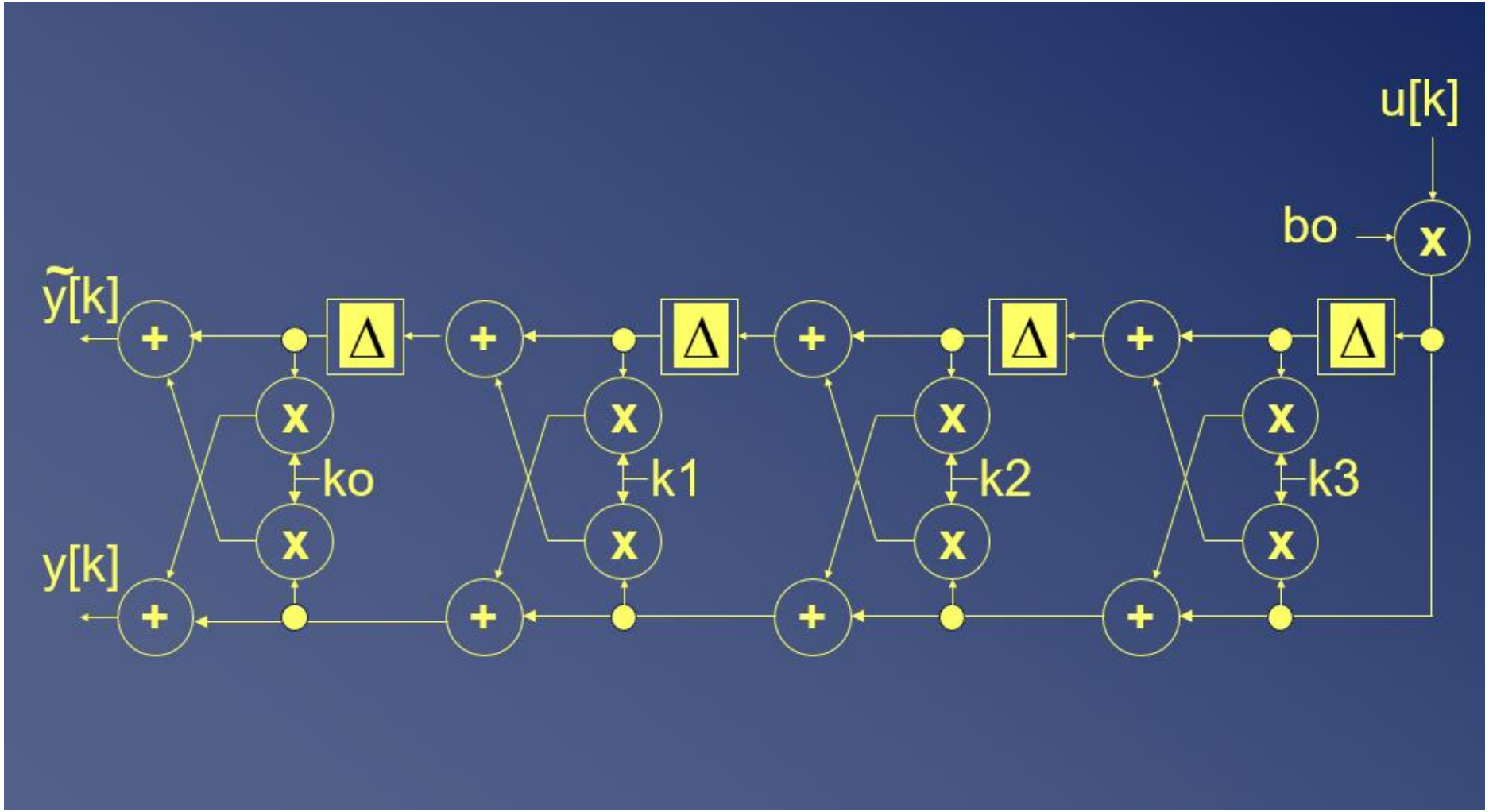
If outside circle, mirror, possibly in combination with swapping x and y



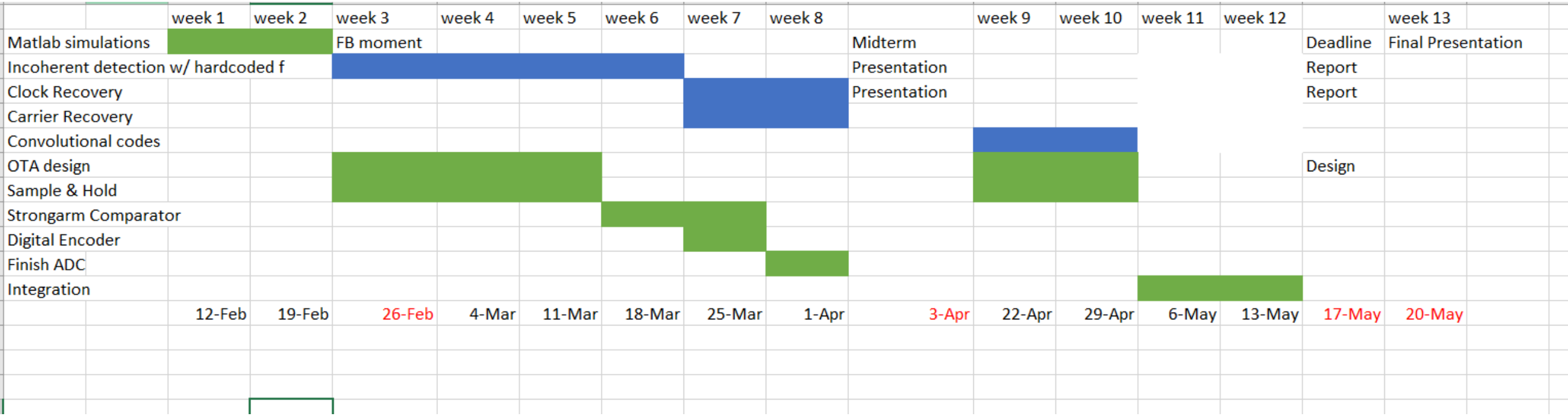
Varicode is just a table lookup (big if else statement)

Symbol(s)	Char	Symbol(s)	Char	Symbol(s)	Char	Symbol(s)	Char
0	SPACE	0-29	@	0-30	~	0-31	=
1	a	1-29	A	1-30	1	1-31	[
2	b	2-29	B	2-30	2	2-31	\
3	c	3-29	C	3-30	3	3-31	]
4	d	4-29	D	4-30	4	4-31	^
5	e	5-29	E	5-30	5	5-31	
6	f	6-29	F	6-30	6	6-31	{
7	g	7-29	G	7-30	7	7-31	
8	h	8-29	H	8-30	8	8-31	}
9	i	9-29	I	9-30	9	9-31	`
10	j	10-29	J	10-30	0	10-31	±
11	k	11-29	K	11-30	!	11-31	÷
12	l	12-29	L	12-30	quote	12-31	°
13	m	13-29	M	13-30	#	13-31	×
14	n	14-29	N	14-30	$	14-31	£
15	o	15-29	O	15-30	%	15-31	
16	p	16-29	P	16-30	&	16-31	
17	q	17-29	Q	17-30		17-31	
18	r	18-29	R	18-30	(	18-31	
19	s	19-29	S	19-30	)	19-31	
20	t	20-29	T	20-30	*	20-31	
21	u	21-29	U	21-30	+	21-31	
22	v	22-29	V	22-30	-	22-31	
23	w	23-29	W	23-30	/	23-31	
24	x	24-29	X	24-30	:	24-31	
25	y	25-29	Y	25-30	;	25-31	
26	z	26-29	Z	26-30	<	26-31	
27	.	27-29	,	27-30	>	27-31	BS
28	CRLF	28-29	?	28-30	IDLE	28-31	DEL

Differentiator and matched filter via lattice ladder



Planning


week 1
week 2
week 3
week 4
week 5
week 6
week 7
week 8
week 9
week 10
week 11
week 12
week 13
Matlab simulations
FB moment
Midterm
Deadline
Final Presentation
Incoherent detection w/ hardcoded f
Presentation
Report
Clock Recovery
Presentation
Report
Carrier Recovery
Convolutional codes
OTA design
Design
Sample & Hold
Strongarm Comparator
Digital Encoder
Finish ADC
Integration
12-Feb
19-Feb
26-Feb
4-Mar
11-Mar
18-Mar
25-Mar
1-Apr
3-Apr
22-Apr
29-Apr
6-May
13-May
17-May
20-May