Analog design document P&D Ruben

# Variable gain amplifier

For the variable gain amplifier, an OTA and a digitally controlled system for automatic gain control (AGC). We want the OTA to be as close as possible to an ideal OTA, while considering the required bandwidth, the input CM range and so on. To ensure that the signal is within the input range of the ADC and makes us of the full dynamic range of the ADC, AGC is used. AGC can be implemented via digitally controlled switches that adjust the value of the (parallel) resistors that define the gain of the circuit.

## Proposed specifications and topology for the OTA

Gain: 40 dB or higher   
Bandwidth: at least 20.5 kHz (Carrier frequency)  
GBW: at least 2.05 MHz   
Input signal: 1 – 100mV (Amplitude)  
Topology: cascoded OTA (telescopic OTA, symmetrical OTA, combination, with gain-boosting)  
=> multistage for the required gain

## Automatic gain control

By looking at the most significant bit of the samples after the ADC, clipping or inefficient use of the dynamic range can be detected. A few successive samples can indicate clipping (all 1’s) or unused bits (all 0’s). With digital circuitry a system of parallel resistors can be switched on and off to convert the amplitude of the input signal ranging from 1 mV up to 100 mV to a consistent value.

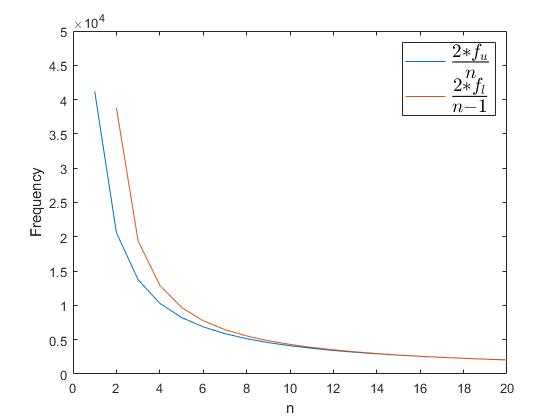
# Analog-to-digital converter

The proposed Analog-to-Digital converter (ADC) is a 3-bit Flash ADC. This ADC is easy to implement, but will be power hungry. If we want to make the circuit less power hungry, we should switch over to a SAR implementation for example.

## Time sampling

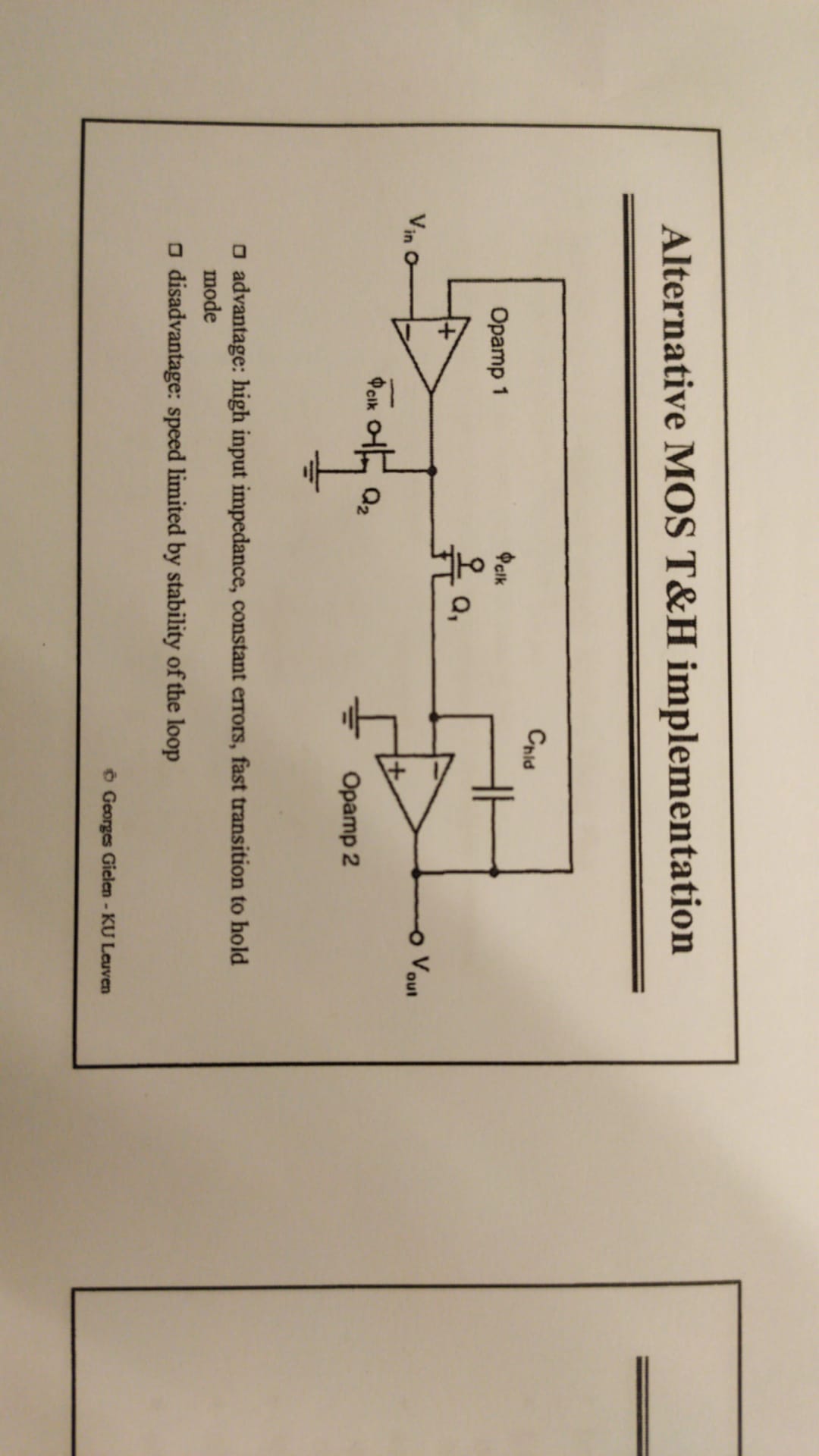
The sample rate for a bandpass signal can be lower than the Nyquist rate while reconstruction of the signal is still possible. The condition the sample rate needs to satisfy is:

Where is the upper frequency and is the lower frequency of the frequency band used by the bandpass signal and is a positive integer. Since the signal is an IF-signal at a carrier frequency of 20 (± 0.5) kHz and the signal has a bandwidth of 100 Hz, the upper frequency will be 20600 Hz and the lower frequency will be 19400 Hz.



The figure shows that the possible values for n are . The sampling frequency will therefore have to be higher than at least 2,4 kHz. Actually, the minimum sampling rate will be a little higher than 2.4 kHz, because is floored to the first integer value 17. The proposed ADC will have a sampling rate of 3 kHz.

Time sampling will be done using a MOS Track & Hold implementation seen in the figure below:



The clock is implemented digitally and fed back to the T&H circuit.

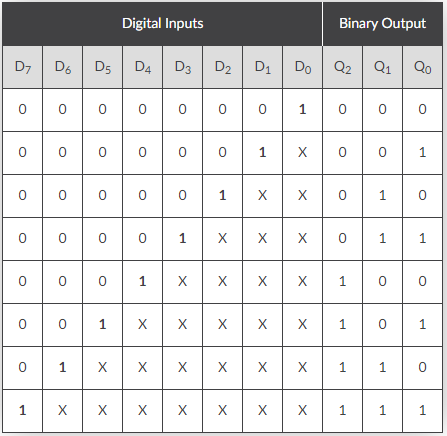
## Amplitude quantisation

Technology supply voltage is 3.3 V. So for a rail-to-rail ADC the closed-loop amplification should be about 3300 in the worst case (1 mV input signal). Because the bandwidth of the signal should at least be 20.5 kHz, this is impossible to achieve with a single-stage amplifier.

for FSR = 3.3 V

for n = 3 bits

## Digital 8-to-3 bit priority encoder



Because no D’s will be high at the same time, for the interpolating flash ADC, all the zero to the left will also be X (= don’t care).