

# ANDREW X ZHONG

707 Continental Cir, Mountain View, CA 94040 • (217) 550-2869 • andrewxz@berkeley.edu • ocf.io/andrewxz

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## EDUCATION

**University of California, Berkeley** - Berkeley, CA

*Master of Engineering*, Computer Science - Visual Computing and Computer Graphics

05/2014

**University of Illinois at Urbana-Champaign** - Urbana, IL

*Bachelor of Science*, ECE with *Highest Honors*, Overall: 3.89/4.0, Technical: 3.92/4.0

05/2013

**Zhejiang University** - Hangzhou, China

*Chu Kochen Honors College*, Overall: 3.96/4.0

09/2008 - 06/2010

**Related Coursework:** Algorithms, Computer Vision, Computer Graphics, Machine Learning, Data Structures, Parallel Computing, Operating Systems, Computer Architecture, Web Development, Database, Leadership, Entrepreneur Finance

## SKILLS

**Languages:** C/C++, Python, Java, OpenGL, CUDA, OpenMP, HTML, CSS, JavaScript, SQL, VHDL, Verilog, x86

**Applications:** OpenCV, Motion Capture (VICON), Google Cloud Platform, Android, Kinect, MATLAB, ModelSim

## EXPERIENCE

**Magic Leap Inc.** - Lead Engineer in Performance and Data, Mountain View, CA

11/2015 - Present

- Streamlined perception algorithm batch verification and metrics visualization on local cluster/public cloud
- Motion capture / ground truth data generation and syntheses / spatial and temporal calibration

**Apple Inc.** - Performance Analysis Engineer, Cupertino, CA

06/2014 - 11/2015

- Performed use cases performance validation and trade-off analysis for next-generation mobile system-on-chips (SoCs)
- Implemented SoC models and interface layers to agent models/RTL and software simulation platforms in C/C++
- Initiated a trace-based system performance/traffic pattern analysis and visualization tool powered by python and sqlite3

**Qualcomm Research Silicon Valley** - Augmented Reality (Prof. Björn Hartmann), Santa Clara, CA 09/2013 - 05/2014

- Designed a user interface framework that delivers an interactive indoor navigation experience through 3D augmented graphical views aligned with indoor objects
- Demonstrated our application in the CITRIS Invention Lab at Berkeley, providing augmented navigation, interactive device instructions, demo products display and device reservation lookup for lab visitors and apprentices
- Developed on the Android mobile platform powered by OpenGL graphics, orientation sensors and a position simulator

**Qualcomm Inc.** - Graphics System Design Intern, San Diego, CA

05/2013 - 08/2013

- Initiated and developed text processing and pattern matching tools for massive netlist and log files
- Performed MIPI DSI (Display Serial Interface) modeling and video stream simulations

**Coordinated Science Laboratory** - Diagnosing Performance Violations at System Level Using Data Mining (Prof. Shobha Vasudevan), Urbana, IL

10/2012 - 05/2013

- Localized the latency and throughput violations using a concurrent pattern mining approach
- Applied domain knowledge to filter out up to 92.8% of transaction traces, increasing mining efficiency

**Beckman Institute** - Brain-controlled Programmable Embedded System, Urbana, IL

01/2013 - 05/2013

- Designed an EEG-signal-controlled tablet prototype with ~2.5 s response time and 95% reliability
- Earned Research Award in Senior Design Hall of Fame

**Qualcomm Inc.** - Algorithm and System Design Intern, San Diego, CA

06/2012 - 08/2012

- Implemented the color processing algorithm based on 3D look-up table gamut mapping for Mirasol Display
- Optimized memory placement algorithm and reduced look-up table size by a factor of 4

## PUBLICATIONS

Improving User Experiences in Indoor Navigation with Augmented Reality, *Technical Report No. UCB/EECS-2014-74*

Diagnosing Root Causes of System Level Performance Violations, *ACM/IEEE ICCAD 2013*

Troubleshooting Performance Violations at System Level Using Data Mining, *Poster at DAC 2013*

## HONORS

Eta Kappa Nu, Tau Beta Pi, National Society of Collegiate Scholars, IEEE, SIAM

Highest Honors at Graduation, O. Thomas and Martha S. Purl Scholarship, Dean's List

First-Class Scholarship for Outstanding Merits, 2008-2009

First Prize in National Physics Contest in Jiangsu, China, 2007

## **PROJECTS**

- Data Visualization Framework on VR Systems** - AT&T VR Mobile App Hackathon - San Francisco 06/2015
- Designed an immersive virtual reality framework for real-time data visualization on Gear VR with Unity Game Engine
  - Enabled users to literally walk into big data represented by dots and curves, zoom, pinch and travel in 4 dimensions
- Machine Learning** - CS Berkeley 01/2014 - 05/2014
- Applied logistic regression, SVM, decision trees, random forests, neural networks, K-means, PCA and etc. on various supervised/unsupervised classification/regression problems
  - Predicted day of the week with 98.84% accuracy with 15 months of daily traffic data in the bay area
- Parallel Computing** - CS Berkeley 01/2014 - 05/2014
- Parallelized matrix multiplication, particle simulation and Knapsack problem with OpenMP, MPI, CUDA or UPC
  - Implemented a generic parallelized framework of A\* search with both CUDA and OpenMP
- Augmented Object Detector - Android App** - CS Berkeley 09/2013 - 02/2014
- Detected objects from Android camera video stream with Haar training
  - Rendered the detected objects in a 3D virtual scene on top of camera view with OpenGL ES 2
- Operating Systems** - CS Berkeley and ECE UIUC 01/2013 - 02/2014
- Developed a multi-threaded HTTP server that supports asynchronous IO and thread-safe caching
  - Built a Linux-based OS in C and x86: paging, interrupts, system calls, program loader, page allocator, multiple terminals, scheduling, signals, sound and mouse support, shell extensions and GUI
  - Achieved 4th place out of 30 teams in the Microsoft Operating System Design Competition
- Computer Graphics and Computer Vision** - CS Berkeley 09/2013 - 11/2013
- Coded in C++ from scratch: a ray tracer that implements Phong shading, refraction and .obj file inputs
  - Developed in OpenGL: uniform subdivision, adaptive tessellation, obj & mtl inputs, vertex shading
  - Explored homography rectification, 3D reconstruction, edge detection, texture and digit recognition
- Pipelined Processor Design** - ECE UIUC 09/2012 - 12/2012
- Designed and verified datapath, control and cache of a 5-stage pipelined processor based on LC3b
  - Achieved 2nd place out of 22 teams in the AMD Processor Design Competition