**Kuwait University**
**College Engineering and Petroleum**
**Computer Engineering Department**

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# CpE-262: Fundamental of digital logic

## Semester: Spring

## HomeWork No. 6

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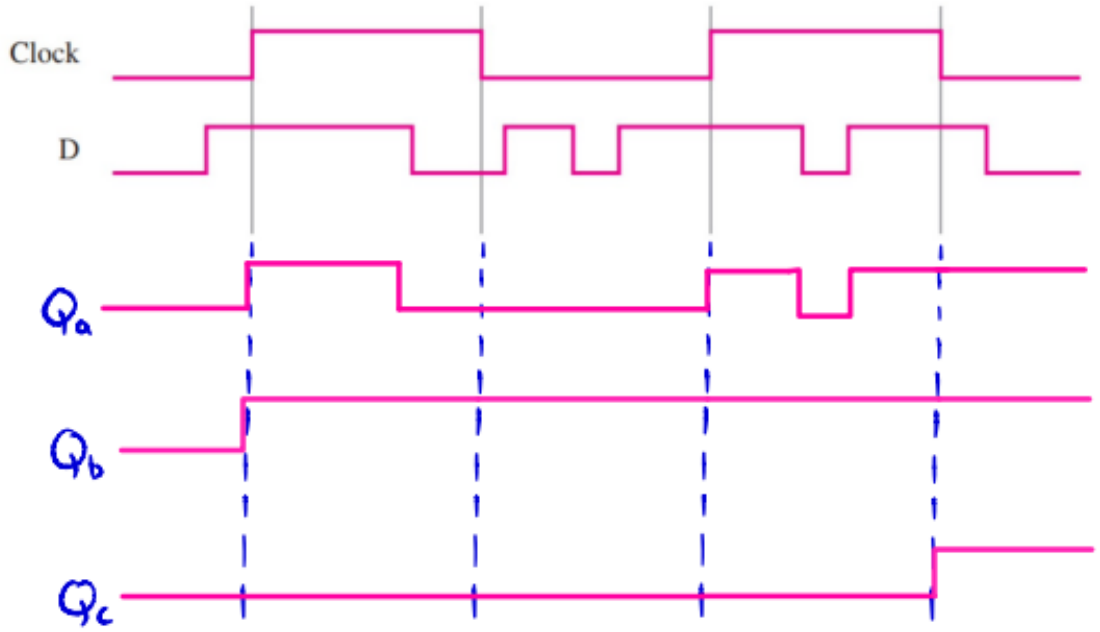
**Problem #1**

Consider the timing diagram in the Figure. Assuming that the D and Clock inputs shown are applied to the circuit in Figure 5.10 from the textbook, draw waveforms for the $Q_a$, $Q_b$, and $Q_c$ signals.



Problem #2

a. Design T-flip-flop and JK-flip-flop using D-flipflop.

- JK-flip-flop using D-flipflop

Qn+1 = JQ' + K'Q , D = Qn+1

| J | K | Qn | Qn+1 | D |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |

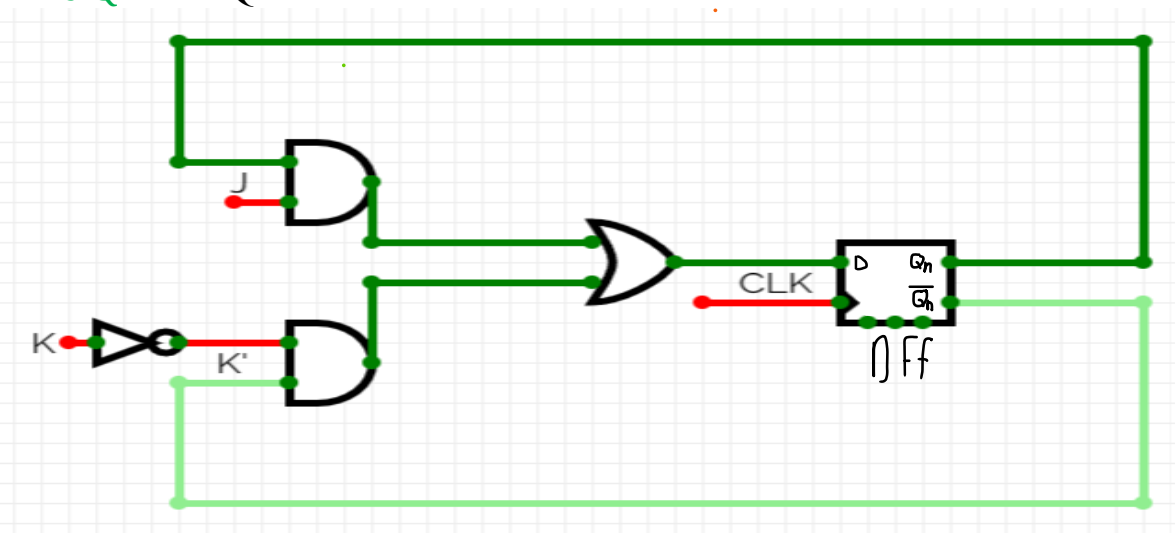
## EXCITATION TABEL FOR D-flipflop

| Qn | Qn+1 | D |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## K-MAP

| J K / Qn | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |

D = J Qn'+ K' Qn



- T-flip-flop using D-flipflop

Qn+1 = T XOR Qn , D = Qn+1

CHARACTERISTIC TABLE

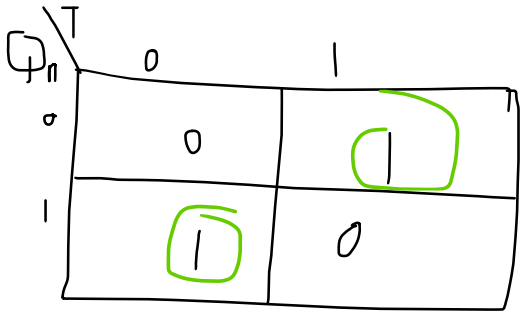
| T | Qn | Qn+1 | D |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

## EXCITATION TABEL FOR D-flipflop

| Qn | Qn+1 | D |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 1 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |

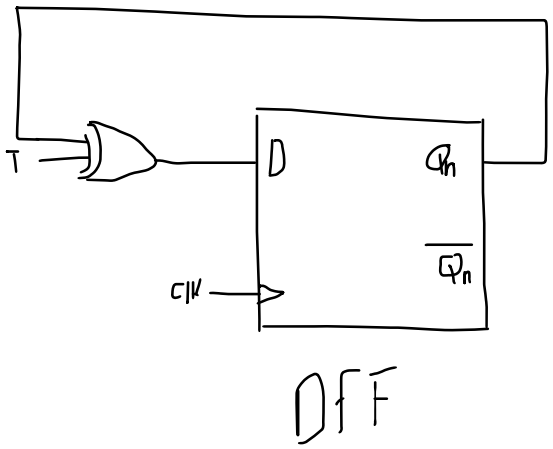
K-MAP

K-MAP




$D = T\,\overline{Q_n} + \overline{T}\,Q_n$

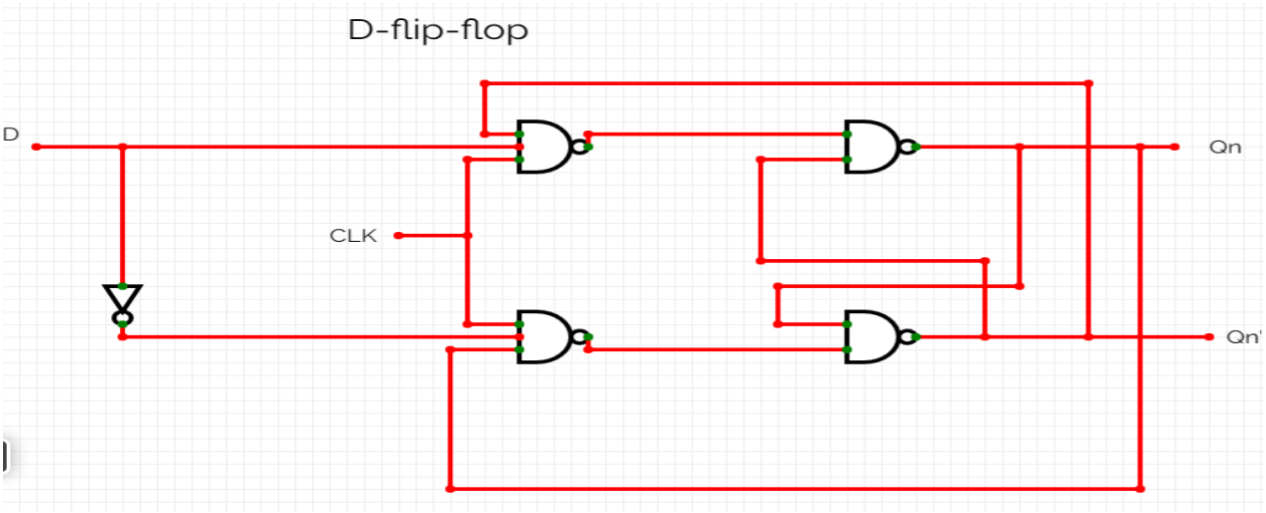
$= T \oplus Q_n$

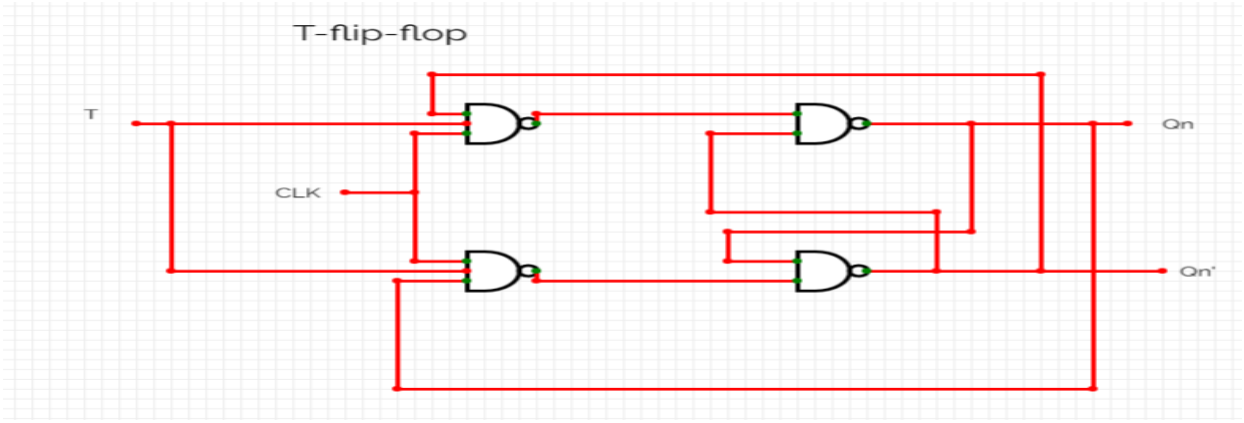


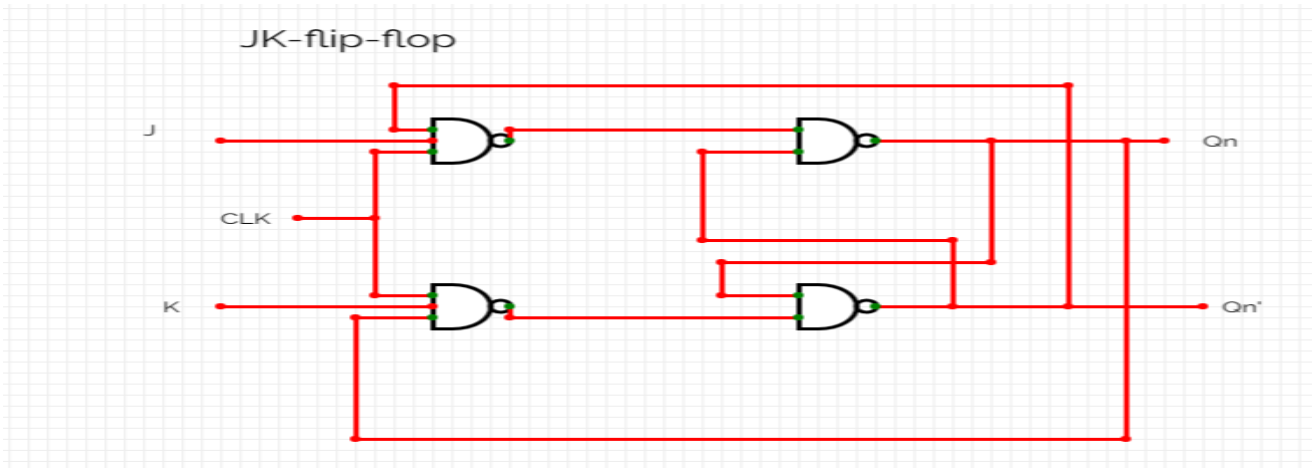

DFF

Problem #6
Compare between D-flip-flop, T-flip-flop, and JK-flip-flop with positive-edge trigger.
a. Gate level for each gate.
b. Characteristic table.
c. Graphical Symbol.
d. Complete the following timing diagram showing the output of each gate based on the given input and the clock

a. Gate level for each gate.



b. Characteristic table.

D-flip-flop

| D | Qn | Qn+1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

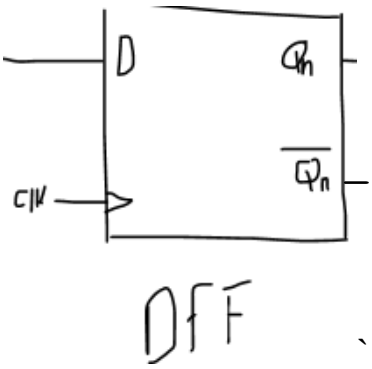
T-flip-flop

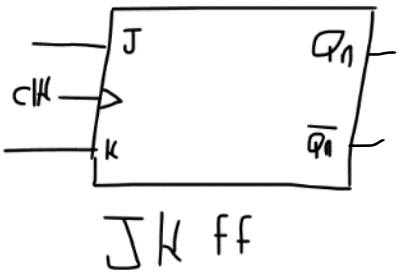
| T | Qn | Qn+1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

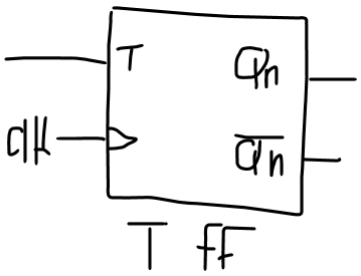
JK-flip-flop

| J | K | Qn | Qn+1 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

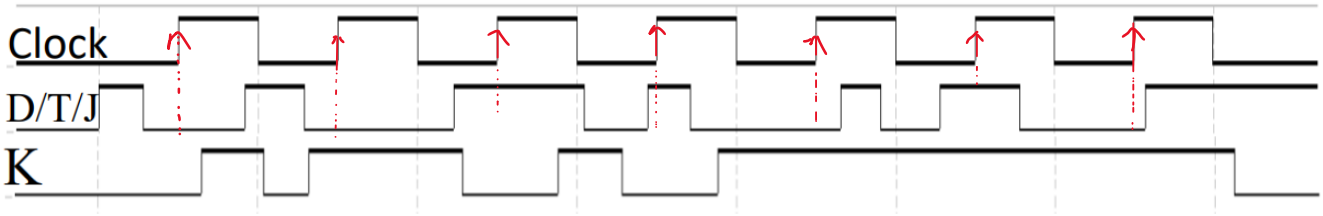
c. Graphical Symbol.

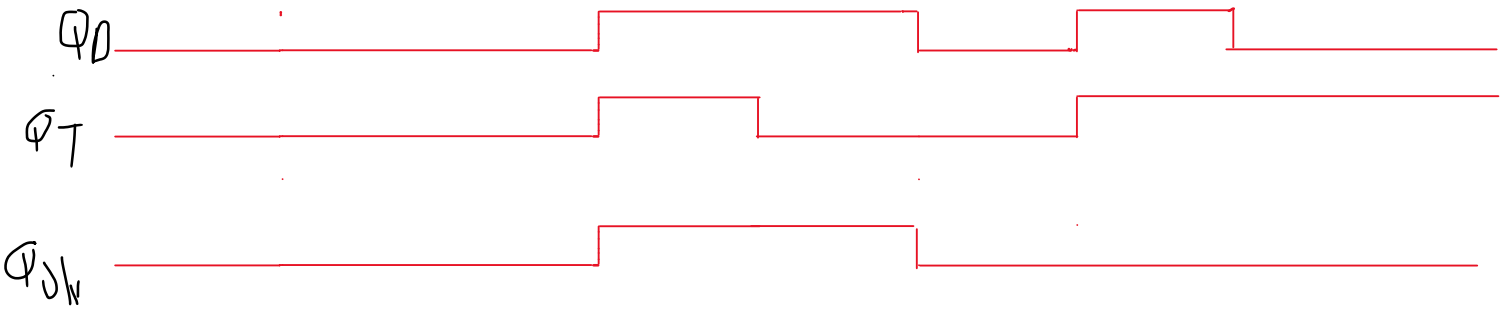


d. Complete the following timing diagram showing the output of each gate based on the given input and the clock



**Problem #7**

Design an equality comparator circuit for 4-bit binary numbers A and B, which represent unsigned binary numbers. The comparator produces an output E. E is set to 1 if A equals B, otherwise 0.

$A = A_3 A_2 A_1 A_0$

$B = B_3 B_2 B_1 B_0$

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

} XNOR Gate

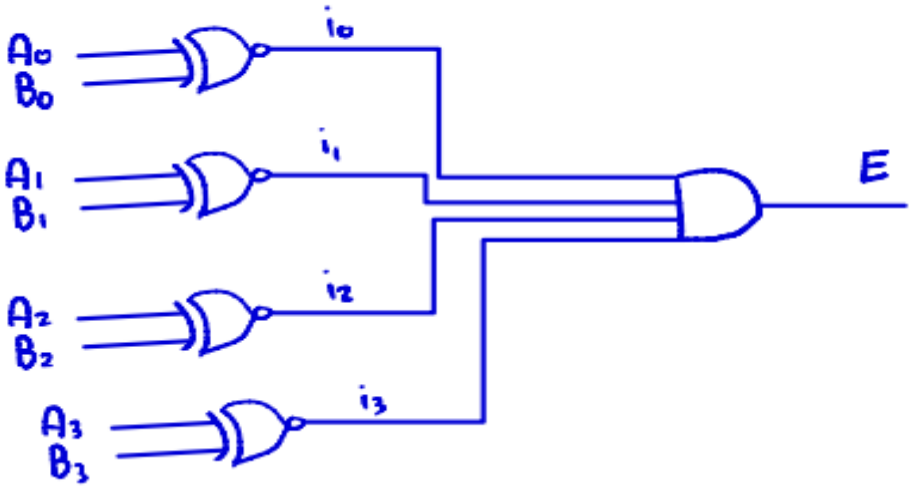
$i_0 = \overline{A_0 \oplus B_0} =$

$i_1 = \overline{A_1 \oplus B_1} =$

$i_2 = \overline{A_2 \oplus B_2} =$

$i_3 = \overline{A_3 \oplus B_3} =$

$\rightarrow A \; Eq \; B = i_0 \cdot i_1 \cdot i_2 \cdot i_3$



**Problem #10**

Create a Verilog code that represents 8-to-1 multiplexer using an if-else statement.

```
module muX   (in,out,s);
input [7:0] in;
input [2:0] s;
output out;

reg out;
Wire [2:0] s;
wire [7:0]in;
always @(s or in)
begin
 If (s==0)
out = in[0];

 else If (s==1)
out = in[1];

 else If (s==2)
out = in[2];

 else If (s==3)
out = in[3];

 else If (s==4)
out = in[4];

 else If (s==5)
out = in[5];

 else If (s==6)
out = in[6];

else (s==7)
out = in[7];
end
endmodule
```