Biasing Transistors (BJT)

I. Introduction

For a transistor to be an amplifier, a correct biasing is required. A correct bias is defined in the Active region of a transistor, which needs two conditions:

$$V_{BE} = forward\ bias$$

$$V_{BC} = reverse\ bias$$

The bias point, then, will determine the following quantities known as the small-signal parameters:

$$Quiescent \rightarrow r_o, r_\pi, and\ g_m$$

In general, one should start transistor analysis with the DC biasing. Then, do the small-signal (AC) analysis, which only deals with the small changes in voltages and currents. Finally, one can compute the input and output resistance of circuit to complete the analysis. Note that DC voltage source is treated as short-circuit (ground) and DC current source is treated as open circuit, for an ideal current source exhibit infinite input resistance. The reason why one can perform DC and AC analysis separately is because the superposition principle can be applied.

Note that there are variations in collector current and the Base-Emitter voltage. If there were no variations, then there wouldn't be amplification.

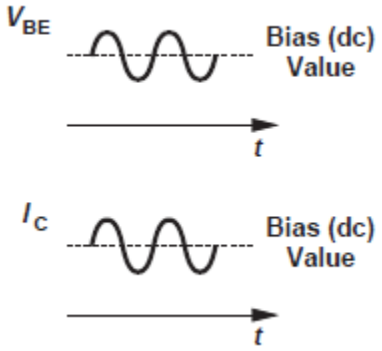


Figure 1.

a. Linearity

Linearity is one key point in transistor amplifier analysis since it defines what "small-signal" means in circuit. One can perform the small-signal analysis only when the biasing points (I_C, V_{BE}, etc) exhibit or experience small changes in them. To expound, non-linear circuit can't be a candidate for amplifier and the small-signal analysis wouldn't work. Non-linearity means

that when small change in voltage (collector-emitter) causes a large change in current (collector). As a rule of thumb, 10% of variation in such change is acceptable and can be thought as “small-change”.

b. Understand the gravity of Biasing quantitatively

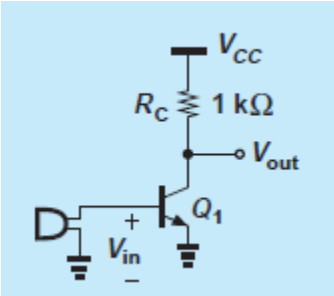


Figure 2. Example Circuit

Let’s suppose one forgot to bias a circuit and use typical values as follow:

$$I_S = 6\times10^{-16}\ A$$

$$V_T = 26\ mV$$

$$V_{in} = 20\ mV$$

The microphone produces $20\ mV$ and since there’s no biasing point:

$$V_{in} = V_{BE} = 20\ mV$$

Now, one can calculate the collector current using the following equation:

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

After some math,

$$I_C = 1.295\times10^{-15}\ A$$

Now, the output voltage:

$$V_{out} = R_C I_C = 1.295\times10^{-12}\ V \cong 0\ V$$

$$g_m = \frac{I_C}{V_T} = 4.98\times10^{-14}\ mho \cong 0\ mho$$

Hence, the circuit produces no transconductance therefore no output. If one tries out with correct bias point ($V_{BE} \approx 700\ mV$), then the result would have become:

$$I_C = 0.295\ mA$$

$$V_{out} = 0.295\ V$$

$$A_v = \frac{V_{out}}{V_{in}} = 14.75$$

c. Biasing and Gain

Once transistor is in the forward-active region, one can select the voltage gain by choosing appropriate collector current.

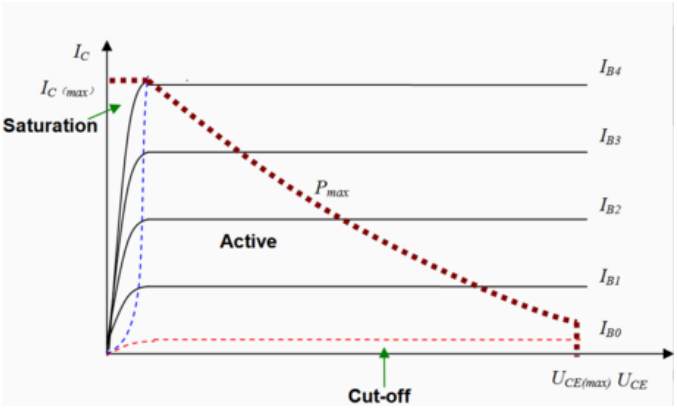


Figure 3.

d. Contents of Biasing

Let's go through all the biasing techniques and then it may become comfortable when biasing transistor. List of biasing techniques:

Simple Biasing
Resistive Divider Biasing
Biasing with Emitter Degeneration
Self-biased Stage
Biasing PNP transistor

Note

"Emitter Degeneration" for stabilizing the bias point
"Resistive Divider" for suppressing the dependency of collector current upon β

i. Simple Biasing

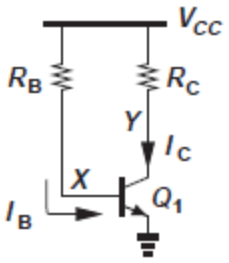


Figure 4. Simple Biasing Circuit

Equations for simple biasing circuit:

$Assume\ V_{BE} = 700{\sim}800\ mV$
$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{I_C}{\beta}$
$V_{CE} = V_{CC} - R_C I_C > V_{BE}$

The condition for collector voltage is greater than the base voltage is necessary for ensuring the forward active region.

In summary, the procedure:

$I_B \rightarrow I_C \rightarrow V_{CE}$

Note that since we used an assumption for the base-emitter voltage, iterations are required. Just keep track of all the collector current until they converge to some number.

ii. Resistive Divider Biasing

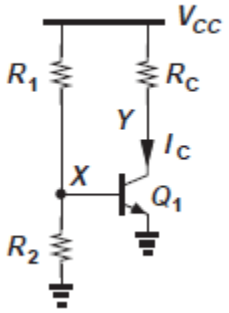


Figure 5.

Equations for Resistive Divider Biasing:

$V_X = \frac{R_2}{R_1 + R_2} V_{CC}$

$$I_C = I_S \exp\left(\frac{V_X}{V_T}\right) \rightarrow independent\ of\ \beta$$

Note that the base current should be negligible in spite of the independency of collector current upon β.

What do we do when the base current is not negligible at the end?

Now, we introduce the Thevenin equivalent circuit technique. If we use Thevenin approach, then we don't have to assume that the base current would be negligible. Note that Thevenin voltage is equal to the open-circuit output voltage.

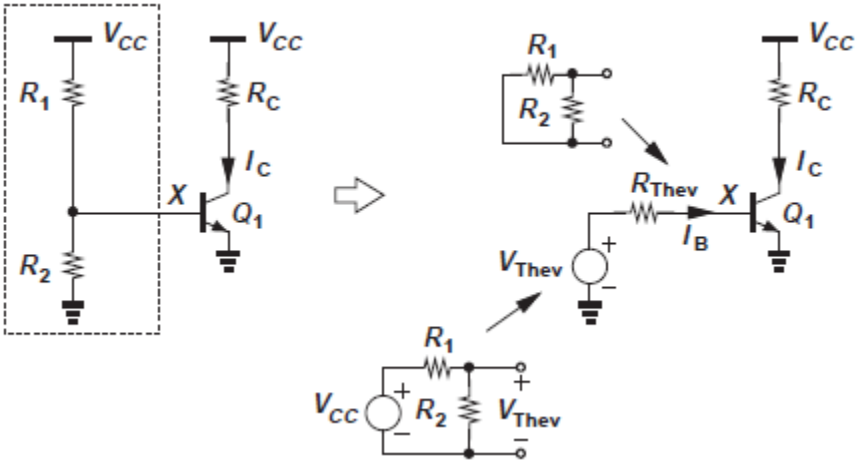


Figure 6.

Equations for Thevenin approach:

$$V_{thev} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$R_{thev} = R_1 || R_2 \rightarrow output\ resistance\ if\ V_{CC} = 0$$

$$V_X = V_{thev} - I_B R_{thev}$$

$$I_C = I_S \exp\left(\frac{V_X}{V_T}\right) \rightarrow I_B\ doesn't\ have\ to\ be\ negligible$$

As before, iterations are required to calculate the bias accurately; however, since the collector current is now in the exponential function, there is huge fluctuation. Hence, we suggest the following form to calculate the base current.

$$I_B = \frac{\left(V_{thev} - V_T \ln\left(\frac{I_C}{I_S}\right)\right)}{R_{thev}}$$

$$I_C = \beta I_B$$

Summary:

Assume $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \rightarrow I_B \rightarrow I_C \rightarrow V_{BE} \rightarrow \cdots$

iii. Emitter Degeneration Biasing

This configuration solves two problems: the sensitivity of β and V_{BE}. R_1 and R_2 are for the sensitivity of β. R_E at the emitter end is for stabilizing the bias point.

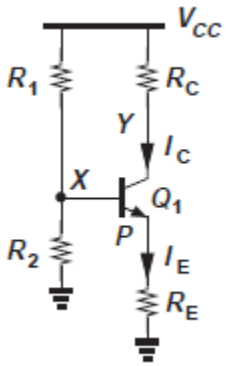


Figure 7. Emitter Degeneration Biasing

Equations for Emitter Degeneration Biasing:

$V_X = \frac{R_2}{R_1 + R_2} V_{CC}$
$V_P = V_X - V_{BE}$
$I_E = \frac{V_P}{R_E} \cong I_C \; if \; \beta \gg 1$

Robust Design Rules:

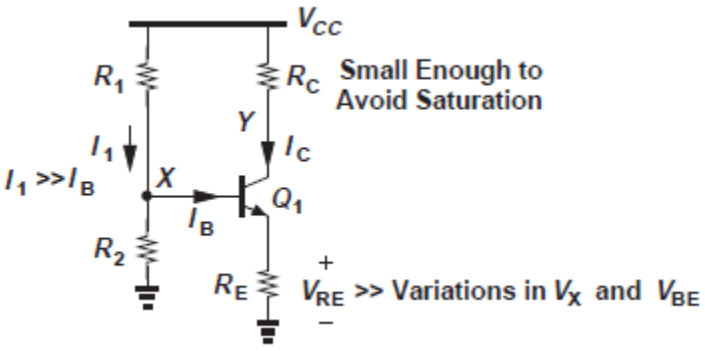


Figure 8. Robust Biasing Circuit Topology

Two rules:

$I_1 \gg I_B$

V_{RE} should be large enough

The first rule check point ensures lower sensitivity to β. The second one is for removing the uncertainty in variations in V_X and V_{BE}.

Design Procedure:

1. Decide I_C, which will determine g_m and r_π
2. Choose $V_{RE} \cong I_C R_E$ $(e.g. 200\ mV)$ based on the expected variations of $R_1, R_2, and\ V_{BE}$
3. Calculate $V_X = V_{BE} + I_C R_E$ where $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$
4. Choose R_1 and R_2 so that $I_1 \gg I_B$
5. For gain, R_C must be selected based on the maximum value that places Q_1 at the edge of saturation.

Considering $V_{CE,sat}$?

Trade-offs of lower sensitivity:

If I_1 is much more larger than (e.g.more than 10 times), then R_1 and R_2 will become small → lower input impedance of circuit.
If we chose very large $V_{RE} \rightarrow V_X$ become very large too $(V_X = V_{BE} + V_{RE})$ →limit the minimum value of V_C to avoid saturation.

iv. Self-Biased Stage

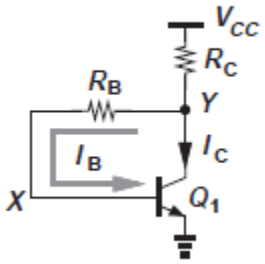


Figure 9. Self-Biased Stage Circuit

This topology is always in forward active region regardless of circuit parameters because $V_B < V_C$; $V_X = V_Y - I_B R_B$. This means even if we indefinitely increase R_C, Q_1 would still be remained the active region.

Equations for self-biased stage:

$V_Y = V_{CC} - R_C I_C = R_B I_B + V_{BE}$

$I_C = \frac{I_B}{\beta}$
$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}}$
$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$

Summary:

Guess V_{BE} → Compute I_C → then iterate until converges to some number of V_{BE}

Two important guidelines for self-biased stage:

$V_{CC} - V_{BE} \gg the\ uncertainty\ in\ V_{BE}$
$R_C \gg \frac{R_B}{\beta}$

Design Procedure of self-biased stage:

$e.g. Choose\ R_C = \frac{10R_B}{\beta}$
$hence\ I_C = \frac{V_{CC} - V_{BE}}{1.1R_C}$

v. Summary of NPN biasing

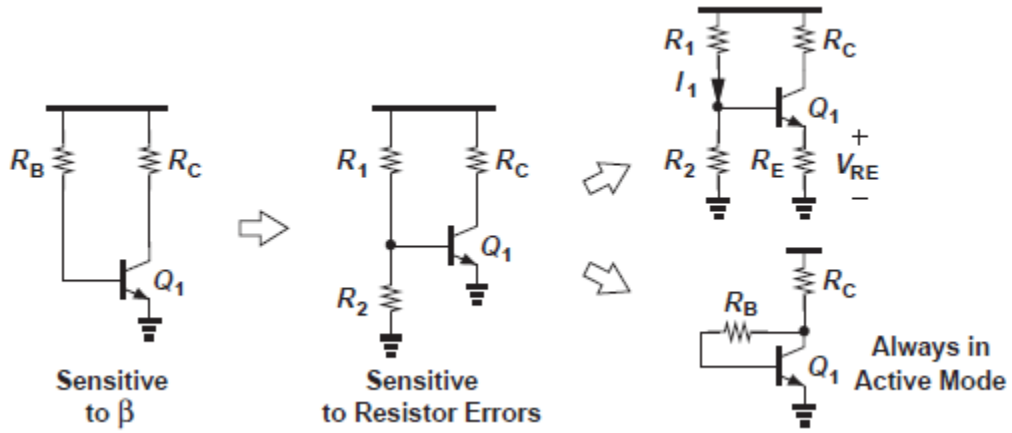
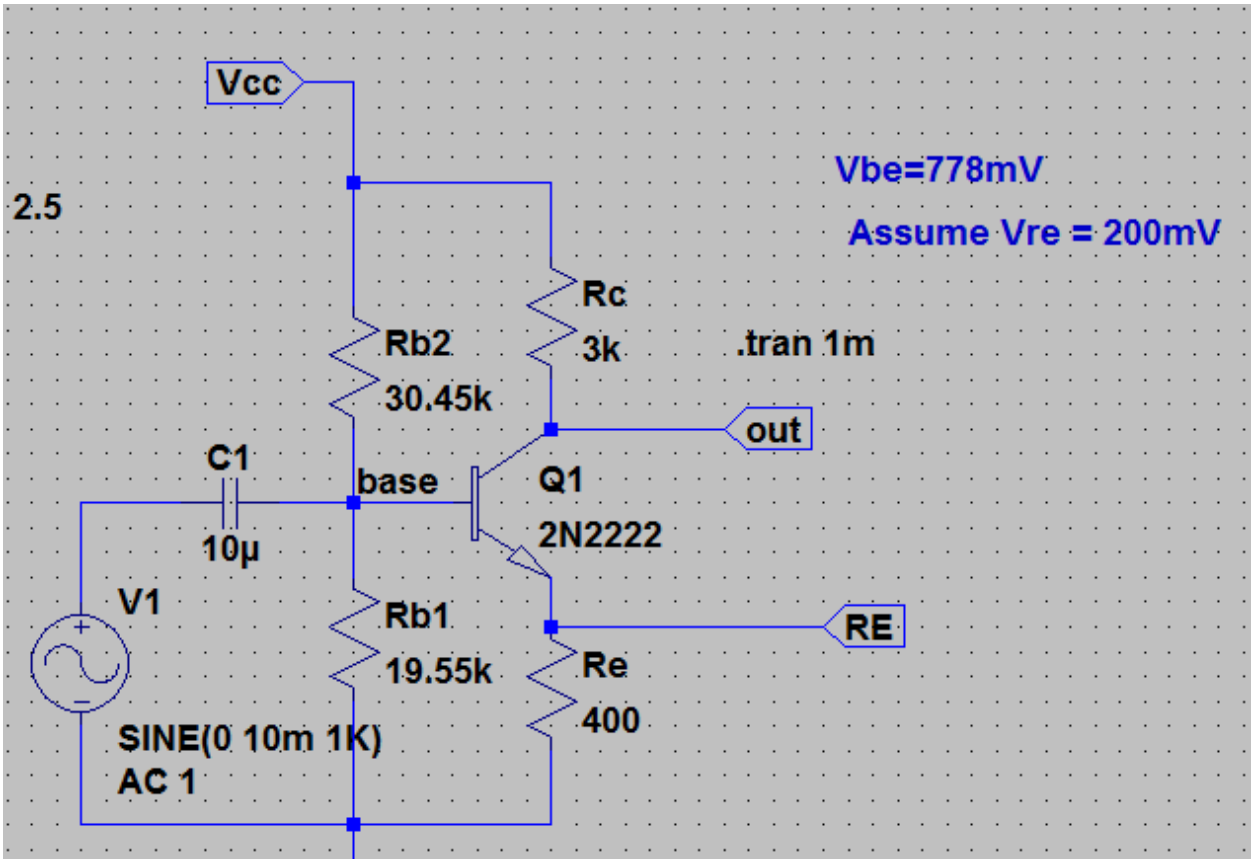


Figure 10.

vi. Biasing of PNP transistor

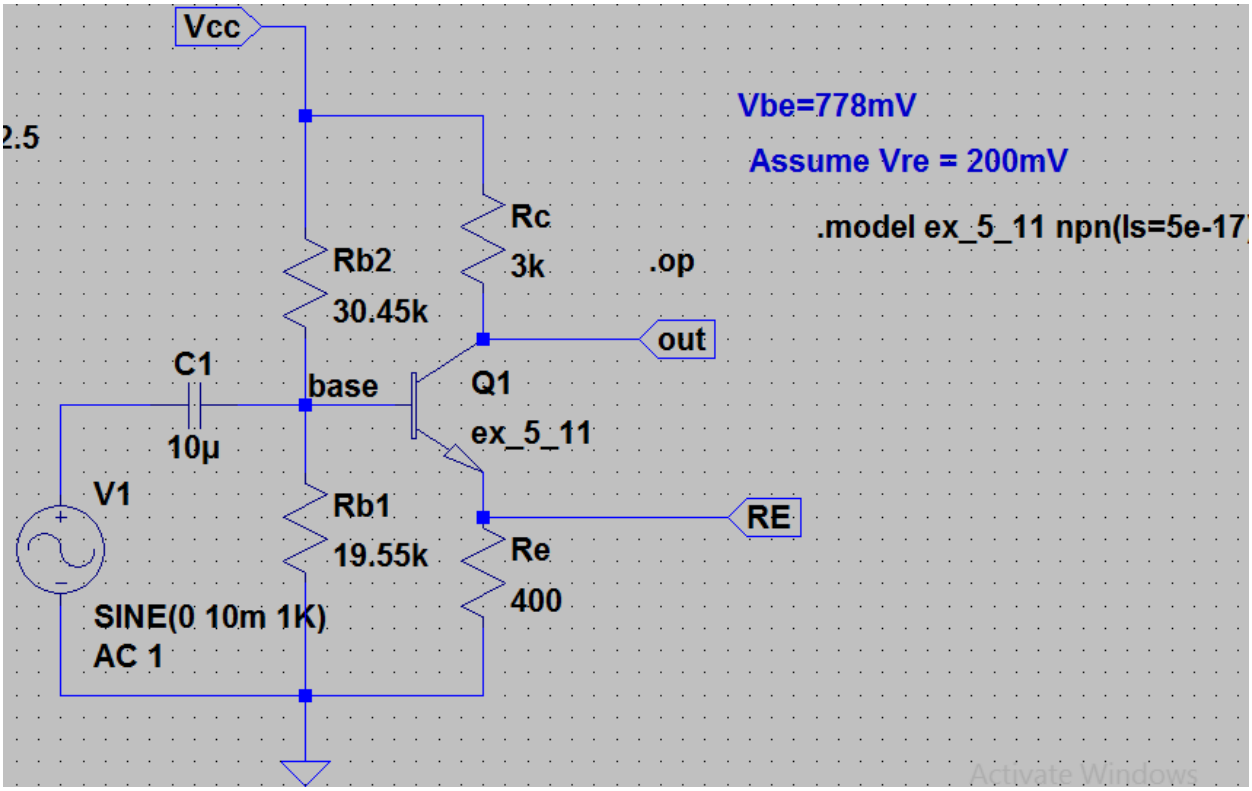
II. Examples

a. Example 5.11



Simulated Bias Points: (wrong model version…….. Q2N2222 has $I_S = 1\times10^{-14}A$)

V_{re}	0.279 V
V_{out}	0.422 V
V_{base}	0.925 V
I_C	0.692 mA
I_{sup}	0.744 mA
V_{BE}	646 mV
V_{BC}	502 mV
V_{CE}	144 mV
g_m	26.7 $mmho$



Figure

Name:	q1
Model:	ex_5_11
Ib:	4.00e-06
Ic:	4.00e-04
Vbe:	7.68e-01
Vbc:	-3.71e-01
Vce:	1.14e+00
BetaDC:	1.00e+02
Gm:	1.55e-02
Rpi:	6.47e+03
Rx:	0.00e+00
Ro:	8.78e+20
Cbe:	0.00e+00
Cbc:	0.00e+00
Cjs:	0.00e+00
BetaAC:	1.00e+02
Cbx:	0.00e+00
Ft:	0.00e+00

V(re):	0.161474	voltage
V(vcc):	2.5	voltage
V(out):	1.30094	voltage
V(base):	0.929913	voltage
V(n001):	0	voltage
Ic(Q1):	0.000399688	device_current
Ib(Q1):	3.99688e-006	device_current
Ie(Q1):	-0.000403685	device_current
I(C1):	9.29913e-018	device_current
I(Rb1):	4.75659e-005	device_current
I(Rb2):	5.15628e-005	device_current
I(Rc):	0.000399688	device_current
I(Re):	0.000403685	device_current
I(Vcc):	-0.00045125	device_current
I(V1):	9.29913e-018	device_current

Figure. DC Operating Points

Calculations:

$$V_{BE} = 778\ mV\ and\ assume\ V_{RE} = 200\ mV$$

$$I_C = 0.5\ mA\ (given)$$

$$I_B = \frac{I_C}{\beta} = 5\ \mu A\ (\because \beta = 100)$$

$$I_1 \gg I_B\ (I_1\ is\ the\ current\ flowing\ through\ R_{B2})$$

$$\frac{V_{CC}}{R_{B1} + R_{B2}} \gg I_B$$

From KVL:

$$V_B = \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC} = V_{BE} + I_E R_E = 978\ mV$$

Let's take 10 times of I_1 and say it is equivalently saying much greater than I_B, then we obtain:

$$\frac{V_{CC}}{10 I_B} = R_{B1} + R_{B2} = 50kohm$$

Hence, we obtain one of the resistance:

$$R_{B2} = \frac{(978\ mV)}{V_{CC}} * 50kohm = 19.56kohm$$

The other resistance can be easily obtained and this value is:

$$R_{B1} = 50k - 19.56k = 30.44kohm$$

Now, collector resistance can be found from the biasing requirement:

$$V_C > V_B$$

$$V_{CC} - I_C R_C > V_B$$

Hence,

$$R_C < 3043.45\ ohm$$

The output voltage can be determined after determining the collector resistance:

$$let\ R_C = 3kohm$$

$$V_{out} = V_{CC} - R_C I_C = 2.5 - (3k)(0.5mA) = 1.0\ V$$

Note that circuit designers should also think about the positive and negative swings. For symmetry purpose, suggested output DC voltage level should be $V_{out} \cong [V_{CC} - 0V(GND)]/2$ so that AC output voltage can oscillate without clipping.

For the gain:

$$A_v = -\frac{R_C || R_L}{\frac{1}{g_m} + R_E + \frac{R_{Thev}}{\beta + 1}} \cdot \frac{R_1 || R_2}{R_1 || R_2 + R_S}, \quad (5.251)$$

$$A_{v,calculated} = -g_m R_C = -(1.55 \times 10^{-2})(3000) = -5.26$$

However, the plot shows that:

$$A_{v,simulated} = -6.4$$

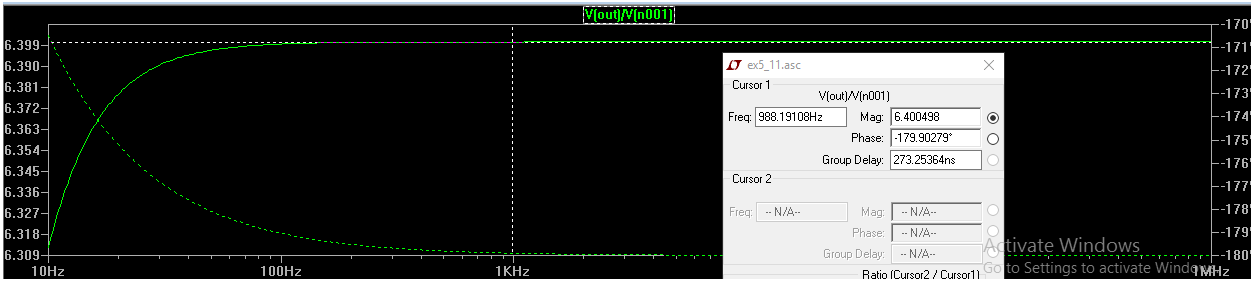


Figure. Gain plot of example 5.11

Input and Output Graphs:

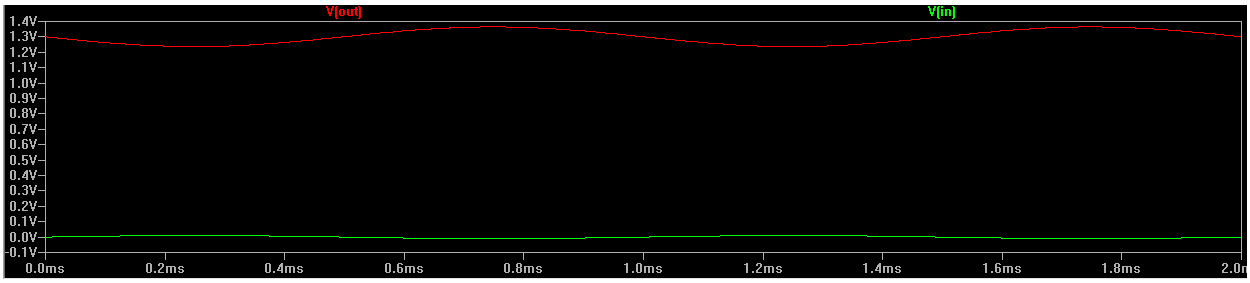


Figure. Input and Output

Notice that the output contains the DC level ($\cong 1.3V$) and AC part (which is the amplified input level with the gain).

Now, let's examine the case where collector resistance value is too high.

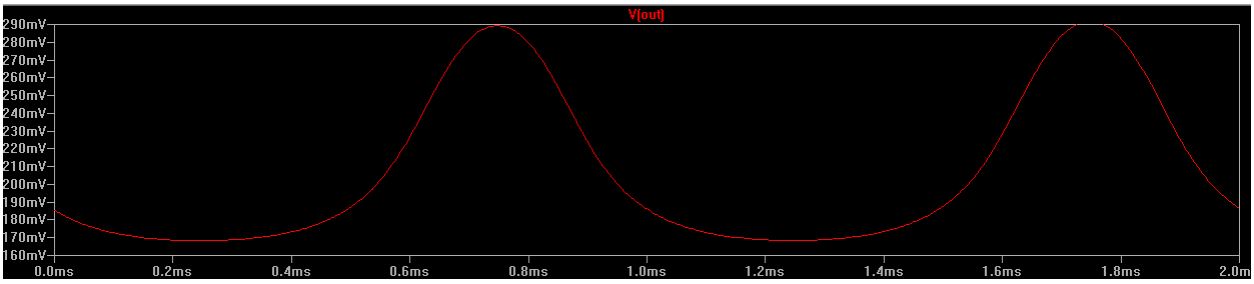


Figure. Output Voltage when $R_C = 10kohm$

Notice that output voltage is no longer linearly related to the input signal. From the basic amplifier analysis, we know that amplification only possible in the forward region of operation and now we checked it is true. If we calculate and see if Q1 is correctly biased or not:

$$V_C = 2.5 - (0.5mA)(10kohm) = -2.5\,V$$

Hence,

$$V_B > V_C$$

Let's take a look at the below chart and we can tell Q1 has entered the saturation region.

Applied voltages	B-E junction bias (NPN)	B-C junction bias (NPN)	Mode (NPN)
E < B < C	Forward	Reverse	Forward-active
E < B > C	Forward	Forward	Saturation
E > B < C	Reverse	Reverse	Cut-off
E > B > C	Reverse	Forward	Reverse-active
Applied voltages	**B-E junction bias (PNP)**	**B-C junction bias (PNP)**	**Mode (PNP)**
E < B < C	Reverse	Forward	Reverse-active
E < B > C	Reverse	Reverse	Cut-off
E > B < C	Forward	Forward	Saturation
E > B > C	Forward	Reverse	Forward-active

Figure. Modes of Operations of BJT

However, there's so called "$V_{CE,sat}$" which allows higher value for collector resistance. This voltage is usually up to $400\ mV$ in low-voltage application.

Hence, modified equation yields:

$$V_C \approx V_B - 400mV$$

Re-calculated the maximum value of the collector resistance with the saturation voltage:

$$R_C < 3843.45\ ohm$$

III. References

[1] Fundamentals of Microelectronics, Behzad and Razavi, 2nd Edition