Oscillators

I. Candidates

TABLE 13.1 Summary of various oscillator topologies and their applications.

		LC Oscillators				
Oscillator Topology	Ring Oscillator	Cross-Coupled Oscillator	Colpitts Oscillator	Phase Shift Oscillator	Wien-Bridge Oscillator	Crystal Oscillator
Implementation	Integrated	Integrated	Discrete or Integrated	Discrete	Discrete	Discrete or Integrated
Typical Frequency Range	Up to Several Gigahertz	Up to Hundreds of Gigahertz	Up to Tens of Gigahertz	Up to a Few Megahertz	Up to a Few Megahertz	Up to About 100 MHz
Application	Microprocessors and Memories	Wireless Transceivers	Stand-Alone oscillators	Prototype Design	Prototype Design	Precise Reference

Figure

Note: Less difficulties for ring oscillator design but LC oscillators are faster and contain less noises although the book doesn't really go through the noise analysis of Oscillator. Unfortunately, LC oscillators are harder to design.

II. Actual Trials

From the reference [1], an LC oscillator follows the model:

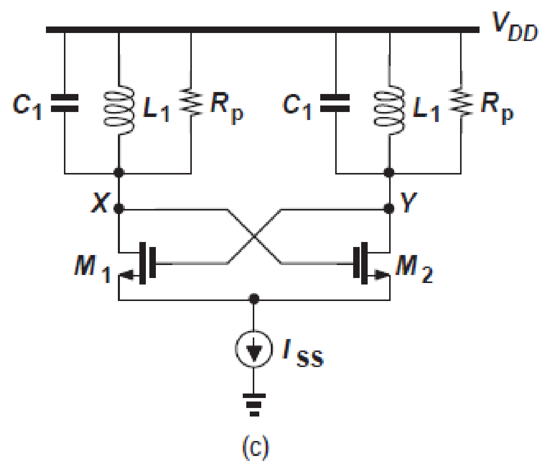

Figure. Cross-coupled Oscillator

My trial model follows the same exact topology but with actual parameters:

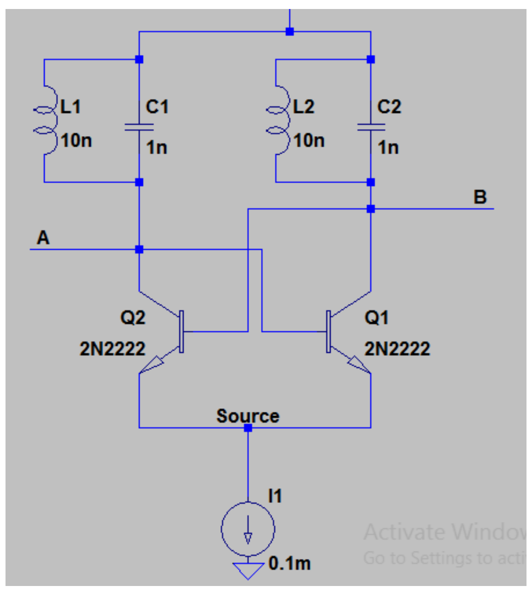

Figure. Intended Oscillating frequency 50MHz

Inductance and Capacitance were found from the following equation:

$$\omega = \frac{1}{\sqrt{LC}}$$

To determine the inductance, first I set the capacitance as $C = 1\ nF$

The inductors contain parallel resistor, which is 10 $k\Omega$ in this design. From the START-UP condition, this parallel resistance should be greater than 520 Ω.

However, DC operating point showed me that this circuit has never been biased correctly. These points were based on:

$$I_{SS} = 0.1\ mA$$

V_{CC}	$5\ V$
V_{source}	$4.422\ V$
$V_{BE1} = V_{BE2} = V_{CE}$	$578\ mV$
V_{BC}	$0\ V$
$I_{B1} = I_{B2}$	$0.249\ \mu A$
$I_{C1} = I_{C2}$	$49.8\ \mu A$
g_m	$1.93\ m\mho$

Highlighted items should be carefully examined.

III. Theory

a. Ring Oscillator

Most microprocessors and memories incorporate CMOS Ring Oscillators. It contains a few stages in a ring. Let's examine CS stage with negative feedback and see if it oscillates.

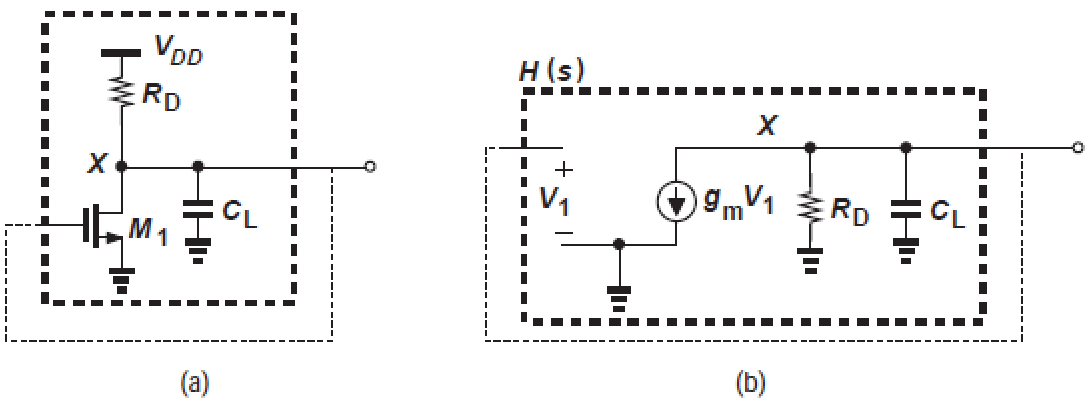

Figure.

Are the ***two Barkhausen's criteria*** met?

$\|H(j\omega)\| = 1 \rightarrow possible$
$\measuredangle\|H(j\omega)\| = 180° \rightarrow impossible\ (single\ pole\ provides\ maximum - 90°)$

The pole at Node X (open loop pole):

$\omega_{p,X} = -\dfrac{1}{C_L R_D}$
$\omega_{p,X}\|_{max} = -90°\ (at\ \omega = \infty)$

Now, let's examine a circuit with two CS stages cascaded:

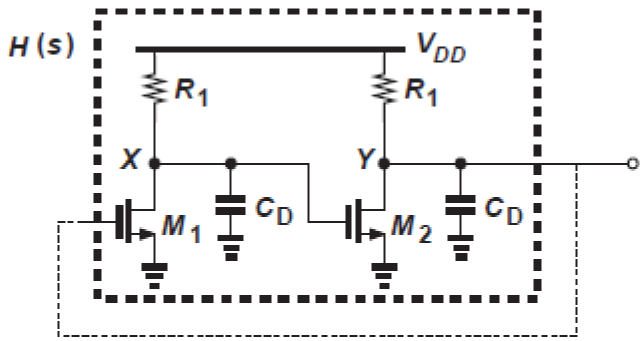

Figure.

The phase shift of the two CS stages provide maximum 180° and yet the circuit would not oscillate since the gain is zero at $\omega = \infty$ and the 180° can only be achieved at $\omega = \infty$. This brings an important point, that is there should be at least 3 CS cascaded stage needed to oscillate.

Three-stage Ring Oscillator:

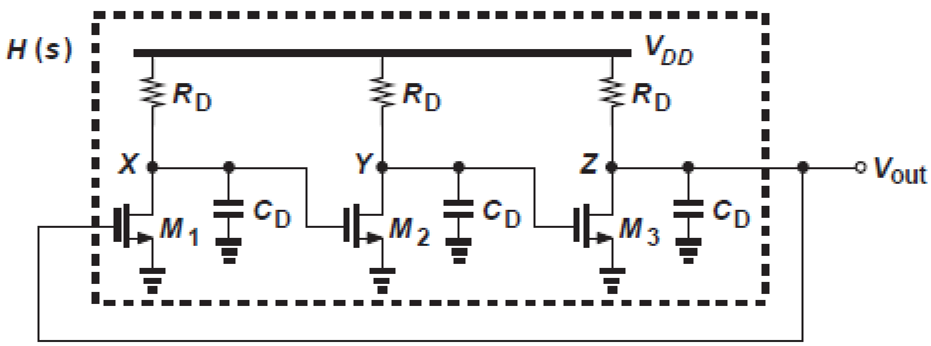

Figure. Simple 3 stage Ring Oscillator

Now, each pole should only provide 60° (or $-60°$).

Equations:

$\omega_1 = \frac{\sqrt{3}}{R_D C_D}$
$H(j\omega)\|_{each\ stage} = -\frac{g_m R_D}{1 + R_D C_D s}$
Barkhausen's criteria: $\left(\frac{g_m R_D}{\sqrt{1 + R_D^2 C_D^2 \omega_1^2}}\right)^3 = 1$ $\therefore\ gain\ for\ each\ stage \geq 2\ at\ low\ frequency$

i. Example – 1MHz Ring Oscillator Circuit

Before calculating the capacitance for the target frequency, we need to set the transistor parameters first. Since I do not know how they are related, I'm just going to use random MOSFET parameters.

$$k_n = \mu_n C_{ox} = 500\mu$$
$$\frac{W}{L} = \frac{100\mu}{10\mu}$$
$$V_{TH} = 1.4\,V$$
$$\lambda = 0.01$$
$$I_D = 1mA$$

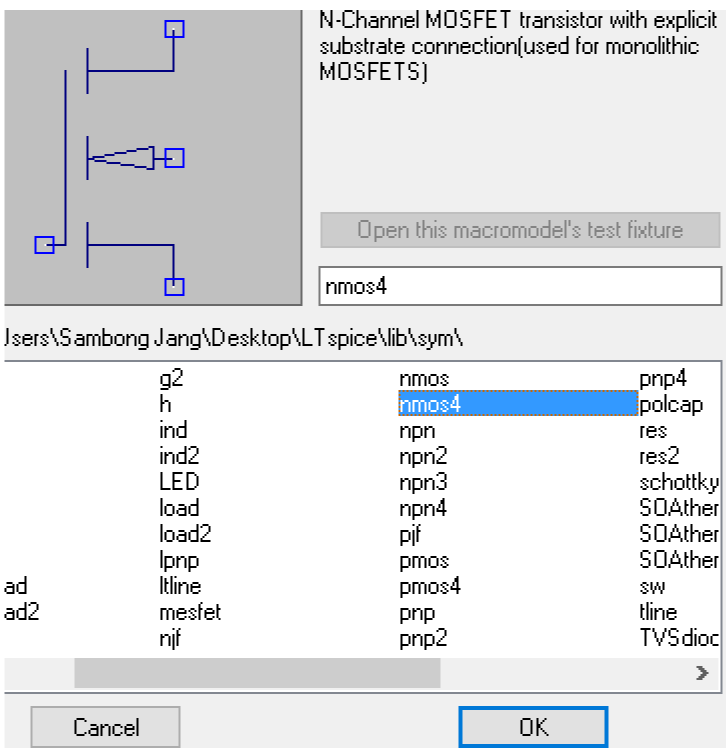

Figure. NMOS model

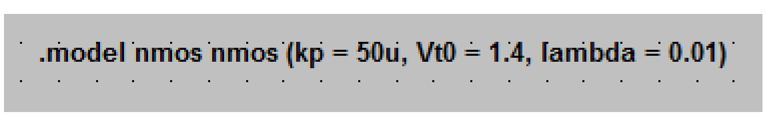

Figure. LTSpice Directive for NMOS model

Let's calculate the rest of dependent variables.

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D} = 1\ mmho$$

Since we know that the gain for each stage should be at least 2, here we let it equal to 3.

$$R_D = \frac{|A_{v,each\ stage}|}{gm} = 3\ kohm$$

We want the circuit to oscillate at $f_1 = 1MHz$

$$\omega_1 = 2\pi(f1) = \frac{\sqrt{3}}{R_D C_D}$$

$$C_D = 91.89\ pF$$

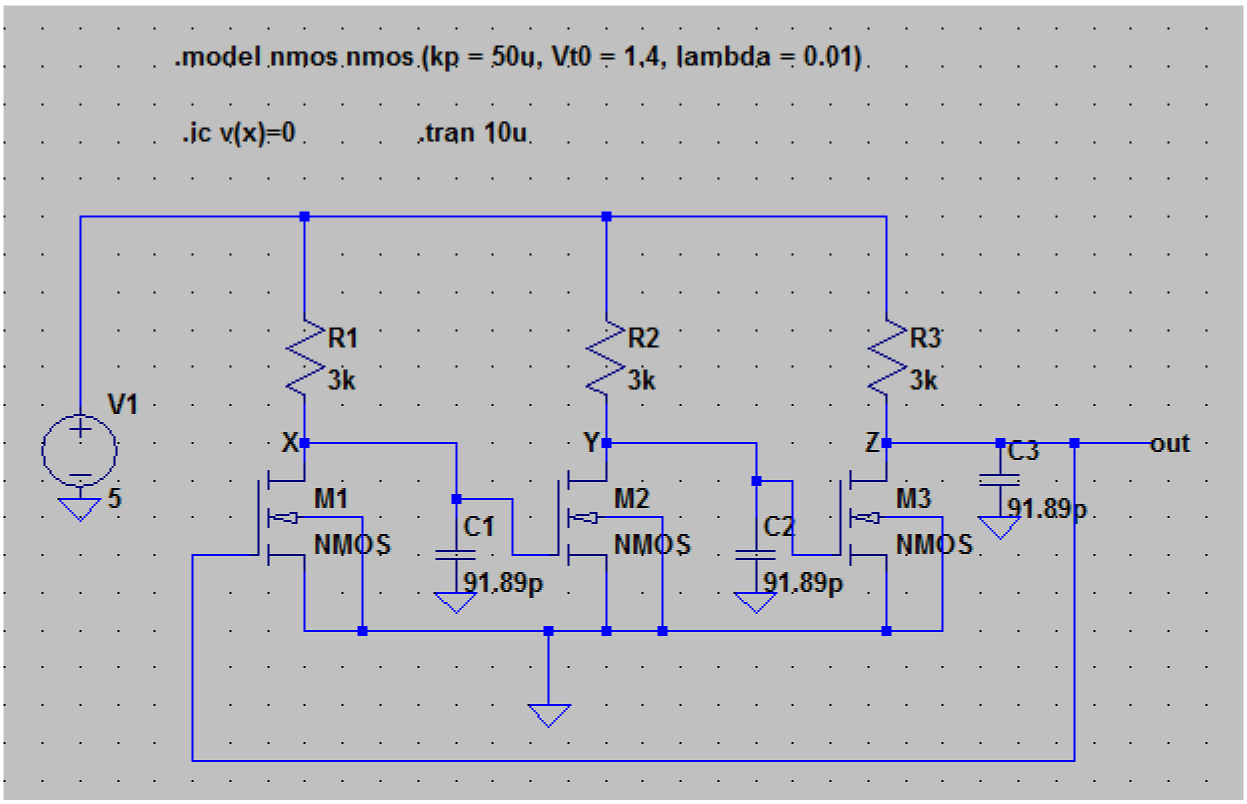

Figure. Ring Oscillator Circuit

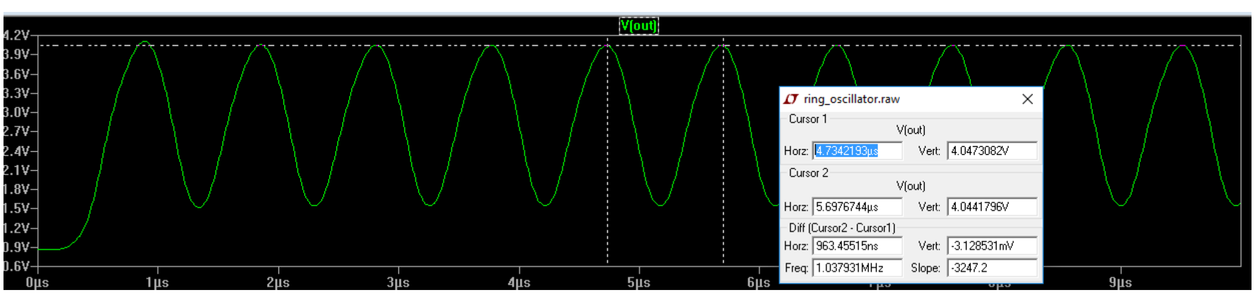

Figure. Transient Response

From the transient response plot, we can conclude that the oscillator provides

$$f_{simulated} = 1.038\ MHz$$

Hence, the circuit behaves in the way I wanted. However, other parameters showed some discrepancies between the simulated and the calculated.

--- MOSFET Transistors ---

Name:	m3	m2	m1
Model:	nmos	nmos	nmos
Id:	1.38e-03	1.00e-11	7.96e-18
Vgs:	5.00e+00	3.33e-06	8.63e-01
Vds:	8.63e-01	5.00e+00	3.33e-06
Vbs:	0.00e+00	0.00e+00	0.00e+00
Vth:	1.40e+00	1.40e+00	1.40e+00
Vdsat:	3.60e+00	0.00e+00	0.00e+00
Gm:	4.35e-04	0.00e+00	0.00e+00
Gds:	1.39e-03	0.00e+00	0.00e+00
Gmb:	0.00e+00	0.00e+00	0.00e+00
Cbd:	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00
Cgsov:	0.00e+00	0.00e+00	0.00e+00
Cgdov:	0.00e+00	0.00e+00	0.00e+00
Cgbov:	0.00e+00	0.00e+00	0.00e+00
Cgs:	0.00e+00	0.00e+00	0.00e+00
Cgd:	0.00e+00	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00	0.00e+00

Figure. .OP – The DC points and other parameters

Calculated $g_{m,calculated} = 1\ mmho$ but the simulation result for M1 MOSDEFT $g_{m,simulation} = 0.435\ mmho$. In addition, there are no other transconductance shown in the DC operating result, which seems peculiar. I should come up with an answer for this later.

Initial Condition for the circuit?

Note that in the circuit, I inserted a spice directive "**.ic v(x)=0**". The textbook describes the reason behind this but in short, this directive would behave as "virtual noise" that what real circuit would have gone through. If the circuit is run without this directive, there would be no oscillation.

IV. References

[1] Fundamentals of Microelectronics, Behzad and Razavi, 2^{nd} Edition