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DATE: 7/12/2020

ELECTRONIC SYSTEMS ENGINEERING
FACULTY OF ENGINEERING and APPLIED SCIENCE

UNIVERSITY OF REGINA

ENEL 383 PROJECT REPORT

OBJECTIVES:

The fundamental objective is to design, test and document a latching control system that provides a start and stop output, based on the presence of 1 of 2 audio frequency tones. The start and stop outputs are indicated by a start (Green LED) and a stop (Red LED) indicator. When the start tone is applied, the start indicator will come on, and remain on, until the stop tone is applied. If neither tone is applied, then the indicators retain their previous state.

The base system is powered from +/- 5V, and the tone amplitude for each tone is 2Vp-p.

EQUIPMENTS:

- Analog Discovery 2 with WAVEFORMS Software
- Breadboard
- OP484FPZ Operational Amplifier
- ADTL082 Operational Amplifier
- 2N3904 Bipolar Junction Transistor
- LEDs (Red and Green)
- NE556 Dual Timer
- Resistors as required
- Capacitors as required
- Digital Multimeter
- 1N914 Diodes
- Jumper Wires

PROBLEM DEFINITION:

1. *Objectives Clarification*
    - Implement a second order active high pass filter with a cutoff frequency to eliminate undesired frequencies and allow desired frequencies.
    - Implement a second order active low pass filter with a cutoff frequency to eliminate undesired frequencies and allow desired frequencies.
    - Implement an inverting amplifier to invert the output voltage from the low pass filter. This circuit should have a gain of -1x.
    - Rectifiers should be implemented in this design to convert two-directional AC voltages into single directional DC voltages and the capacitors should be implemented after the rectifier circuits to reduce the ripple voltages.

- Implement a summation amplifier with a DC offset to combine and level shift (centering) the output voltages of the active filters.
- Implement a Schmitt Trigger to provide two different threshold voltage levels and avoid errors from noisy input voltages.
- Implement an adequate switching interface to turn LEDs ON at their required frequencies.

2. *Objectives Metrics*
    - Supply voltage: +/- 5 V
    - Input voltage: 2 V_{P-P}
    - Start frequency: 1.54 kHz (second order active high pass filter)
    - Stop frequency: 2.3 kHz (second order active low pass filter)

3. *Constraints*
    - Designs and calculations should have a 5% tolerance
    - Must work with power ratings of the components used in the circuit
    - Remote learning

CONCEPTUAL DESIGN:

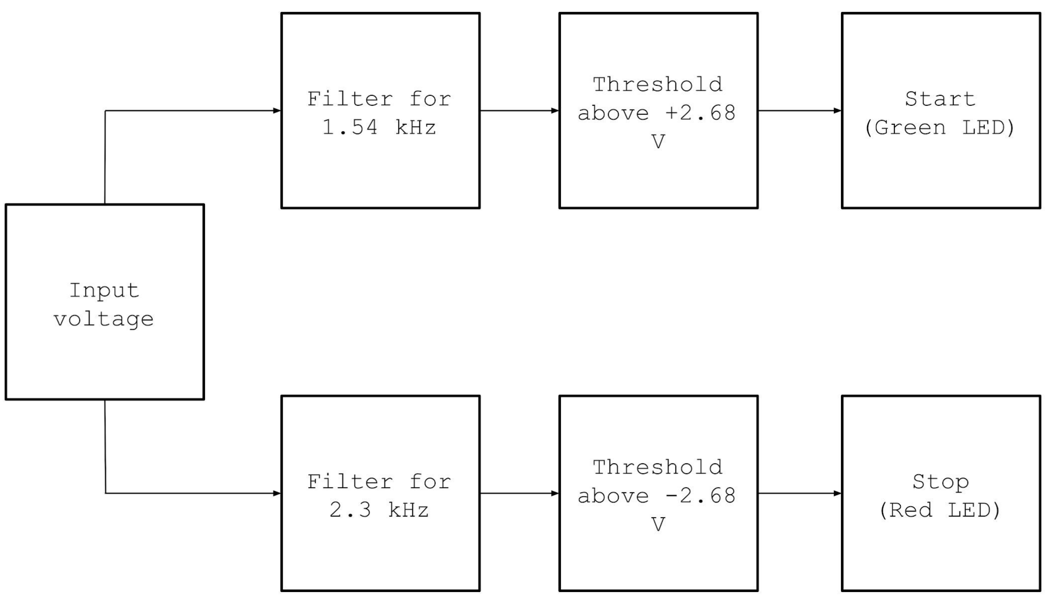

Figure 1: System design map

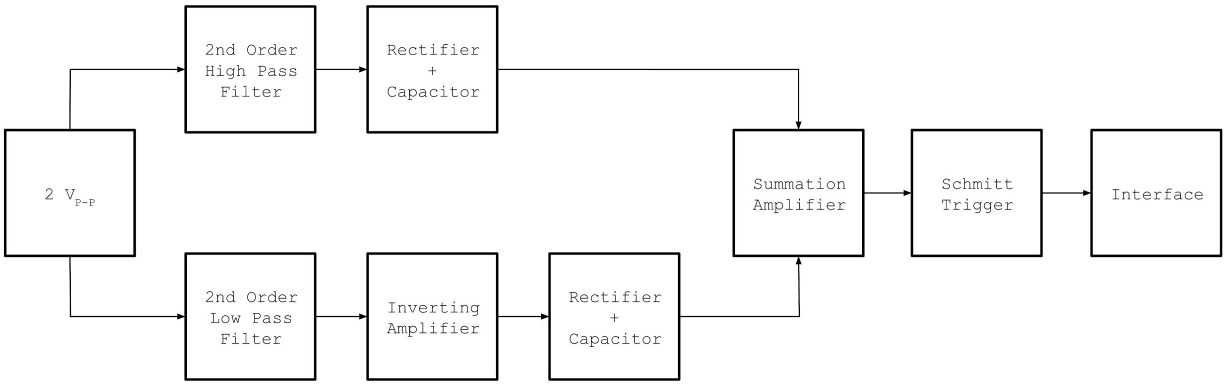

Figure 2: System block diagram

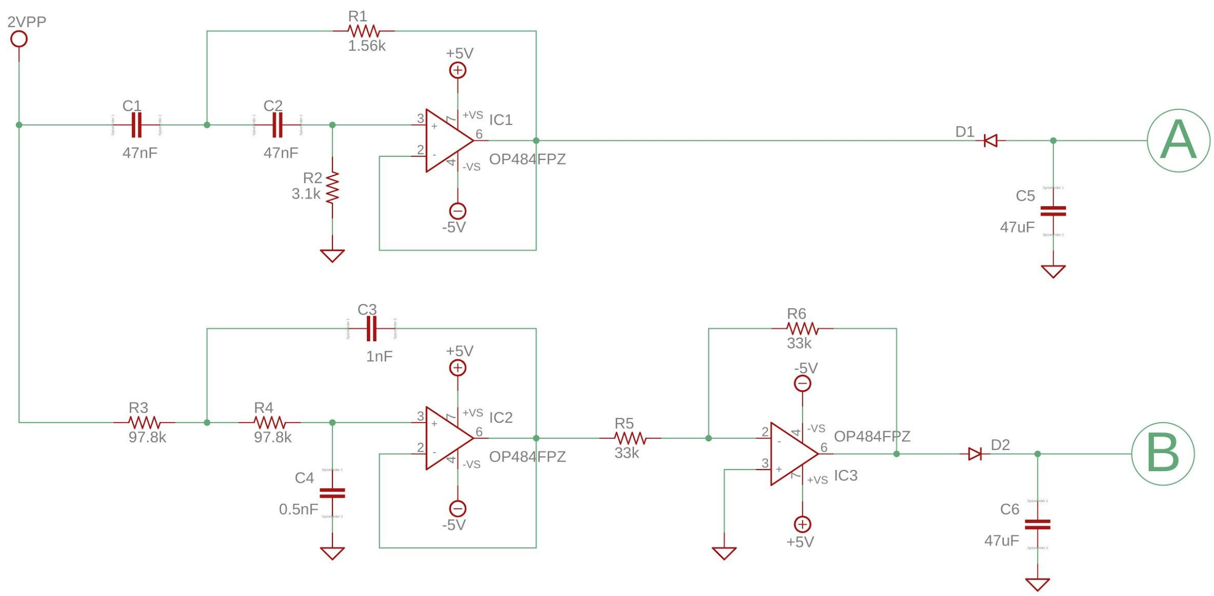

Figure 3: System design schematic (part 1)

- **Second Order Active High Pass Filter**

  $Q = 0.7071$

  $f_C = 1.54$ kHz

  $C = C_1 = C_2$

  Let $C = 0.047$ µF

  $R_1 = 1 / (4 * Q * \pi * f * C) = 1 / (4 * 0.7071 * \pi * 1.54 \text{ kHz} * 0.047 \text{ µF}) = 1555\ \Omega$

  $R_2 = (2 * Q) / (2 * \pi * f * C) = (2 * 0.7071) / (2 * \pi * 1.54 \text{ kHz} * 0.047 \text{ µF}) = 3110\ \Omega$

  By connecting multiple resistors in series, I derived and recorded the following values:

$R_1 = 1.6\ k\Omega$

$R_2 = 3.1\ k\Omega$

$f_C = 1.64\ kHz$

Q = 0.7067

Passband gain = 0 dB

Cutoff gain = -3.02 dB

Roll-off rate = -39.8 dB/dec

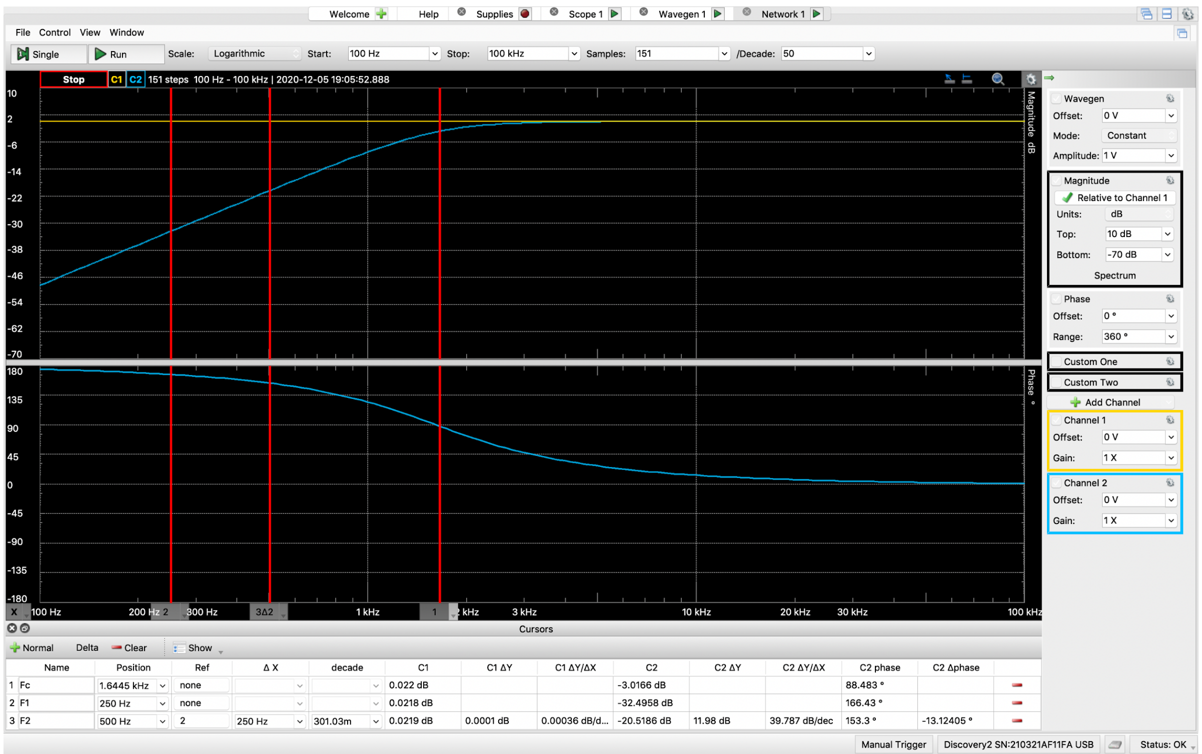

Figure 4: Second order active high pass filter network

- **Second Order Low Pass Filter**

  Q = 0.7071

  F = 2.3 kHz

  $R = R_3 = R_4$

  Let $C_3 = 0.001\ \mu F$

  $C_3 = (2 * Q) / (2 * \pi * f * R)$

  Therefore, $R = (2 * Q) / (2 * \pi * f * C_3) = (2 * 0.7071) / (2 * \pi * 2.3\ kHz * 0.001\ \mu F) = 97860\ \Omega$

  $C_4 = 1 / (4 * Q * \pi * f * R) = 1 / (4 * 0.7071 * \pi * 2.3\ kHz * 97860\ \Omega) = 0.5\ nF$

  By connecting multiple resistors and capacitors in series, I derived and recorded the following values:

$R = 97.8\ k\Omega$

$C_4 = 0.5\ nF$

$f_C = 2.29\ kHz$

$Q = 0.7071$

Passband gain = 0 dB

Cutoff gain = -3.04 dB

Roll-off rate = -39.9 dB/dec

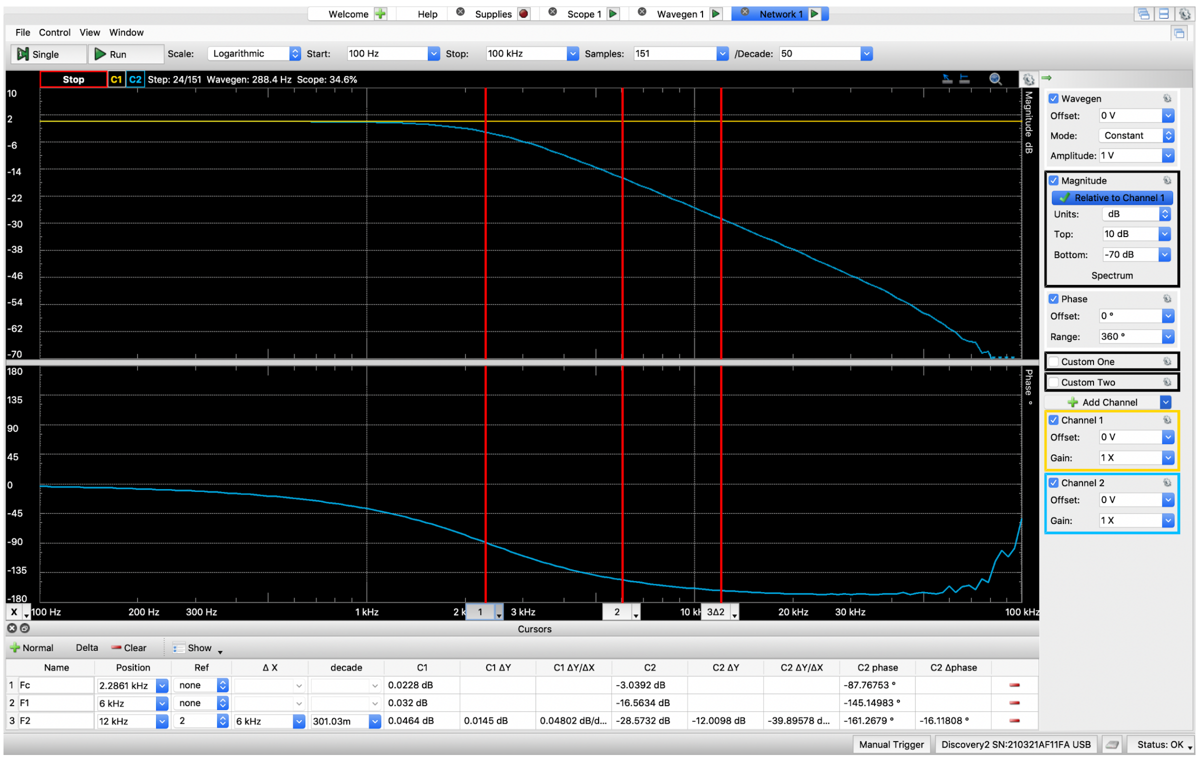

Figure 5: Second order active low pass filter network

- **Inverting Amplifier**

  $A = -(R_6 / R_5)$

  Let $R_5 = 33\ k\Omega$

  $-1 = -(R_6 / 33\ k\Omega)$

  Therefore, $R_6 = 33\ k\Omega$

- **Rectifiers and Capacitors**

  Selected diode: 1N914

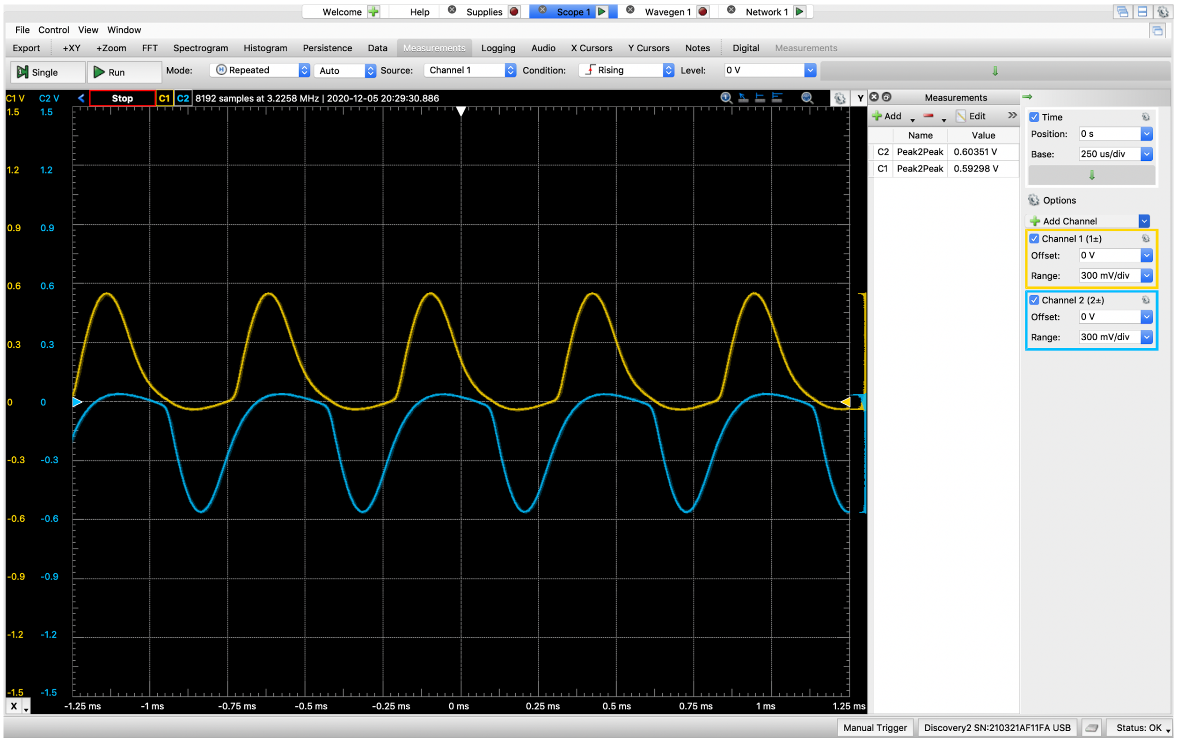

Figure 6: Filters output with rectifier

Selected capacitors: 47 µF capacitors

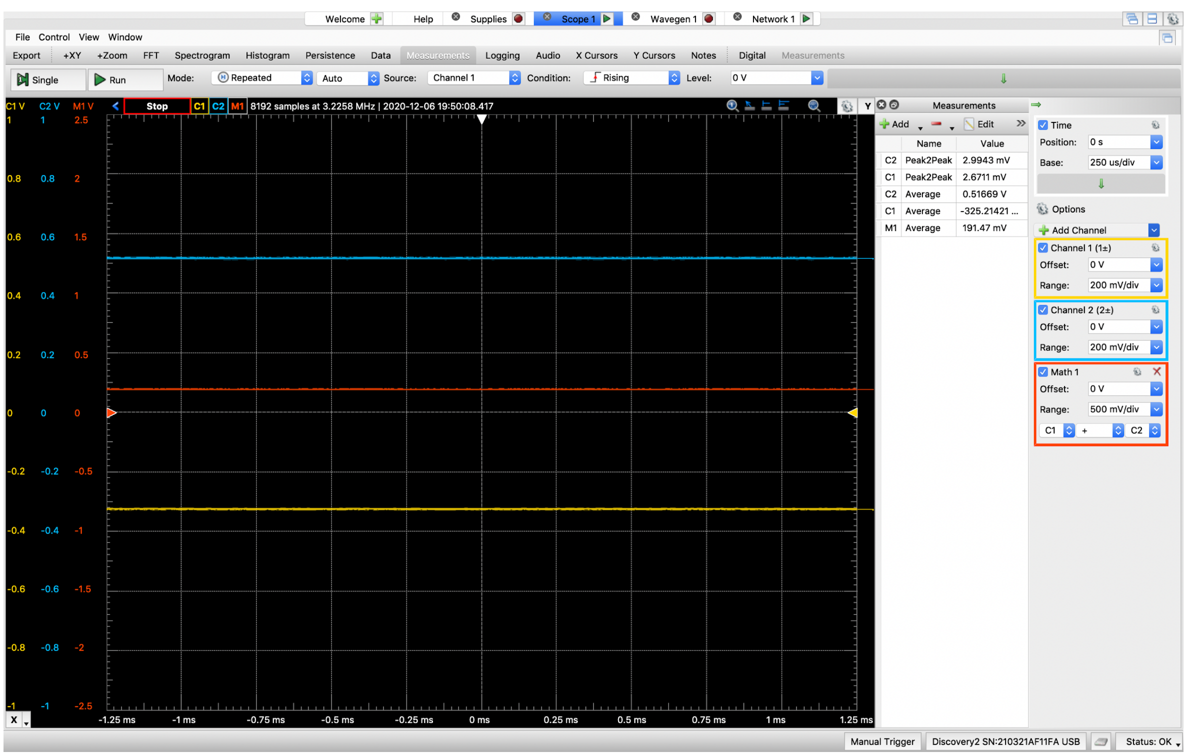

Figure 7: Filters output with rectifier and capacitor (1.54 kHz)

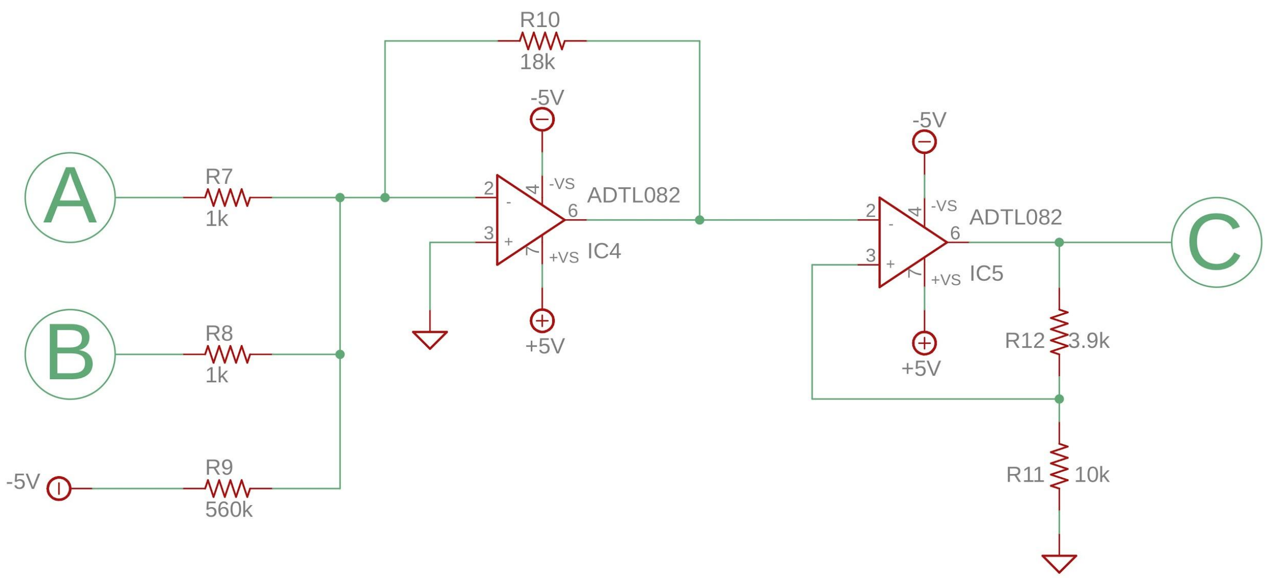

Figure 8: System design schematic (part 2)

- **Summation Amplifier**

  At 1.54 kHz:

  - Output voltage for the high pass filter is -325.21 mV
  - Output voltage for the low pass filter is 0.517 V

  At 2.3 kHz:

  - Output voltage for the high pass filter is -0.519 V
  - Output voltage for the low pass filter is 343.05 mV

Summation amplifier with a gain of -18x

$A = -(R_{10} / R_7)$

Let R = 18 kΩ

$-18 = -(R_{10} / R_7)$

$R_7 = 18\ k\Omega / 18$

$R_7 = 1\ k\Omega$

Since both input voltages should have the same gain of 18x at the output, therefore, R_8 should have the same value as R_7. Therefore $R_8 = 1\ k\Omega$.

Also, a level shift was implemented adding a DC offset to center the summation amplifier output at 0.

Before level shift:

At 1.54 kHz:

- Output voltage was -2.849 V

At 2.3 kHz:

- Output voltage was +2.5116 V.

To center at 0 we need a DC offset of +0.1554, derived from (-2.849 + 2.5116) / 2 = -0.1554.

$0.1554 \text{ V} = -[18 \text{ k}\Omega * (-5\text{V})] / R_9$

$R_9 = (18 \text{ k}\Omega * 5) / 0.1554 = 559 \text{ k}\Omega$

After level shift:

At 1.54 kHz:

- Output voltage is approximately -2.68 V

At 2.3 kHz:

- Output voltage is approximately +2.68 V

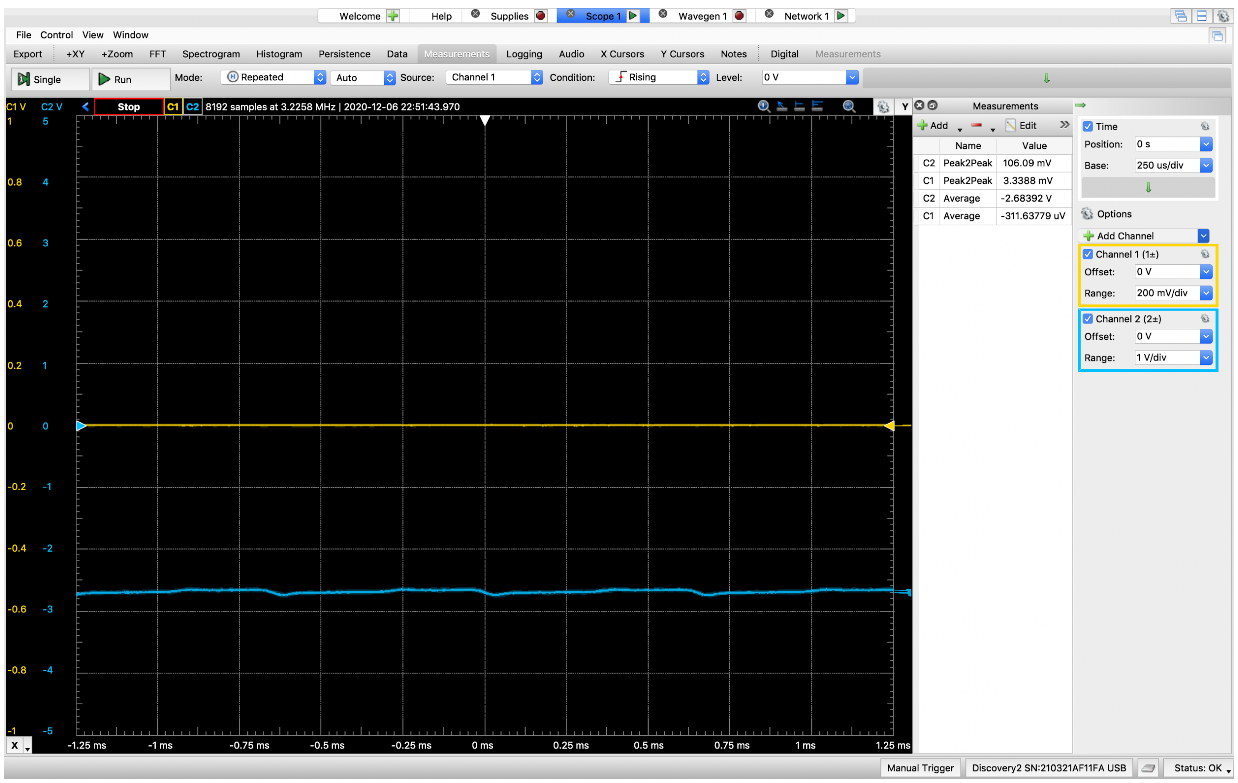

Figure 9: Summation amplifier output at 1.54 kHz

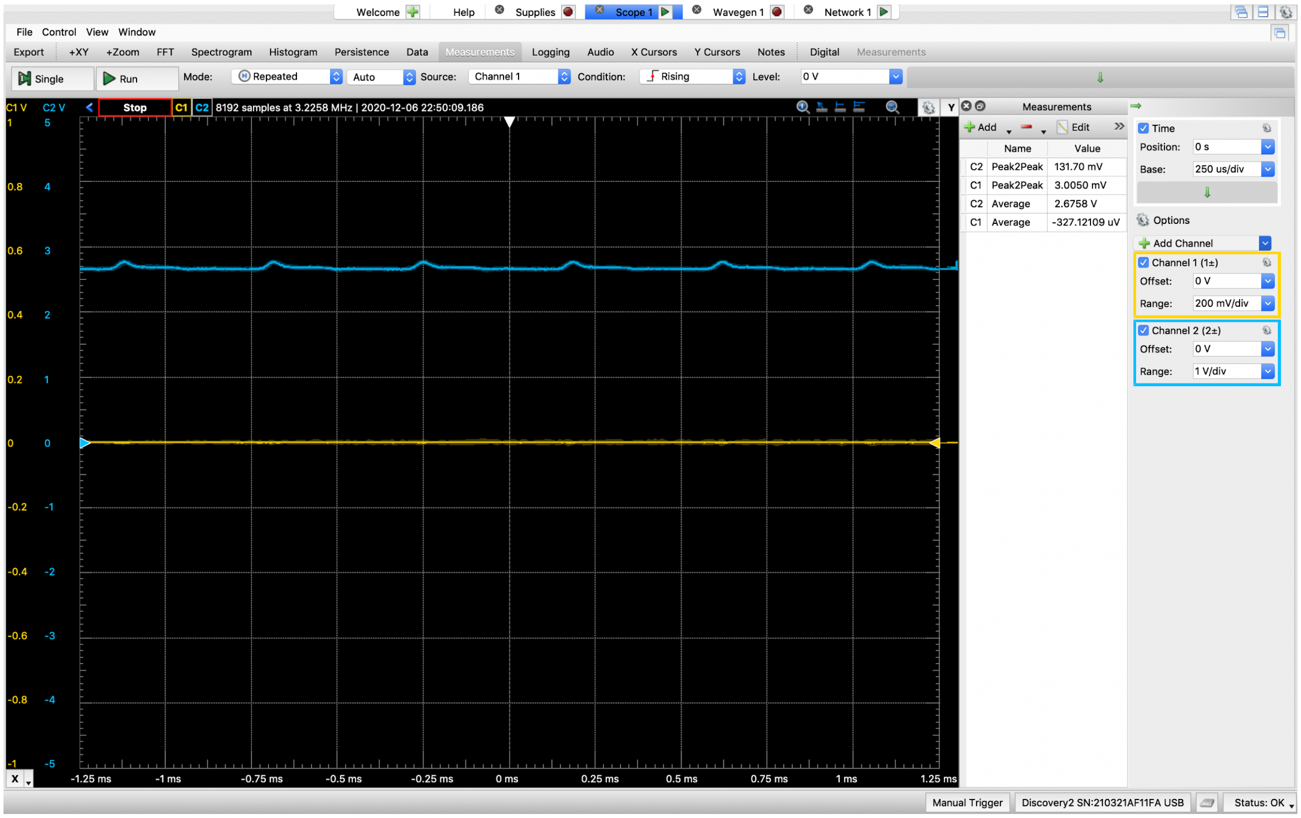

Figure 10: Summation amplifier output at 2.3 kHz

- **Schmitt Trigger**

  The ADTL082 operational amplifier clipped at 4.2934 V and -3.66368 V, therefore, the threshold voltage is set at +/- 2.68 V and rail voltage (Vrail) is between 3.66368 V and 4.2934 V.

  $V_{TH} = V_{RAIL} * [R_{11} / (R_{11} + R_{12})]$

  $V_{TH} = +/- 2.68$ V

  $V_{RAIL} = 3.66386$ V

  Let $R_{11} = 10$ kΩ

  $R_{12} = [(3.66 \text{ V} * 10 \text{ k}\Omega) - (2.68 \text{ V} * 10 \text{ k}\Omega)] / 2.68 \text{ V} = 3.66 \text{ k}\Omega$

  Therefore, $R_{12} = 3.9$ kΩ

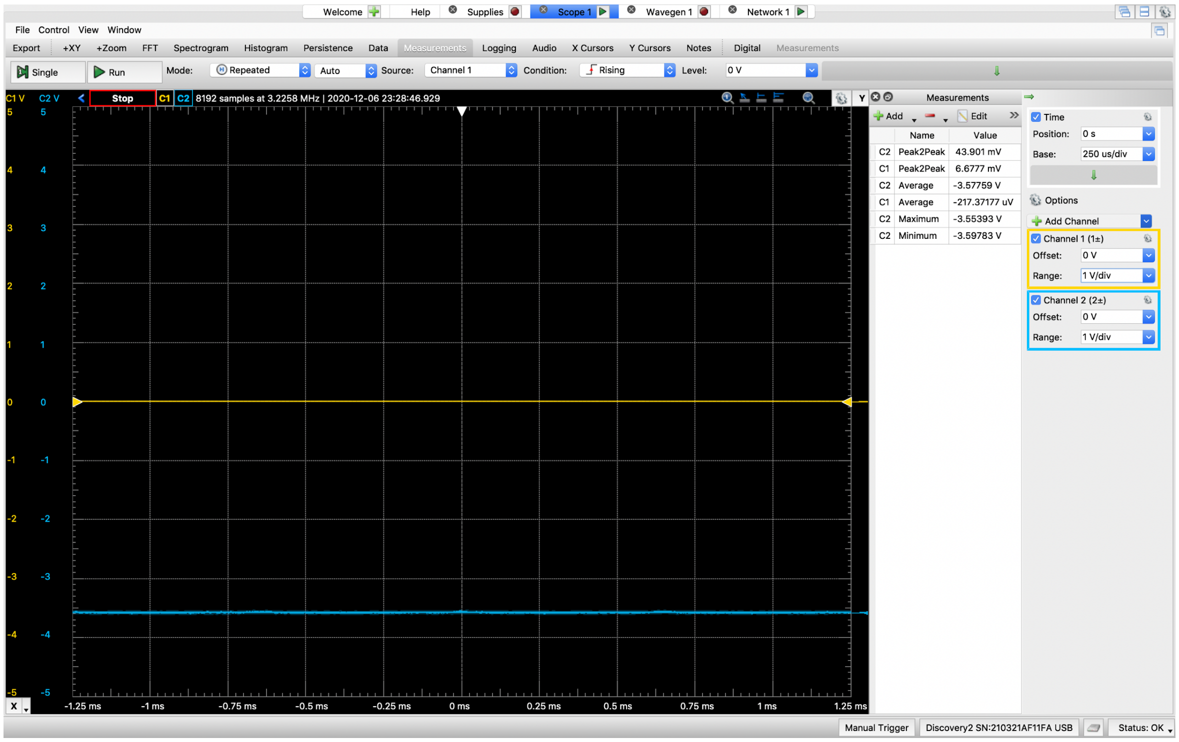

Figure 11: Schmitt trigger output at 1.54 kHz

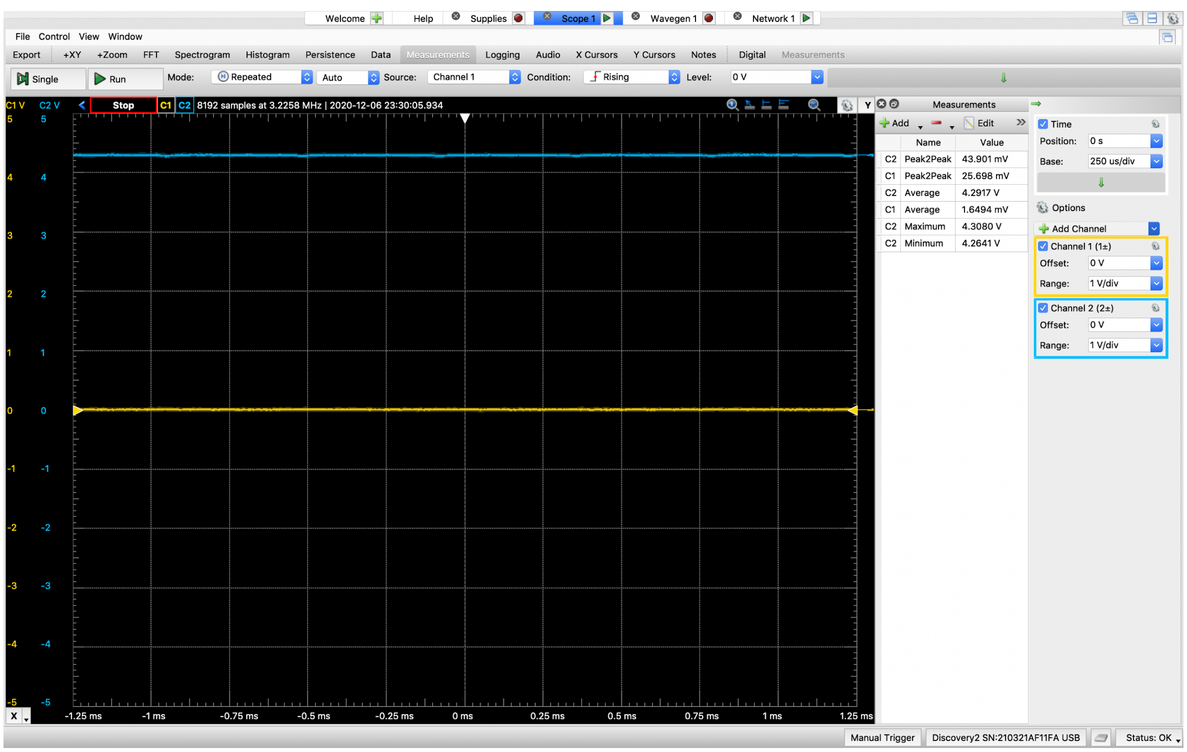

Figure 12: Schmitt trigger output at 2.3 kHz

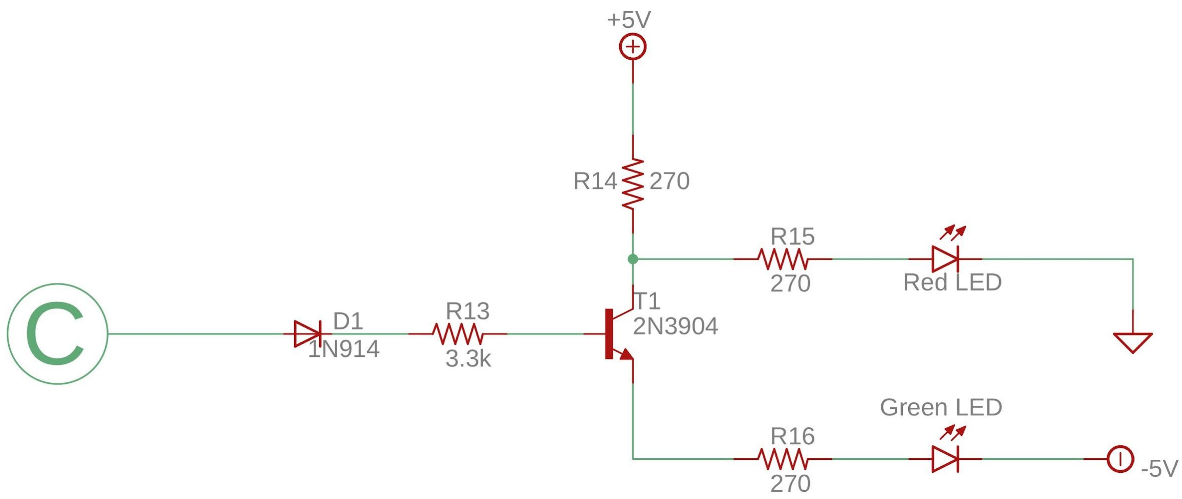

Figure 13: System design schematic (part 3)

- **Bipolar Junction Transistor Switch**

  This interface is used to switch the LEDs ON and OFF. At 1.54 kHz, the green LED turns ON while the Red LED is OFF and at 2.3 kHz, the red LED turns on while the green LED is OFF.

  R_{14} is implemented in this design to produce collector current which is also used to determine the base current.

  I_C = 5 V / 270 Ω = 18.5 mA
  For 2N3904 BJT switch ß = 30
  I_B = Ic / ß = 18.5 mA / 30 = 617.3 µA
  R_{13} = [3.66 - (0.7 + 0.7)] V / 617.3 µA = 3.66 KΩ
  Therefore, R_{13} = 3.3 kΩ

  Resistors R_{15} and R_{16} both have a resistance of 270 Ω, they are connected to the LEDs to limit the current flowing through the LEDs, preventing the LEDs from burning. The LEDs are configured in such a way that one turns ON when a positive voltage is supplied from the schmitt trigger while the other turns ON when a negative voltage is supplied from the schmitt trigger.

  After testing, the red LED turns ON at 1.7 kHz while the green LED is OFF and the green LED turns ON at 2.2 kHz while the red LED is OFF.

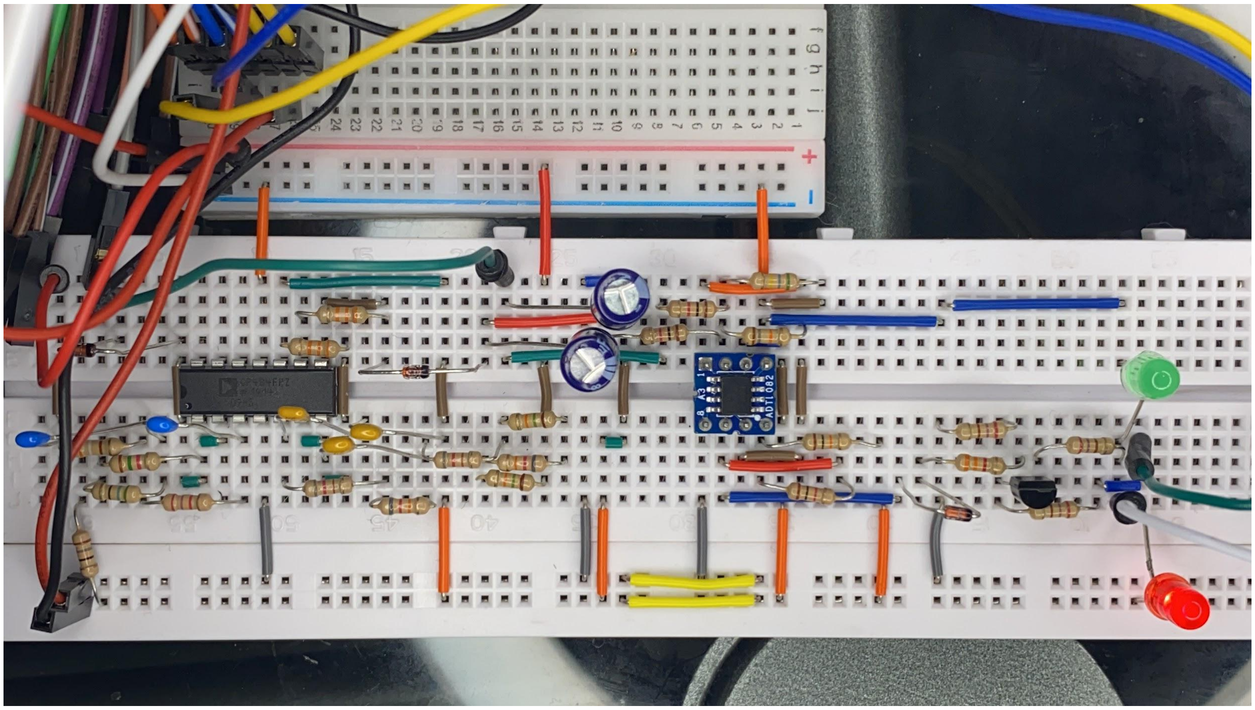

Figure 14: System design circuit

OPTION 2: DUAL AUDIO ANNUNCIATOR

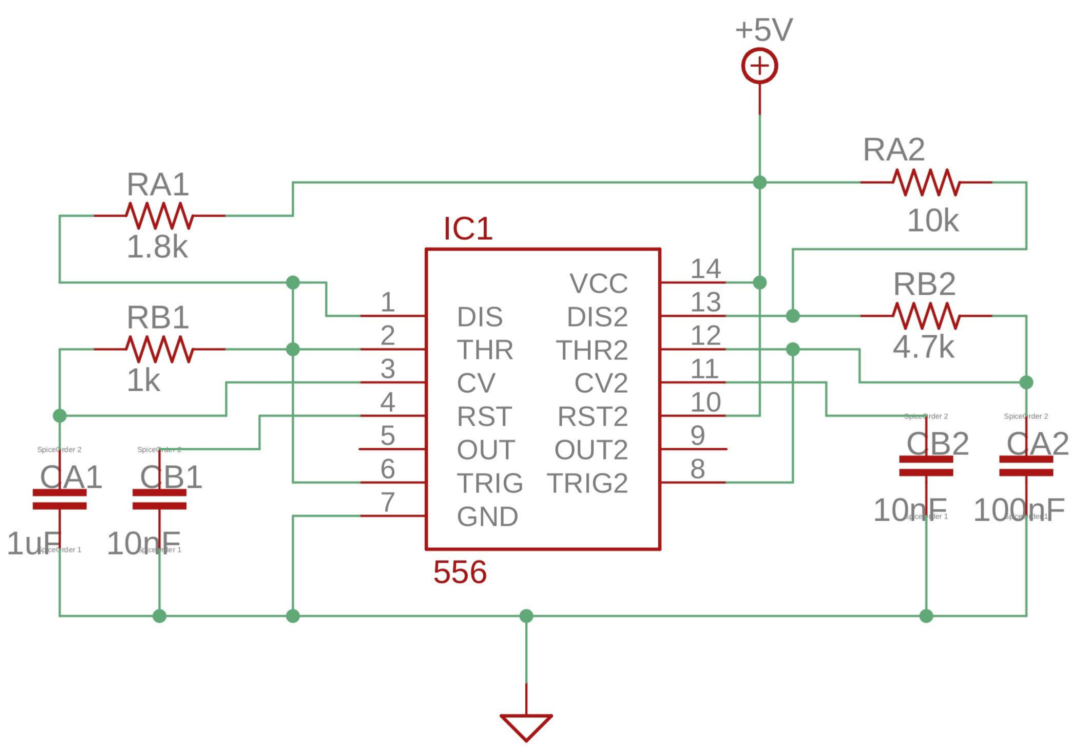

Figure 15: 556 timer astable schematic

- **Frequency: 400 Hz - 600 Hz**

  F = 400 Hz

  T = 1 / F = 2.5 ms

  At 75% duty cycle:

  t_1 = 2.5 ms * 0.75 = 1.875 ms

  t_1 = 0.693 * ($R_A + R_B$) * C

  Therefore, $R_A + R_B$ = 1.875 ms / (0.693 * 1 μF) = 2.7 kΩ

  t_2 = 2.5 ms * 0.25 = 0.625 ms

  t_2 = 0.693 * R_B * C

  Therefore, R_B = 0.625 ms / (0.693 * 1 μF) = 901 Ω

  R_A = 2.7 kΩ - 901 Ω = 1.8 kΩ

  R_A = 1.8 kΩ

  R_B = 1 kΩ

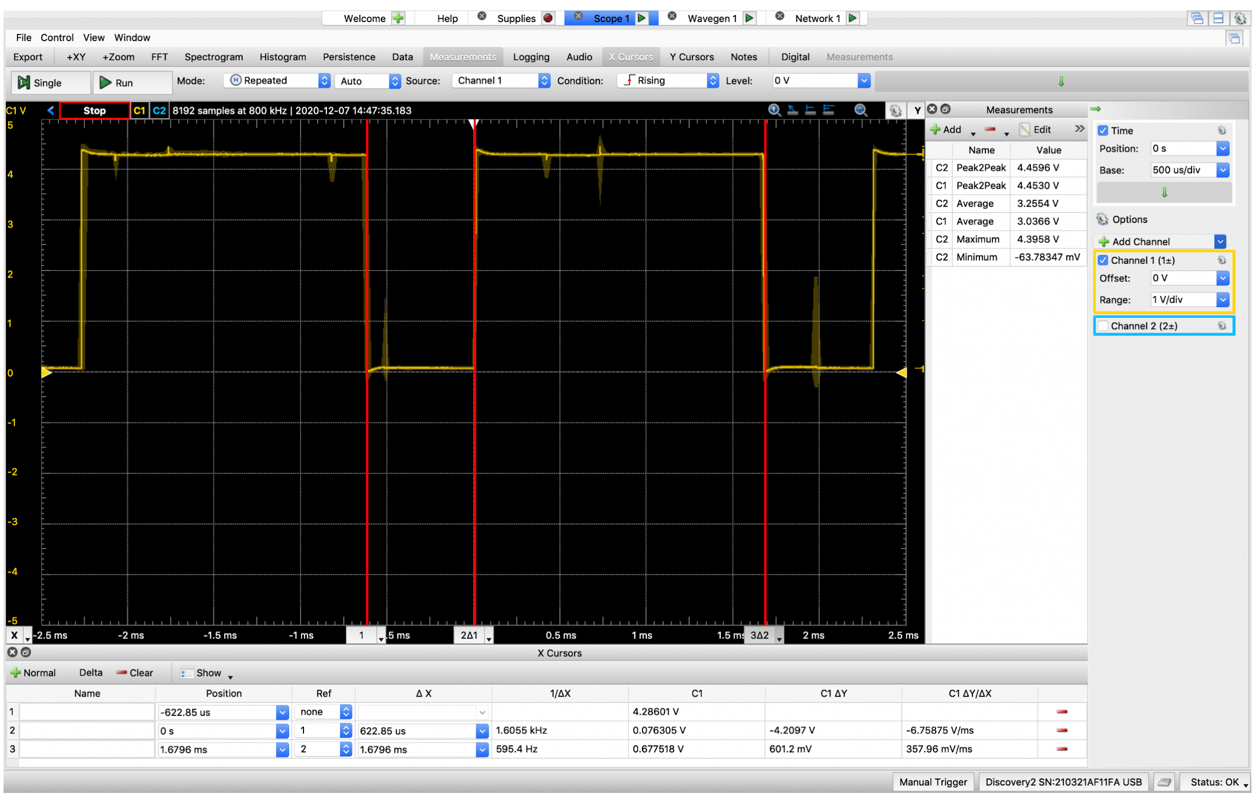

Figure 16: Scope for 400 Hz

T = (1.6796 + 0.62285) ms = 2.3 ms

F = 1 / T = 434 Hz

- **Frequency: 800 Hz - 1200 Hz**

  F = 800 Hz

  T = 1 / F = 1.3 ms

  At 75% duty cycle:

  t_1 = 1.3 ms * 0.75 = 0.975 ms

  t_1 = 0.693 * (R_A + R_B) * C

  Therefore, R_A + R_B = 0.975 ms / (0.693 * 100 nF) = 14.07 kΩ

  t_2 = 1.3 ms * 0.25 = 0.325 ms

  t_2 = 0.693 * R_B * C

  Therefore, R_B = 0.325 ms / (0.693 * 100 nF) = 4.69 kΩ

  R_A = 14.07 kΩ - 4.69 kΩ = 9.4 kΩ

  R_A = 10 kΩ

  R_B = 4.7 kΩ

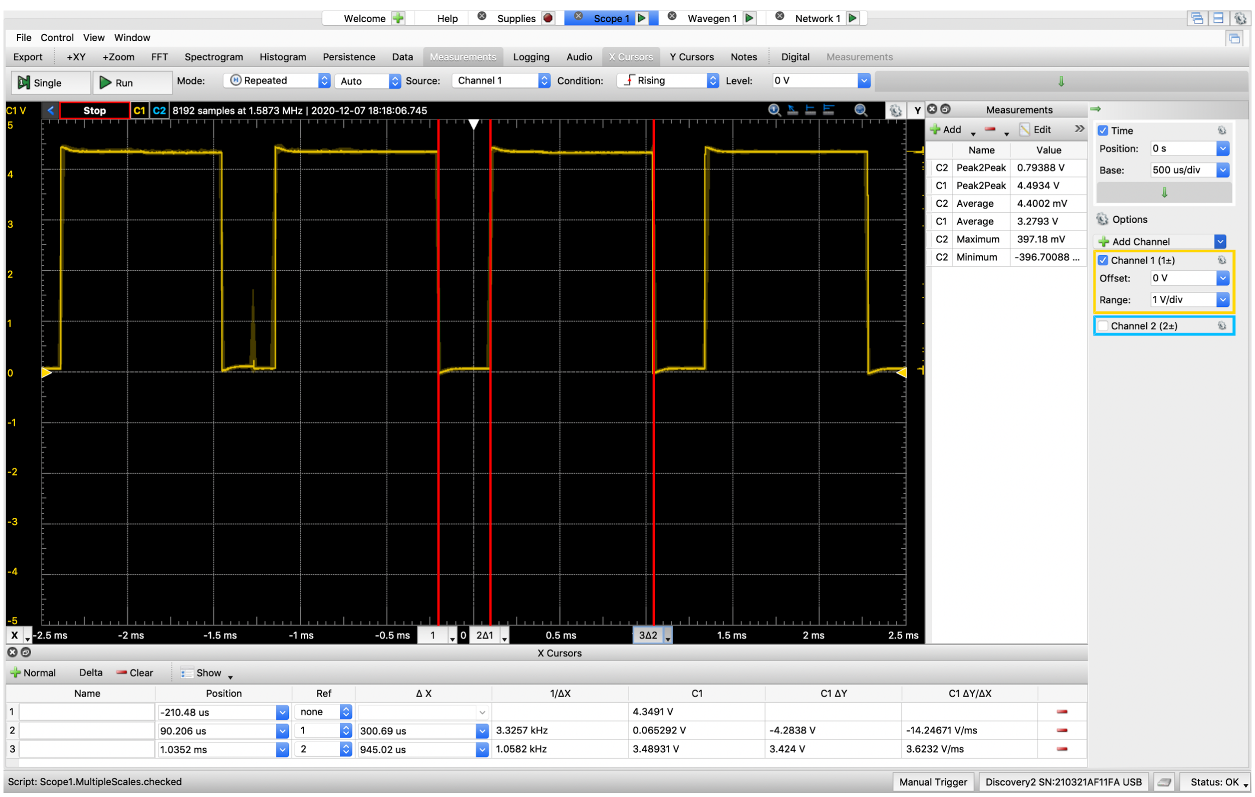

Figure 17: Scope for 800 Hz

T = (954.02 + 300.69) us = 1245.71 us

F = 1 / T = 803 Hz

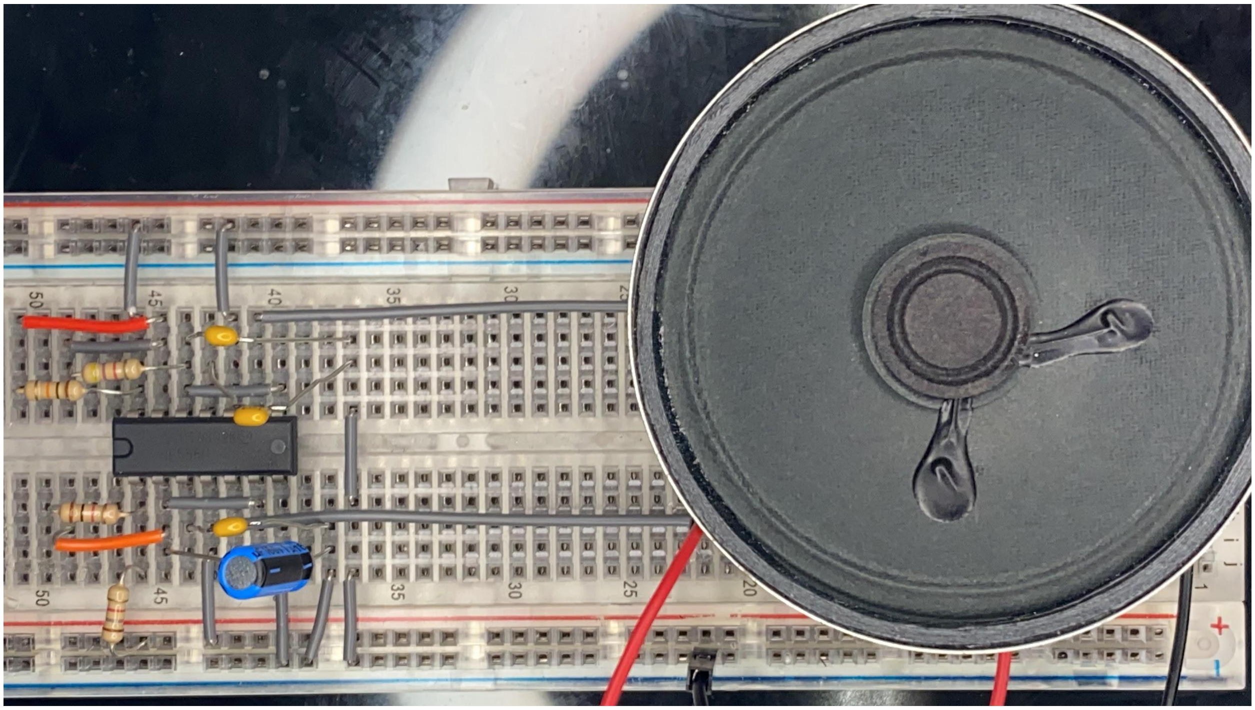

Figure 18: Tones design circuit (556 dual timer)

CONCLUSION:

I have successfully designed, tested and documented a latching control system that provides a start and stop output, based on the presence of 1 of 2 audio frequency tones. The link below is a visual demonstration of my project design and testing:

https://youtu.be/7q3L-giMWOI

Note: This section was added after the submission of this report

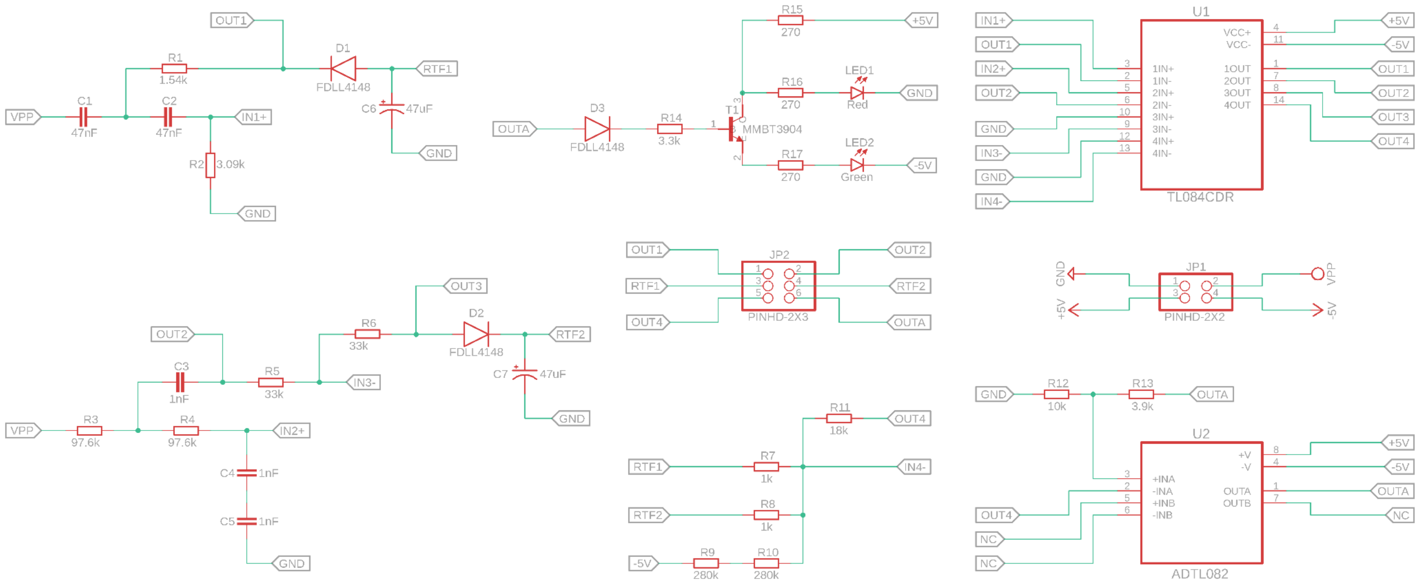

Figure 19: System schematic diagram

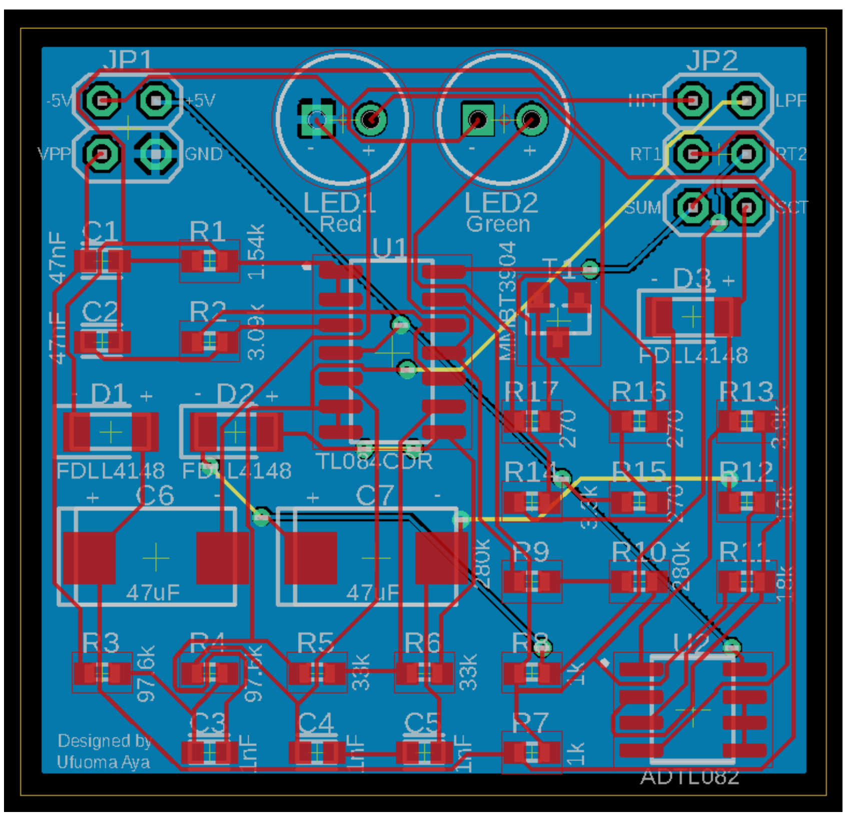

Figure 20: PCB layout

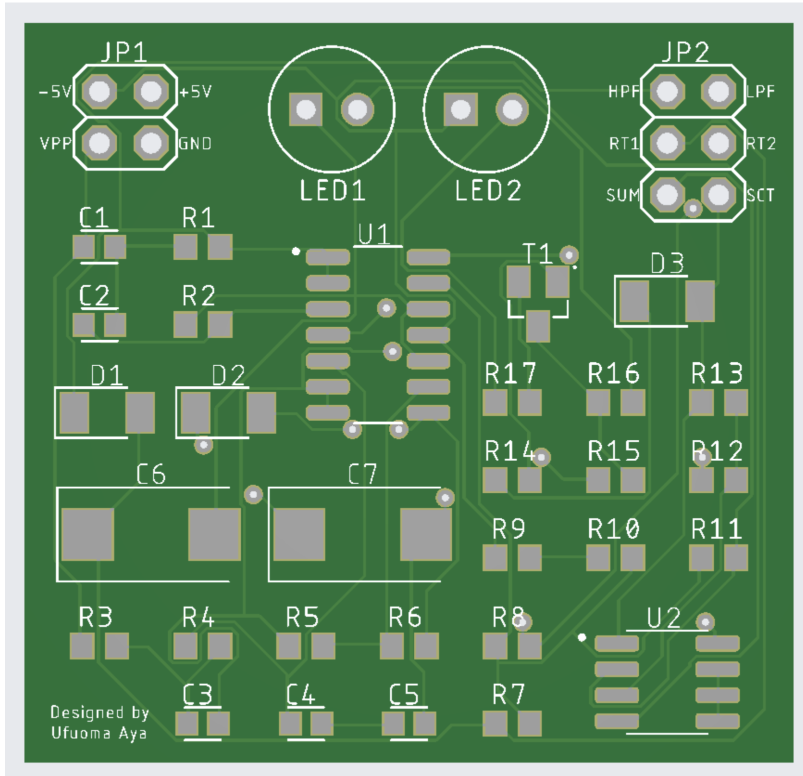

Figure 21: Gerber file PCB viewer

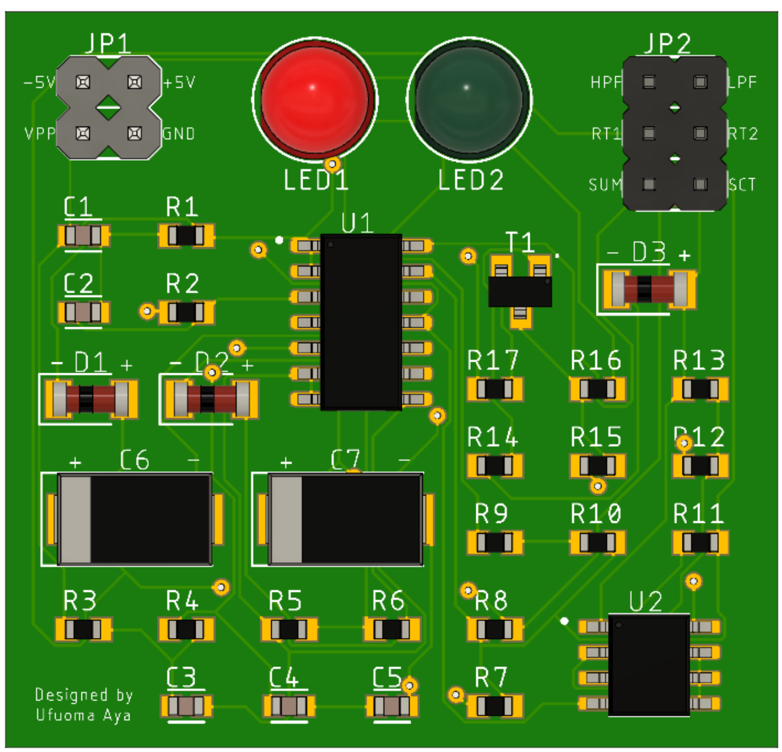

Figure 22: PCB