Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Digital Lab (ENCS2110)

Experiment No.3 Pre-Lab

Title: Encoders, Decoders, Multiplexers and Demultiplexers.

Prepared by:

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Section: 2 **Date:** September 27, 2022

Part 1: Circuits preparation and designation

1.1 4-to-2 Line Encoder with basic gates

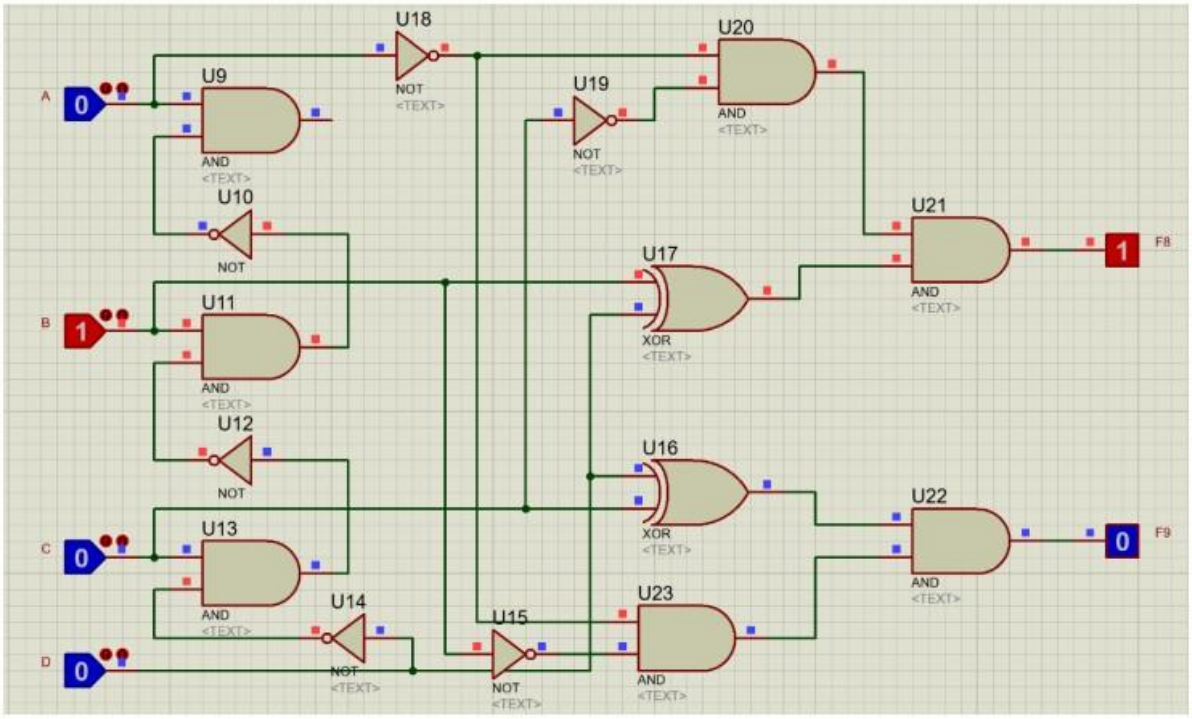


Figure 1: wiring diagram of 4-to-2-line Encoder

1.2 9-to-4 Line Encoder with TTL IC

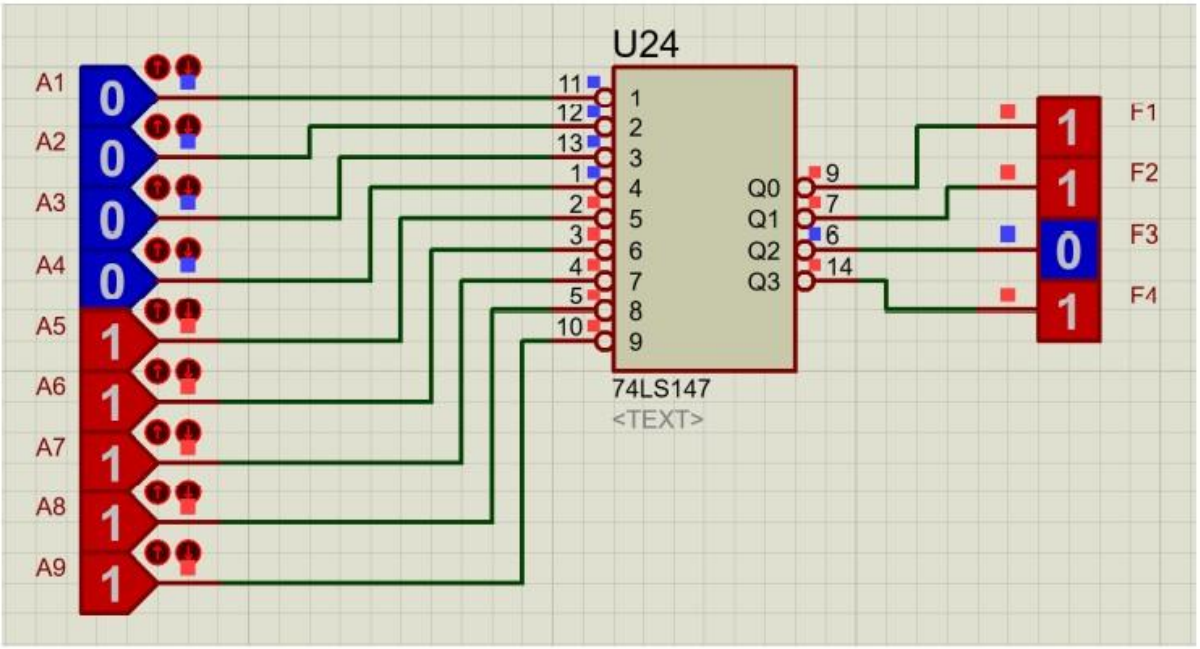


Figure 2:(74147) BCD Priority Encoder

1.3 2-to-4 Line decoder with basic gates

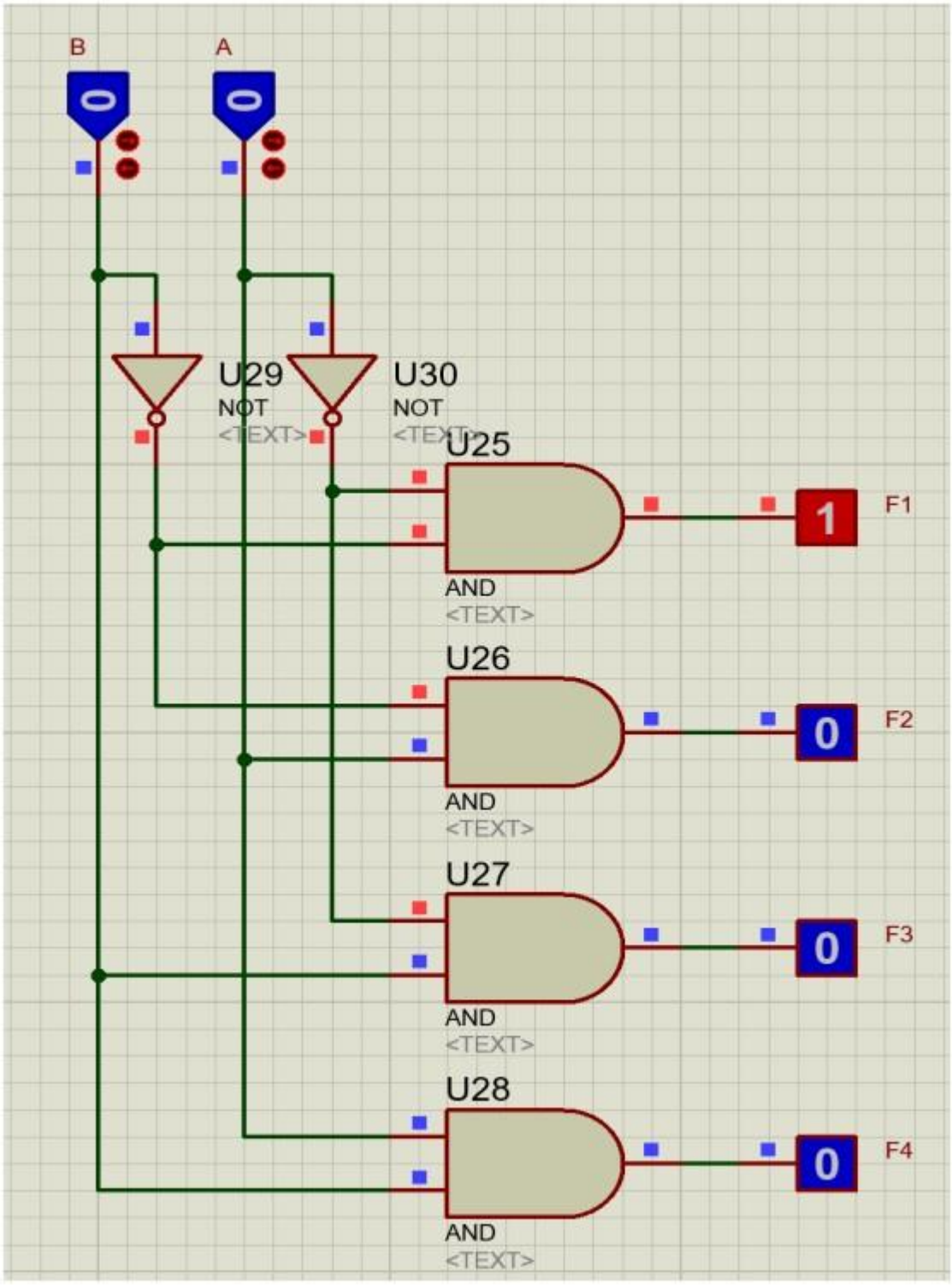


Figure 3: 2-to-4 Decoder

1.4 4-to-10 Line Decoder with TTL IC

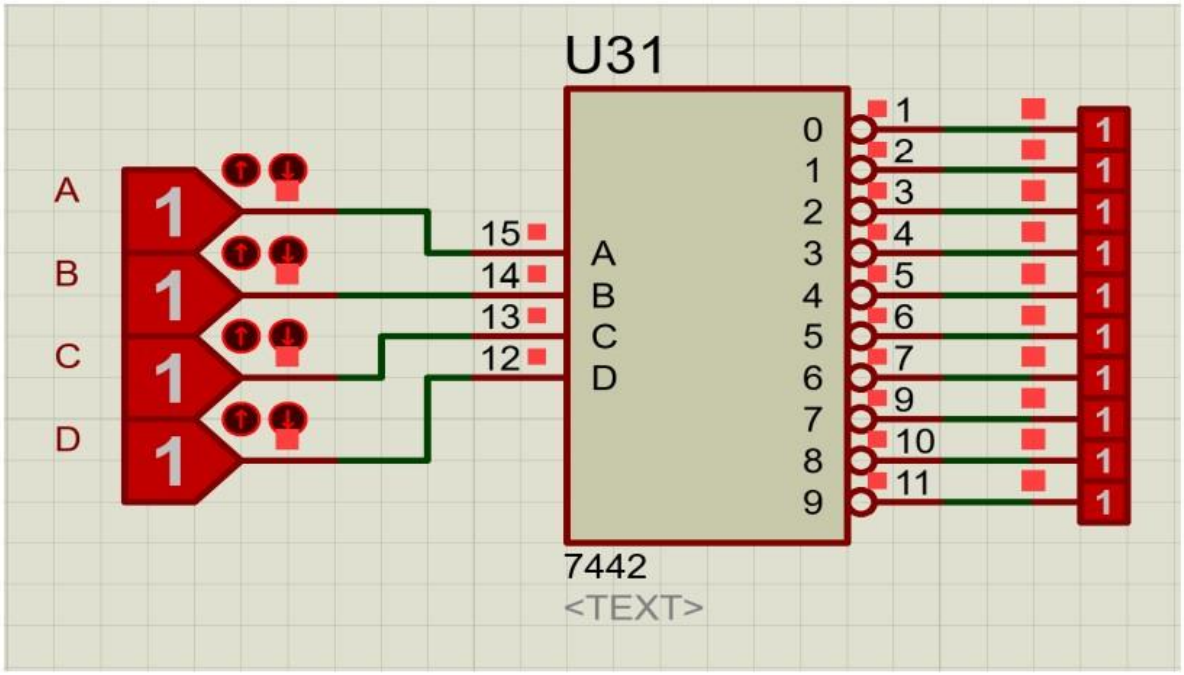


Figure 4: 4-to-10-line Decoder

1.5 2-to-1 Line Multiplexer with basic Gates

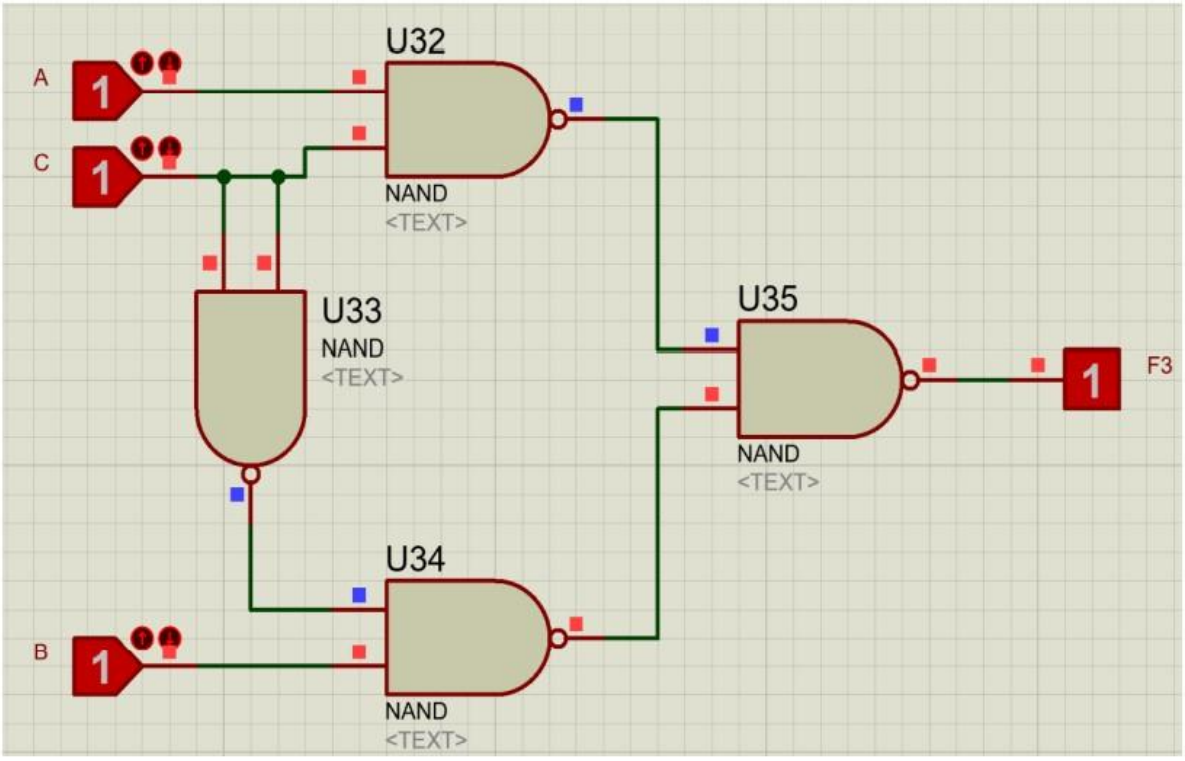
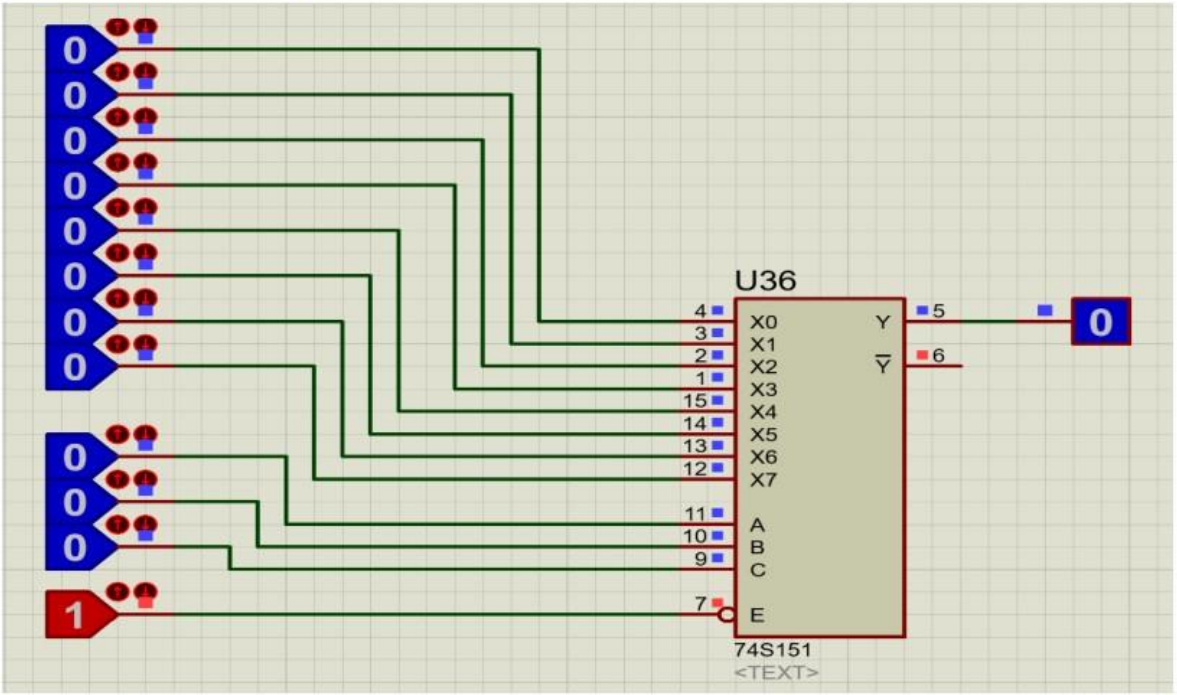


Figure 5: 2-to-1 Multiplexer

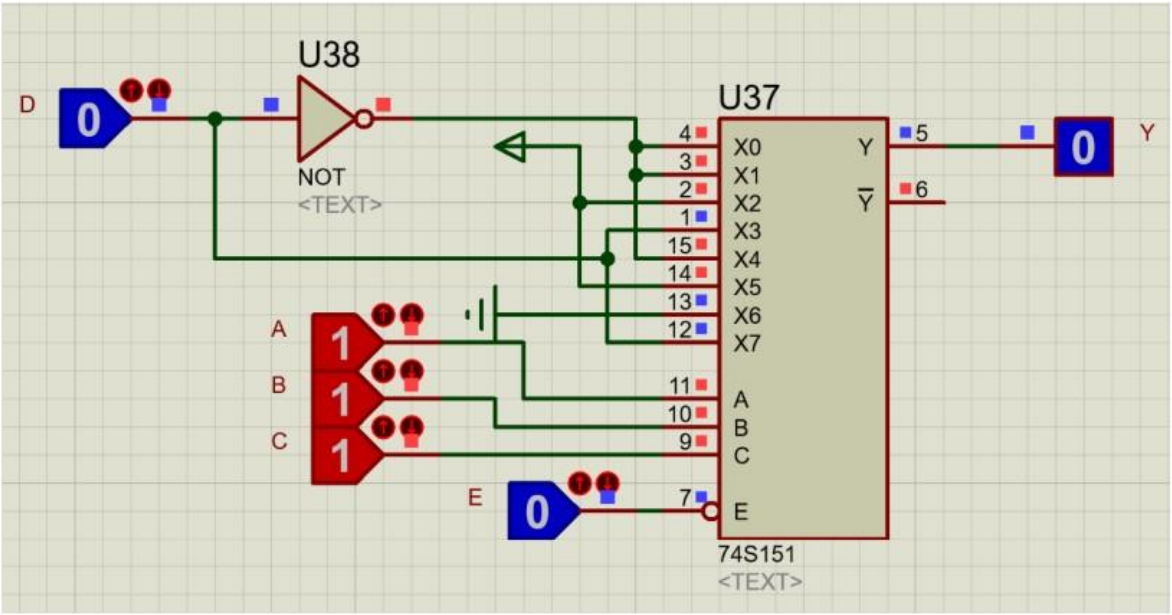
1.6 8-to-1 Line Multiplexer with IC



1.8 Using Multiplexer to Create a Logic Function

Given the following function:

$$F(A, B, C, D) = \Sigma(0,2,4,5,7,8,10,11,15)$$



1.9 1-to-2 Line Demultiplexer with Basic Logic Gates

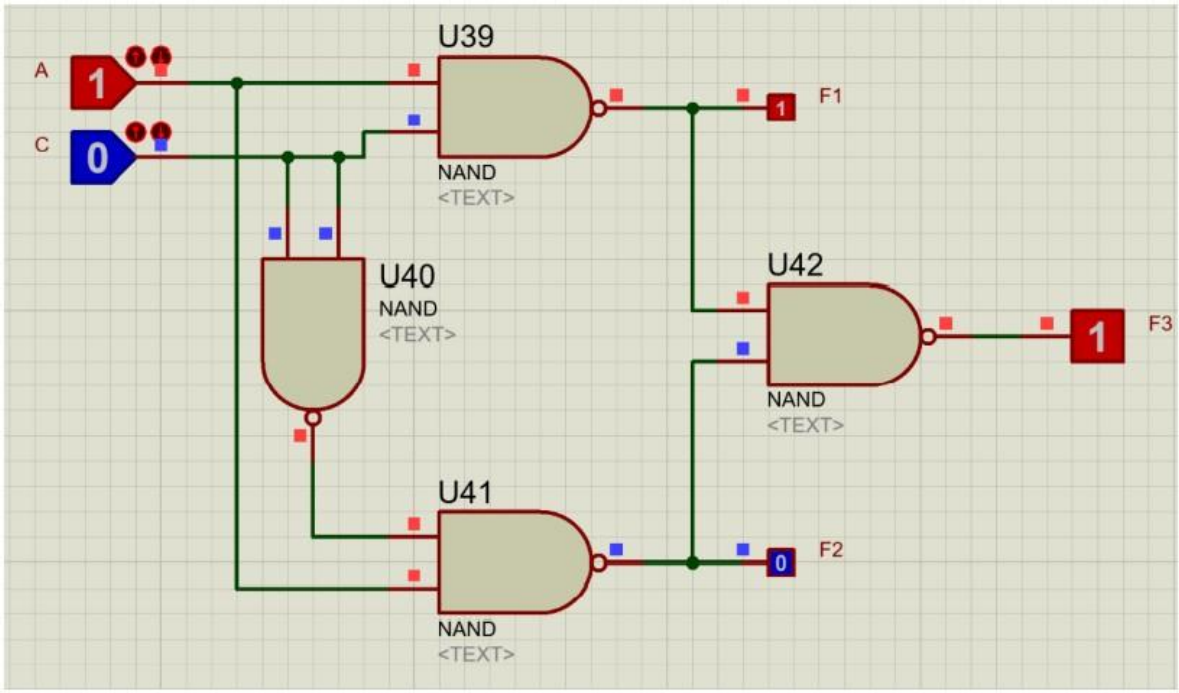


Figure 8: 1-to-2 Demultiplexer

1.10 1-to-8- Line Demultiplexer with CMOSIC

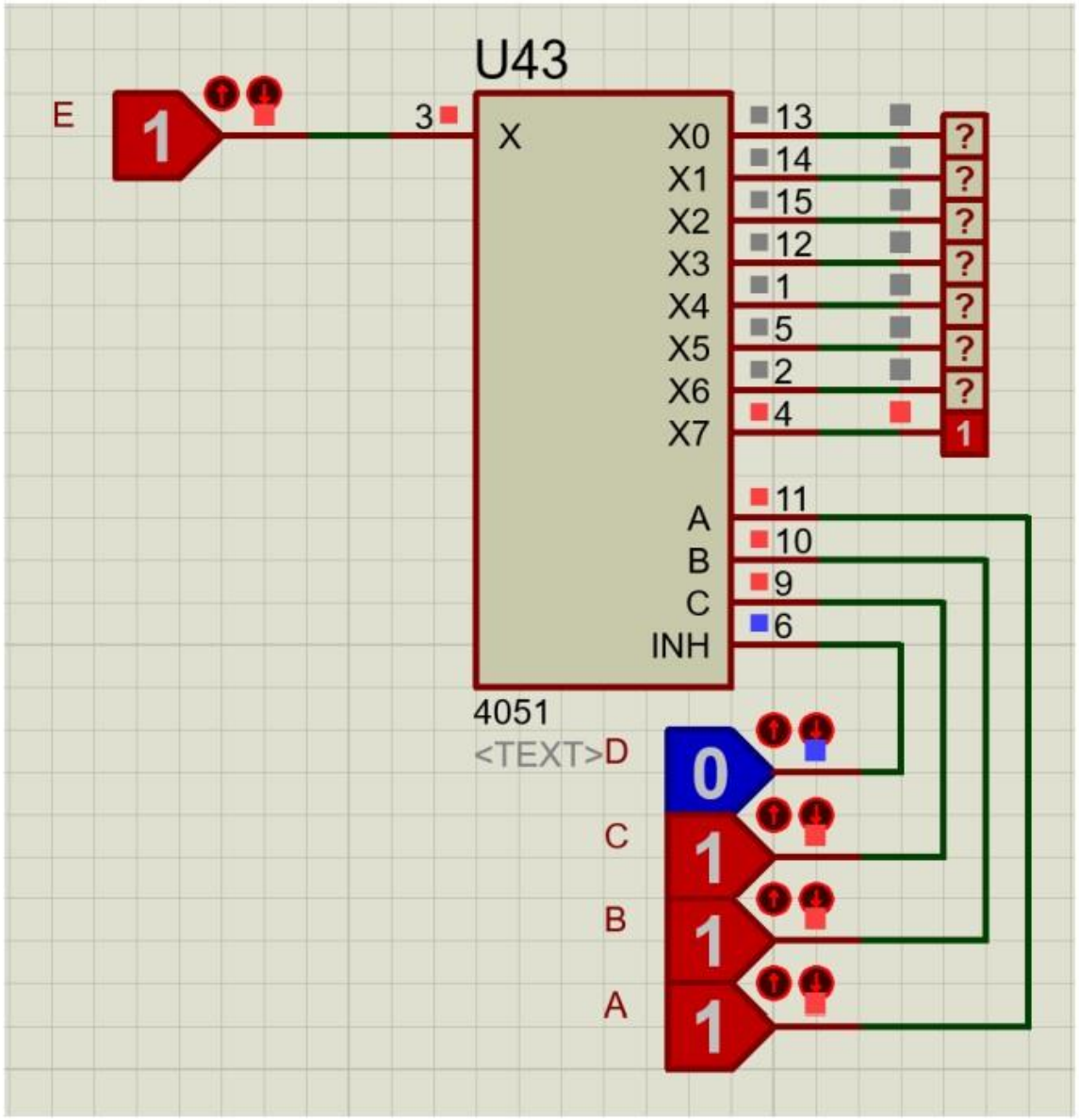


Figure 9: 1-to-8 Demultiplexer

Part 2: Designing a function using SN74151

Y = f(A,B,C)=AB'+B'C

Y= f(A,B,C)=AB'(C+C')+B'C(A'+A) (A+A') = 1, X AND 1 = X

Y=f(A,B,C)=AB'C+AB'C' + A'B'C+AB'C = AB'C + AB'C' + A'B'C (101, 100, 001)

Y=f(A,B,C) = Σ (1, 4, 5)

This means that the function gives 1 only at these three states, otherwise Y is 0.

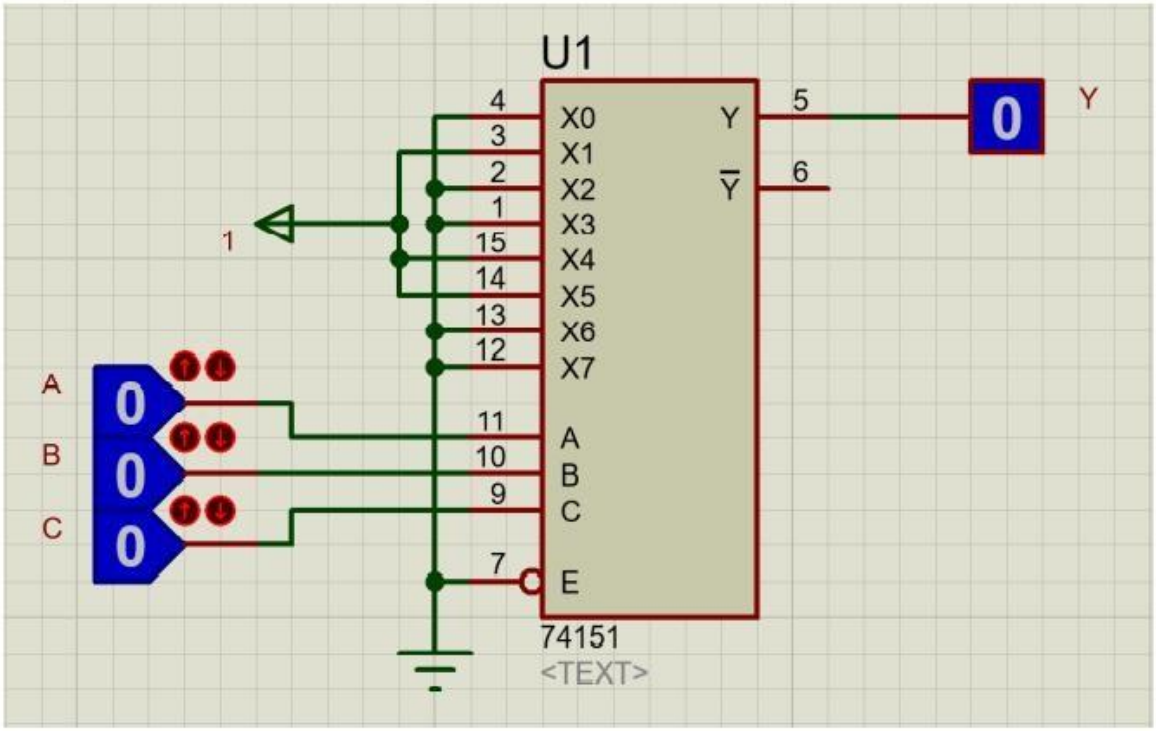


Figure 10: Y = f(A,B,C)=AB'+B'C implementation

Part 3: Designing a function using SN74138

Y = f(A,B,C)=A'BC+BC'

Y = f(A,B,C)=A'BC+BC'(A'+A)

Y = f(A,B,C)=A'BC+A'BC'+ABC' (011, 010, 110)

Y=f(A,B,C) = Σ (2, 3, 6)

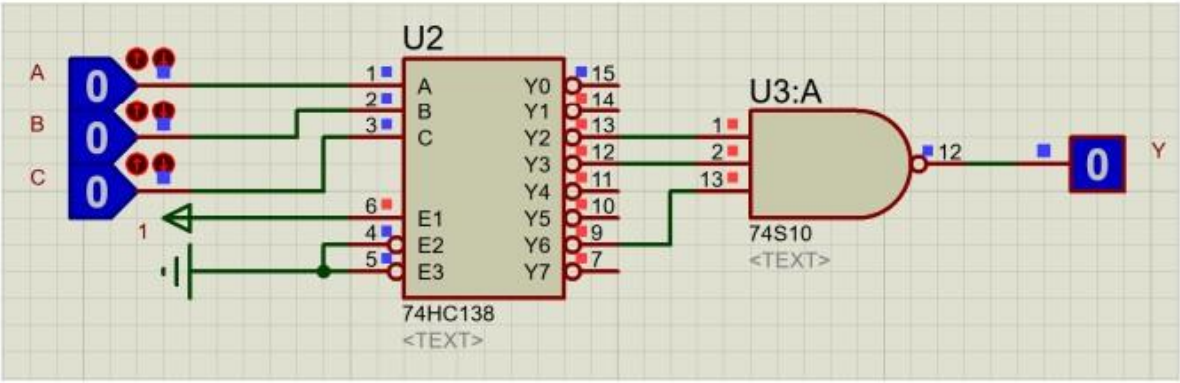


Figure 11: Y = f(A,B,C)=A'BC+BC' implementation