Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Digital Lab (ENCS2110)

Experiment No.2 Pre-Lab

Title: Comparators, Adders and Subtractors

Prepared by:

Name: Aya Dahbour **Number**:1201738

Instructor: Dr. Bilal Karaki **TA:** Eng. Ali Hamoudeh

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1. Design a three-bit comparator (using the basic comparator)

Basic comparator (1-bit comparator):

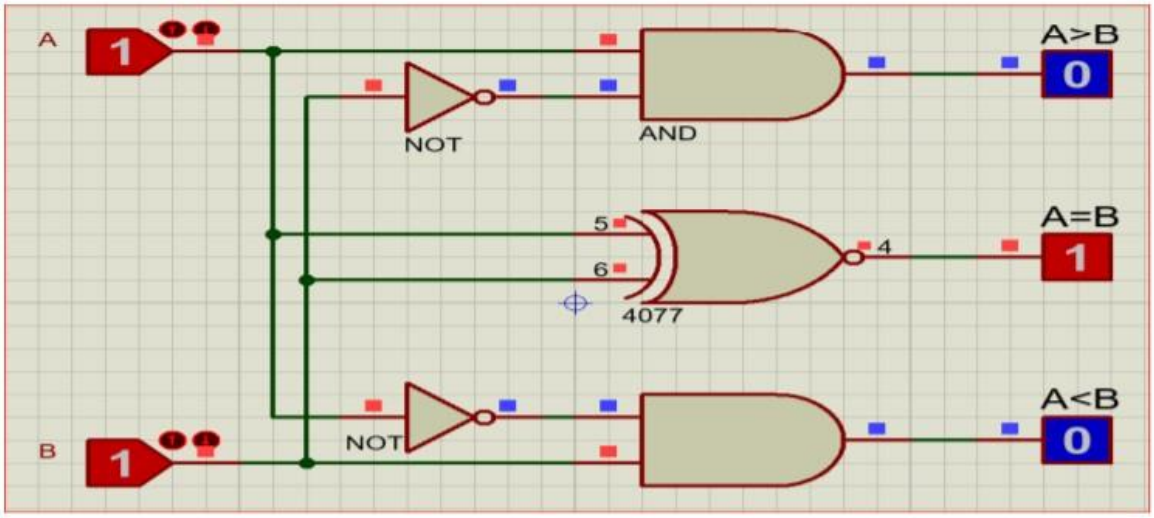

Figure (1): 1-bit comparator logic diagram

3-bit comparator using basic comparator:

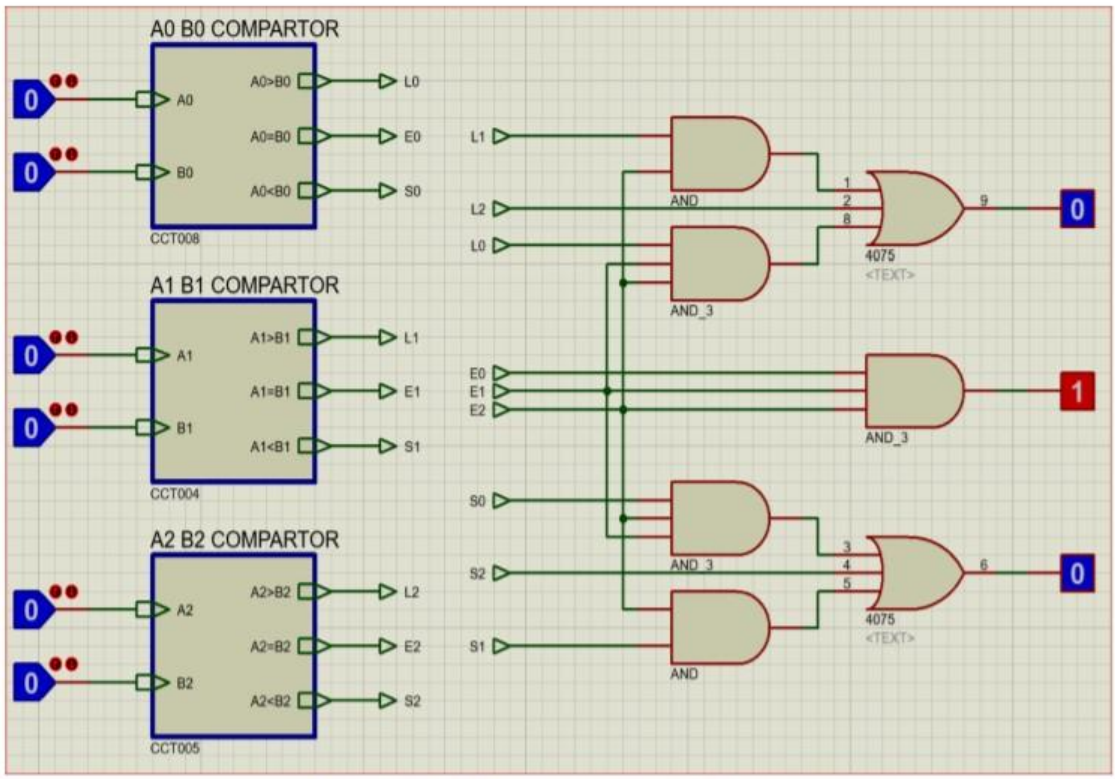

Figure (2): 3-bit comparator logic diagram

2. Design, Boolean function, and truth table of half-and full-adder

A. Half-adder:

Input		Output	
A	B	S	Cout(Carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table (1): Half-adder truth table

A \ B	0	1
0		(1)
1	(1)	

Table (2): S k-map

A \ B	0	1
0		
1		(1)

Table (3): Cout k-map

Summation and carry Boolean functions of half-adder obtained from K-maps:

- $S = AB' + A'B \equiv A \oplus B$
- $Cout = AB$

Half-adder circuit (logic diagram) design using basic gates:

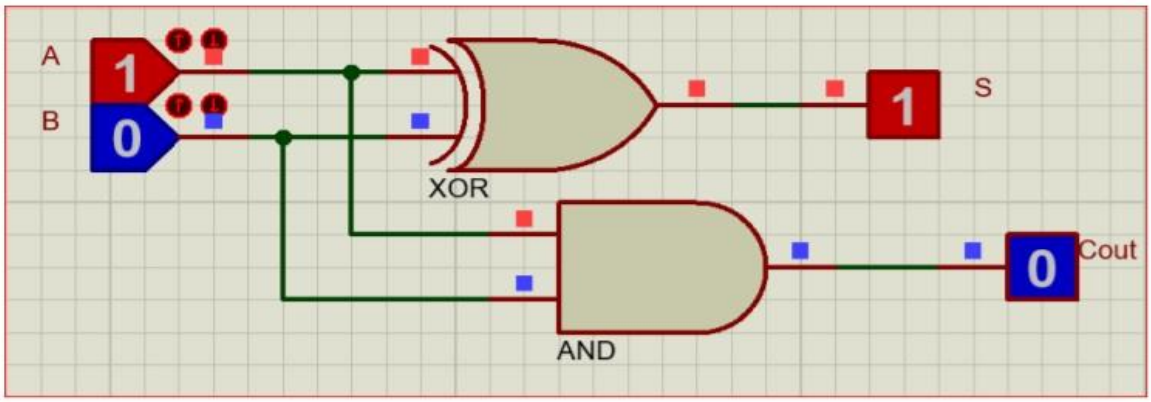

Figure (3): Half-adder logic diagram

B. Full-adder

Input			Output	
A	B	C	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table (4): Full-adder truth table

A \ BC	00	01	11	10
0		(1)		(1)
1	(1)		(1)	

Table (5): S k-map

A \ BC	00	01	11	10
0			1	
1		1	1	1

Table (6): Cout k-map

Summation and carry Boolean functions of full-adder obtained from K-maps:

- $S = A'B'C+A'BC'+AB'C'+ABC = A \oplus B \oplus C$
- $Cout = A'BC+AB'C+ABC'+ABC=(A \oplus B)C + AB$

Full-adder circuit design using basic gates: it also can be designed using HA component.

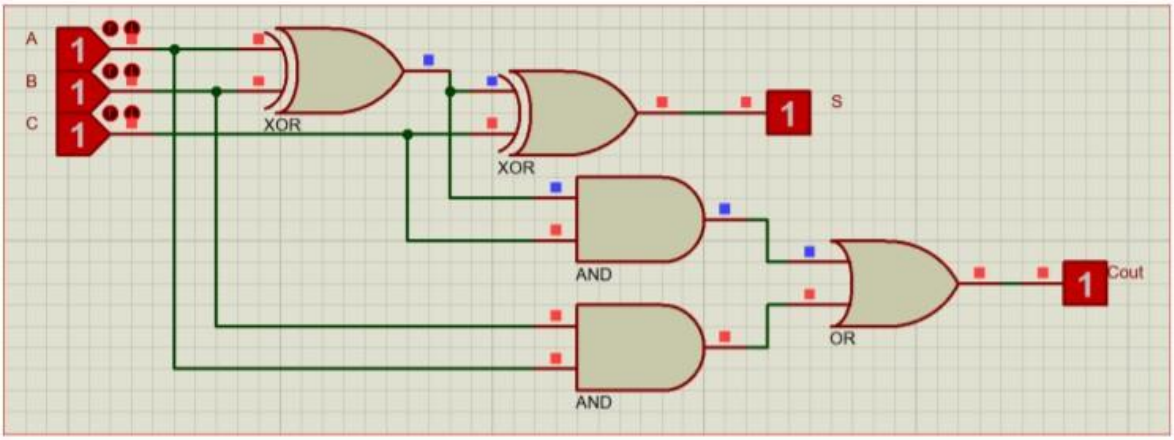

Figure (4): Full-adder logic diagram

3. Design the Logic Diagram, Boolean function, and truth table of a half- and full- Subtractor

C. Half-subtractor:

Input		Output	
A	B	D	Bout(Borrow)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Table (7): Half-Subtractor truth table

A \ B	0	1
0		(1)
1	(1)	

Table (8): D k-map

A \ B	0	1
0		(1)
1		

Table (9): Bout k-map

Difference and borrow Boolean functions of half-subtractor obtained from K-maps:

- $D = AB' + A'B \equiv A \oplus B$
- $Bout = AB$

Half- subtractor circuit (logic diagram) design using basic gates:

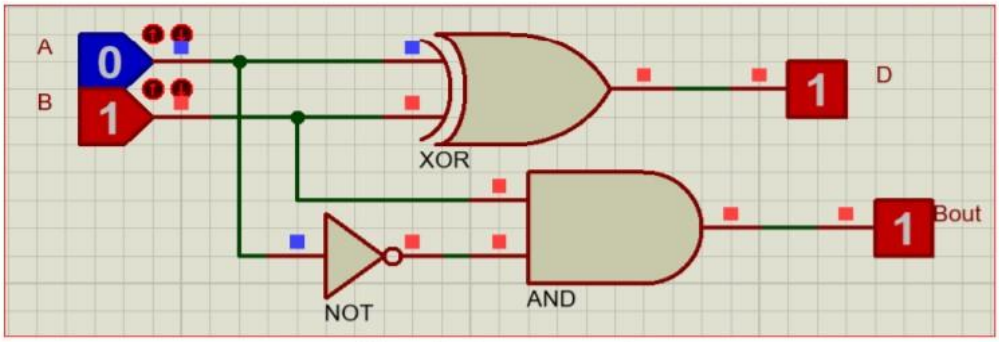

Figure (5): Half- subtractor logic diagram

D. Full- subtractor

Input			Output	
A	B	C	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table (10): Full-Subtractor truth table

A \ BC	00	01	11	10
0		1		1
1	1		1	

Table (11): D k-map

A \ BC	00	01	11	10
0		1	1	1
1			1	

Table (12): Bout k-map

Difference and borrow Boolean functions of full-subtractor obtained from K-maps:

- $D = A'B'C+A'BC'+AB'C'+ABC = A \oplus B \oplus C$
- $Bout = A'B'C+A'BC'+A'BC+ABC=(A \oplus B)'C + A'B$

Full- subtractor circuit design using basic gates: it also can be designed using HA component.

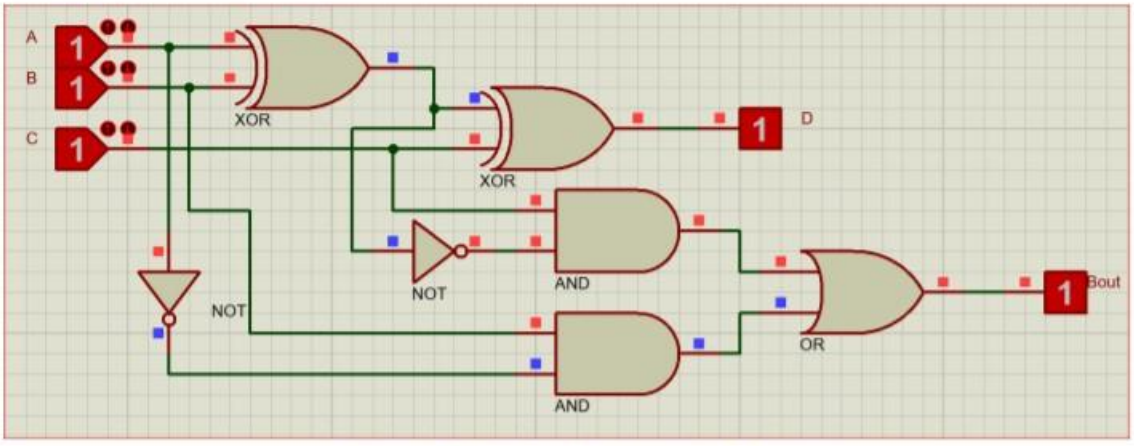

Figure (6): Full- subtractor logic diagram