Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Digital Lab (ENCS2110)

Experiment No.9 Pre-Lab

Title: A Simple Security System Using FPGA

Prepared by:
Name: Aya Dahbour **Number**:1201738

Instructor: Dr. Bilal Karaki **TA:** Eng. Ali Hamodeh

Section: 2 **Date:**May 26,2022

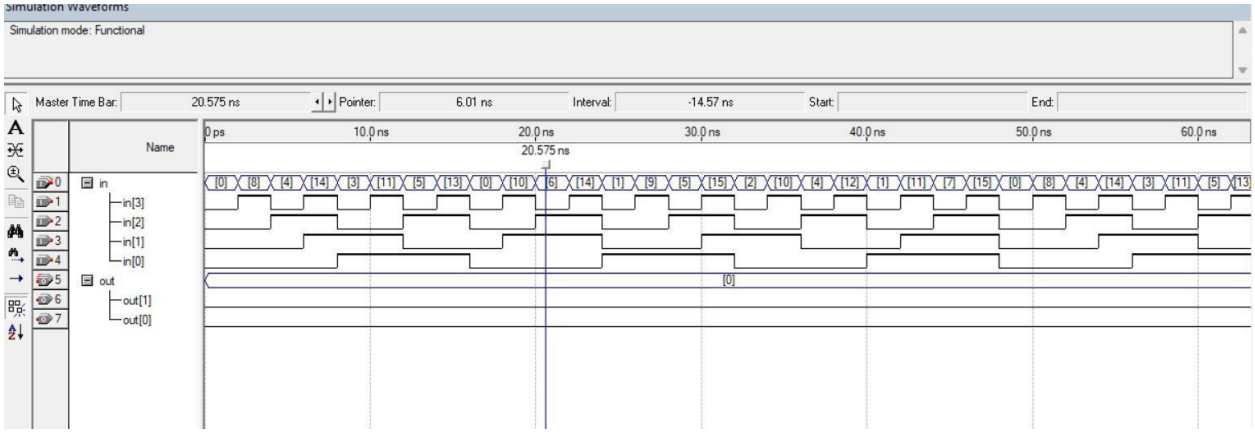
1. Design a 4 x 2 priority encoder by writing and simulating the Verilog code shown in Figure 3 using Quartus

- HDL Code

```
module priority_encoder(out,in);
 input[3:0]in;
 output reg [1:0] out;

 always @(in)
begin
case(in)
   4'b0001:out=2'b00;
   4'b001x:out=2'b01;
   4'b01xx:out=2'b10;
   4'b1xxx:out=2'b11;
   default:out=2'b00;
   endcase
 end
 endmodule
```

- Waveform

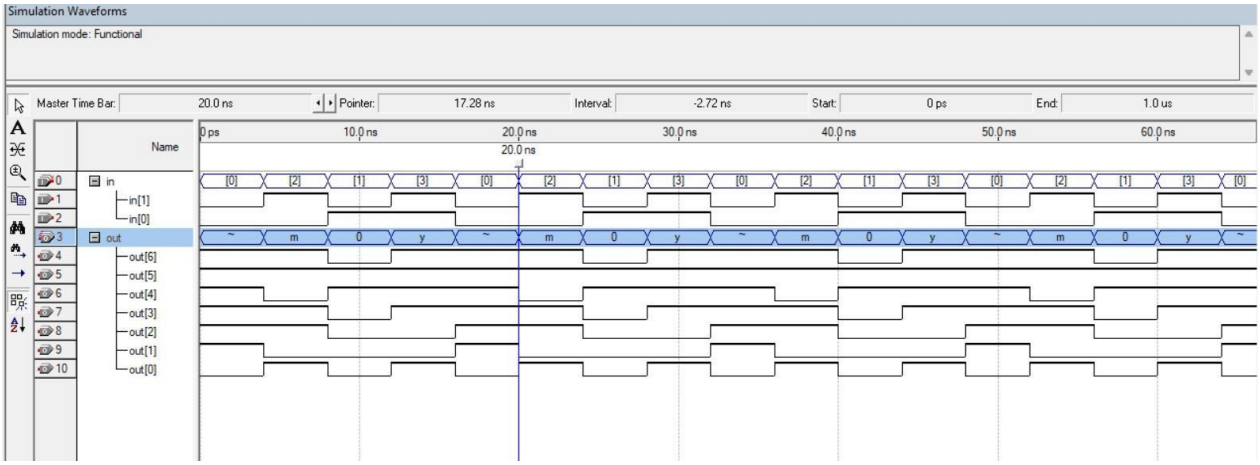


2. Design the 7-segment display driver by writing and simulating the Verilog code shown in Figure 4 using Quartus.

- HDL Code

```
2  module seven_segment_display_driver(in,out);
3   input [1:0] in;
4   output reg [6:0] out;
5   always @(in)
6     begin
7  case (in)
8   0:out= 7'b1111110;
9   1:out= 7'b0110000;
10  2:out= 7'b1101101;
11  3:out= 7'b1111001;
12   endcase
13  end
14  endmodule
```

- Waveform

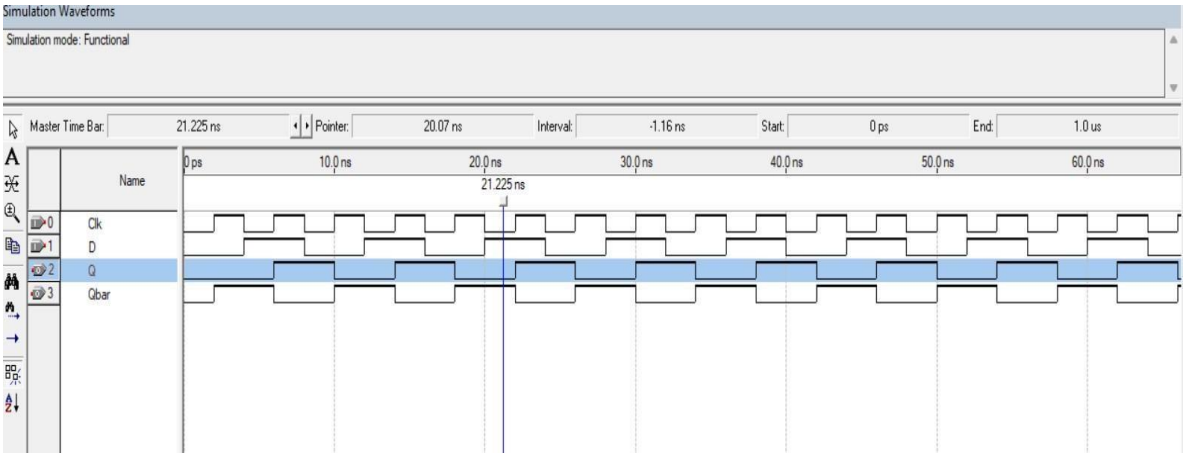


3. Write and simulate the Verilog code of a D- Flip Flop using Quartus.

- HDL Code

```
2   module D_FF (input D, Clk, output reg Q, Qbar);
3     // Q and Qbar change at the positive edge of Clk
4     // Notice that always is NOT sensitive to D
5     always @(posedge Clk)
6   begin
7     Q <= D; // Non-blocking assignment
8     Qbar <= ~D; // Non-blocking assignment
9     end
10    endmodule
```

- Waveform



4. Write and simulate the Verilog code of a 2x1 MUX using Quartus • HDL Code

```
2   module Mux2( input [1:0] A, B, input sel,output [1:0] Z);
3
4    assign Z = (sel == 0)? A : B;
5
6    endmodule
```

- Waveform