جامعة بيرزيت

BIRZEIT UNIVERSITY

Faculty of Engineering & Technology
Electrical & Computer Engineering Department

Digital Electronics and Computer Organization Lab ENCS 2110
Report #1

Encoders, Decoders, Multiplexers and demultiplexers

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3.1 Abstract

This Experiment aims to realize the operating principle of encoders/decoders and multiplexers/demultiplexers. Also, to build encoders , decoders , multiplexers and demultiplexers by using gates and IC. Furthermore, to use logic functions , and to understand how each one of the component works.

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3.2 Theory

3.2.1 Encoders

An encoder is a combinational circuit that proceeds the reverse operation of the decoder. The number of inputs is counted by 2^N, and it has N outputs. The encoder converts the input to binary code.

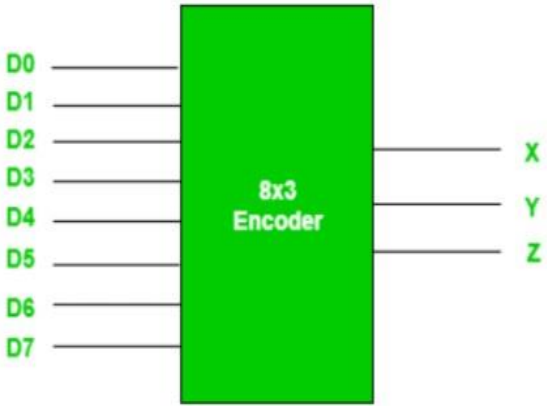


Figure 3.1 Encoder Component

Sometimes there is more than one input is activated, so the inputs must get a priority so that the encoder works correctly, so an encoder was implemented which is a priority encoder, which gives priority to the input marked with the highest priority. The priority means if there exists more than two inputs, one of them is higher in priority, the output will be for the input with the highest priority.

3.2.2 Decoders

A decoder is a combinational circuit that has N inputs and proceeds 2^N outputs. Depending on the circuit if it’s active low or high, only one output of decoder will be activated depending on the input, and others will stay inactivate.

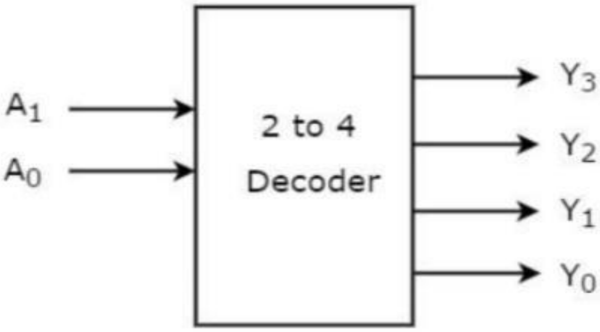


Figure 3.2 Decoder component

3.2.3 Multiplexers

A multiplexer is a combinational circuit that consists of one output and 2N inputs controlled by N selectors (selection lines). The output of the mux is the same as the selected input, so if each selection of Ns moves the corresponding input to the output. MUXs can be used to implement all standard logic gates such as NOT, AND, and OR gates.

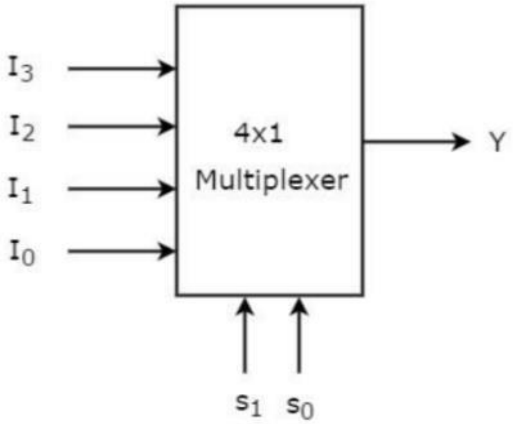


Figure 3.3 : 4-to-1 MUX block diagram

3.2.4 Demultiplexers

A demultiplexer is a combinational circuit that has one input and 2N outputs controlled by N selectors (selection lines). It performs the reverse operation of the multiplexer. The output of the mux is affected by the value of the input. So the output depends on both input and selection lines.

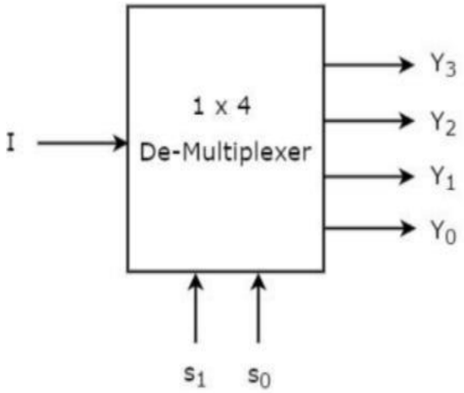


Figure 3.4: 1-to-4 demultiplexer block diagram

3.3 Procedure & Discussion

3.3.1 Constructing 4-to-2-Line Encoder with Basic Gates

Encoder 1 in Module IT-3004 block was used to implement a 4-to-2 encoder. The block was supplied with +5V power using power supply IT-3000. Inputs A~D were connected to data switches SW0~SW3. And, outputs F8 and F9 were connected to logic indicators L0 and L1.

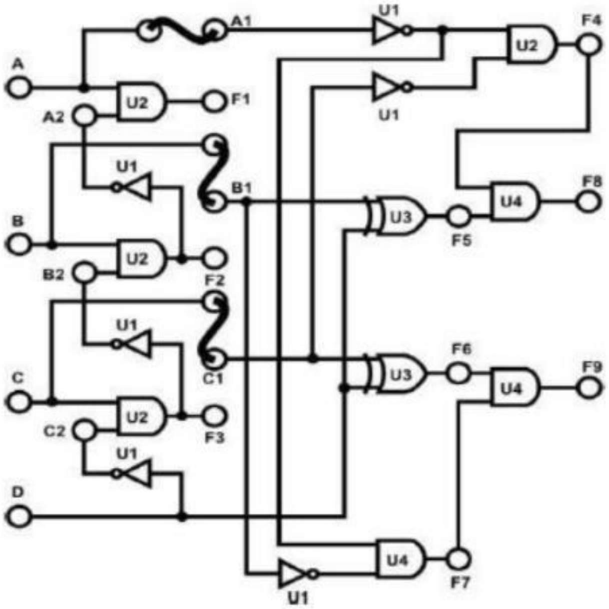
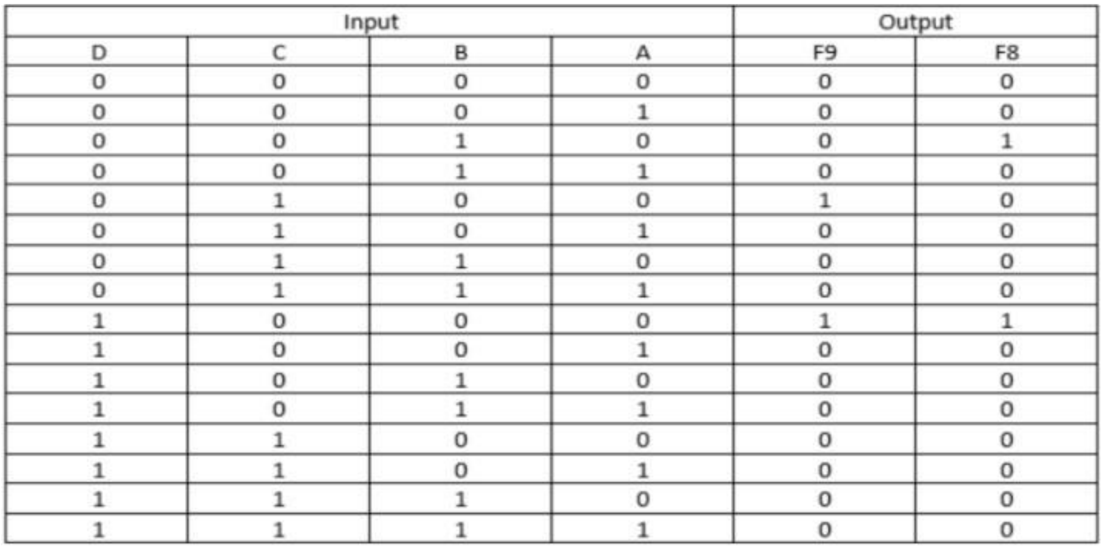


Figure 3.5: 4-to-2 encoder using basic gates

Table 3.1: 4-to-2 encoder truth table



Input				Output	
D	C	B	A	F9	F8
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

3.3.2 Constructing 9-to-4- Line Encoder with TTL IC

Using the same module but a different block which is Encoder 2 to construct a 9-to-4 encoder. All inputs A1~A8 were connected to DIP switches 1.0~1.7, and A9 to DIP switch 2.0. Outputs F1~F4 were connected to logic indicators L1~L4.

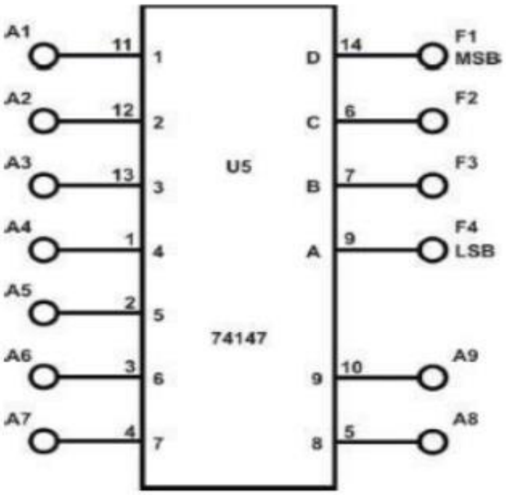
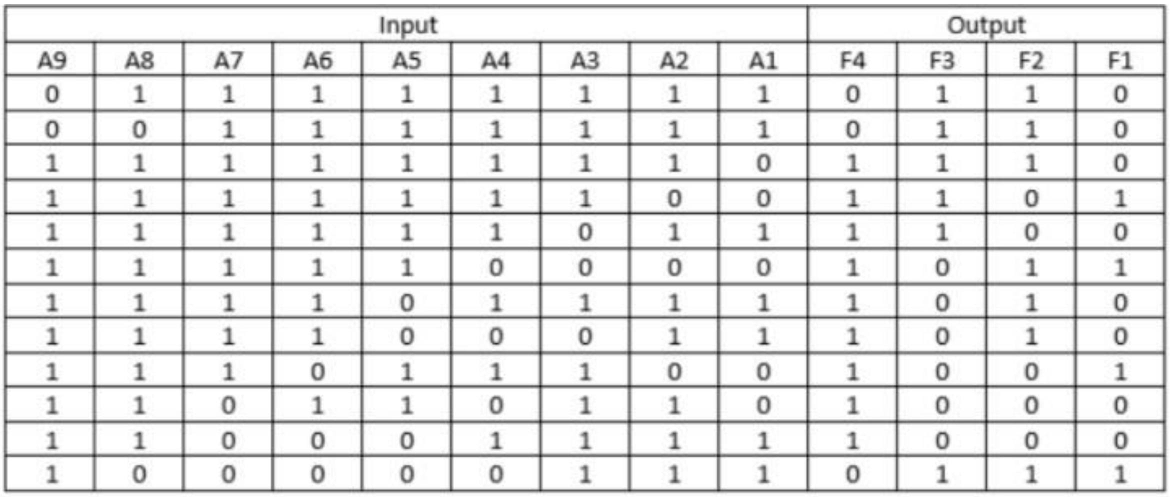


Figure 3.6: (74147) BCD Priority Encoder

Table 3.2: BCD priority encoder truth table



Input									Output			
A9	A8	A7	A6	A5	A4	A3	A2	A1	F4	F3	F2	F1
0	1	1	1	1	1	1	1	1	0	1	1	0
0	0	1	1	1	1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	0	0	0	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1	0	1	0
1	1	1	1	0	0	0	1	1	1	0	1	0
1	1	1	0	1	1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1	0	1	0	0	0
1	1	0	0	0	1	1	1	1	1	0	0	0
1	0	0	0	0	0	1	1	1	0	1	1	1

A9 is the highest priority, and A1 is the lowest. The encoder is active low, so the complement is taken for the output of the circuit, as in the first input, the output is 9 (1001) but since the encoder is active low, the output is (0110).

3.3.3 Constructing 2-to-4 Line Decoder with Basic Gates

In the same module using block Decoder 1, this circuit was wired. The module is already connected with the power supply, but the inputs and outputs are still not connected. By connecting inputs, A and B to data switches SW0 and SW1, and outputs F1~F4 to logic indicators L0~L3 the circuit in Figure 3.7 below is observed.

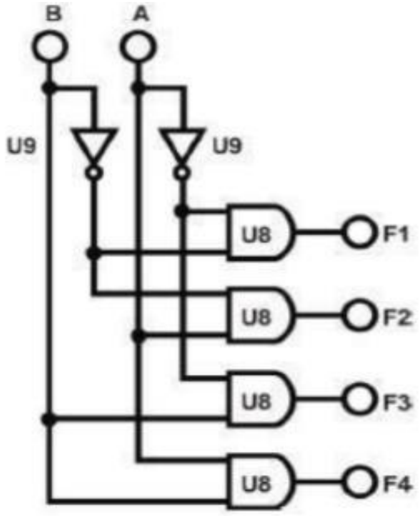
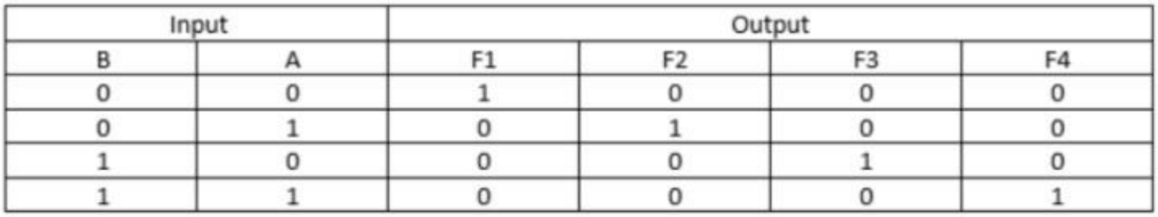


Figure 3.7: 2-to-4 decoder using basic gates

Table 3.3: 2-to-4 decoder truth table



Input		Output			
B	A	F1	F2	F3	F4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

From Table 3.3, the theoretical results of the 2-to-4 decoder are observed. Since the circuit is active high, when the input is 00, the LSB bit in the output is one, while the others are zero. Moreover, when the input is 01, the second output bit is one. The third output bit is one when the input is 10.

And, when the input is 11 the MSB is 1.

3.3.4 Constructing 4-to-10 Line Decoder with TTL IC

Continuing on the same module IT-3004, using U6 (7442) on block decoder 2 this circuit was implemented. Hence, 7442 is a BCD-to-decimal decoder IC. By connecting inputs A, B, C, and D to data switch SW0, SW1, SW2, and SW3 and outputs to logic indicators L0~L9, the circuit in Figure 3.8 is observed.

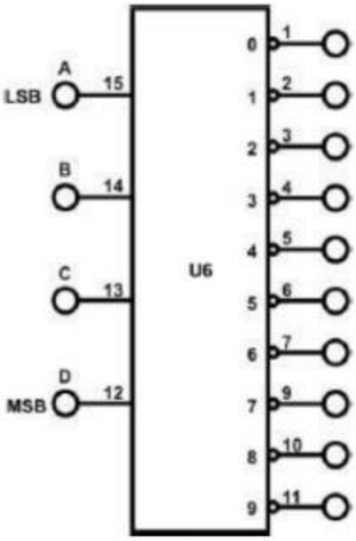
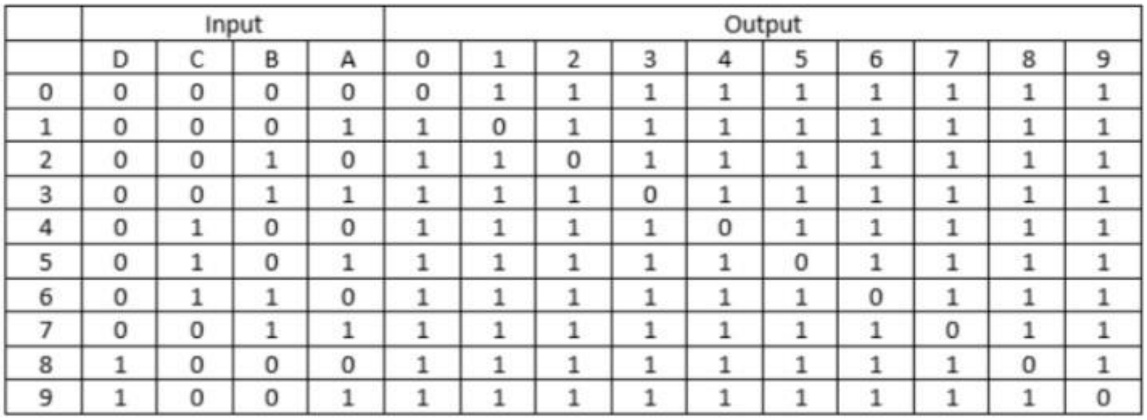


Figure 3.8: 4-to-10 decoder

Table 3.4: 4-to-10 decoder truth table



	Input				Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1	1	1
2	0	0	1	0	1	1	0	1	1	1	1	1	1	1
3	0	0	1	1	1	1	1	0	1	1	1	1	1	1
4	0	1	0	0	1	1	1	1	0	1	1	1	1	1
5	0	1	0	1	1	1	1	1	1	0	1	1	1	1
6	0	1	1	0	1	1	1	1	1	1	0	1	1	1
7	0	0	1	1	1	1	1	1	1	1	1	0	1	1
8	1	0	0	0	1	1	1	1	1	1	1	1	0	1
9	1	0	0	1	1	1	1	1	1	1	1	1	1	0

The circuit is active low, so the output is represented in active low. Starting from 0000, the LSB is 0 and other bits are ones, continuing on the same sequence until reaching the MSB bit when the input is 1111.

3.3.5 Constructing 2-to-1- Line Multiplexer with basic Gates

Using IT-3005 module and block Multiplexer 1 to construct the following circuit which is 2-to-1 MUX. The module was connected to +5V from the power supply, and the inputs A and B were connected to data switches SW0 and SW1, and the selection line C to SW2, while the output F3 is connected to logic indicator L0.

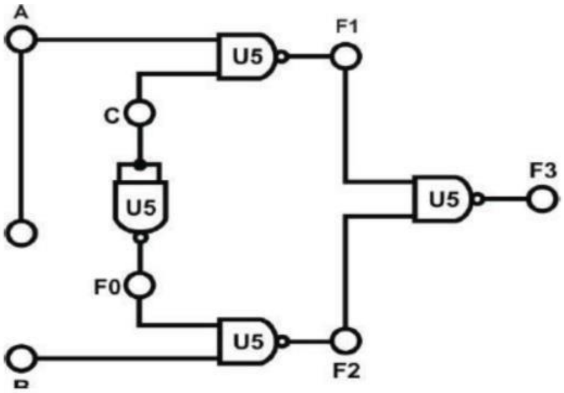


Figure 3.9: 2-to-1 multiplexer

Table 3.5: 2-to-1 multiplexer

Input			Output	
C	A	B	F3	
0	0	0	0	B
0	0	1	1	
0	1	0	0	
0	1	1	1	
1	0	0	0	A
1	0	1	0	
1	1	0	1	
1	1	1	1	

Analyzing the outputs of this MUX, it’s clear that when the selector is 0, the output is the same as state B, also, when the selector is 1, the output is the same as the input A.

3.3.6 Constructing 8-to-1 Line Multiplexer with IC

This circuit can be implemented using U3 (74LS151) on block Multiplexer 2 of the same module (IT 3005). By connecting the inputs D0~D7 to DIP switch 1.0~1.7, and selectors A, B, C to data switches SW0, SW1, and SW2.

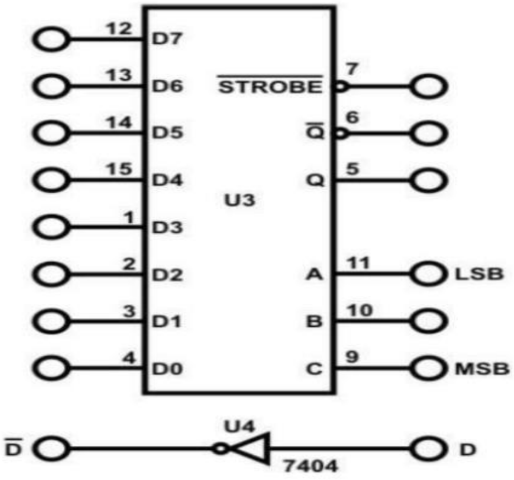
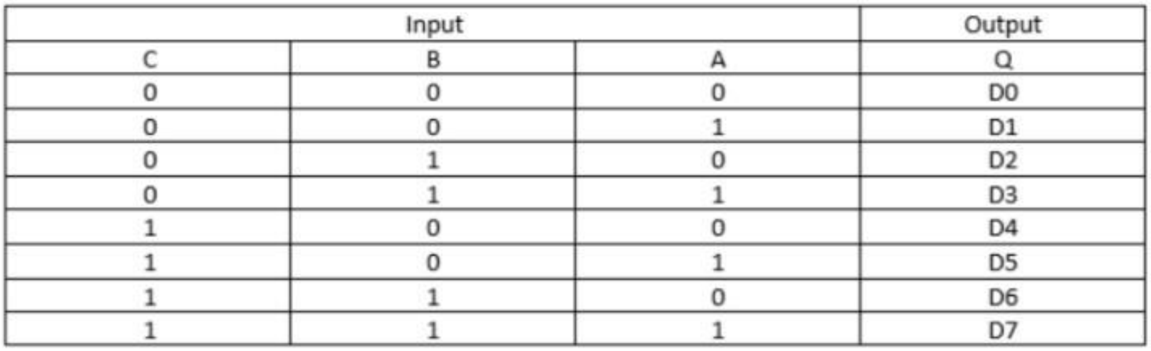


Figure 3.10: 8-to-1 Multiplexer

Table 3.6: 8-to-1 MUX truth table



Input			Output
C	B	A	Q
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

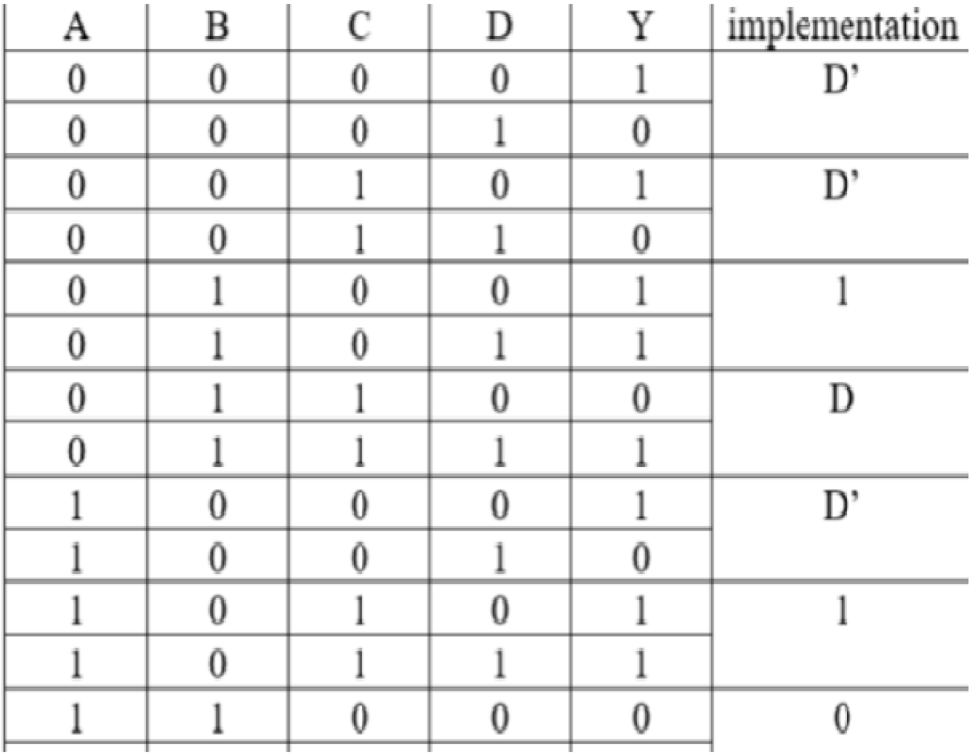
There are 8 different selections, starting from 0 to 7, each selection has its output, when the selection is 0, the output is D0, D0 is an input it may contain 0 or 1, so the output varies. As said before, other selections will have their corresponding output states.

3.3.7 Using Multiplexer to Create a Logic Function

F (A, B, C, D) = Σ (0,2,4,5,7,8,10,11,15)

Since there’s a logic function, firstly, the inputs of the mux must be selected, and then the selection lines must be chosen. To select the inputs of the mux, digital concepts must be used to derive the inputs and selectors. Deriving the truth table of the logic function is like table 3.7 below:

Table 3.7: F (A, B, C, D) truth table



A	B	C	D	Y	implementation
0	0	0	0	1	D’
0	0	0	1	0	
0	0	1	0	1	D’
0	0	1	1	0	
0	1	0	0	1	1
0	1	0	1	1	
0	1	1	0	0	D
0	1	1	1	1	
1	0	0	0	1	D’
1	0	0	1	0	
1	0	1	0	1	1
1	0	1	1	1	
1	1	0	0	0	0

Choosing A, B, and C to be selectors, each state will be repeated twice, so each state will be represented using input D, or 1, or 0 depending on the output Y. The results are obtained above.

In the lab, the circuit was implemented using Module IT-3005 and using Multiplexer 2 block.

3.3.8 Constructing 1-to-2 Line Demultiplexer with Basic Logic Gates

The demultiplexer is implemented the same way as 2-to-1 MUX, but B is connected with input A, so the circuit is changed to one input which is A.

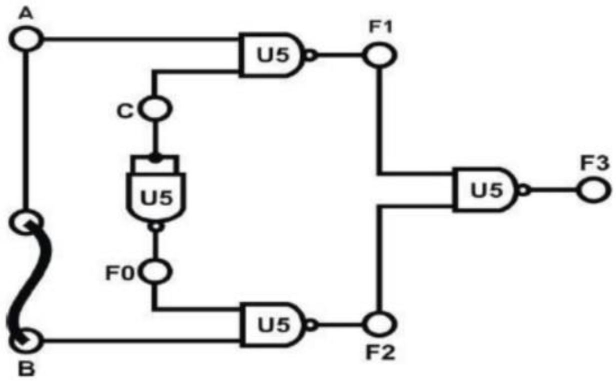


Figure 3.11: 1-to-2 Demultiplexer with basic logic gates

Meanwhile, when A is 0, and C is 0 or 1, the output F1 and F2 are the same, F1 = F2 = 1, If A = 1, C = 1, then F1 = 0, F2 = 1, also when A = 1, C = 0, then F1 = 1, F2 = 0.

Table 3.8: 1-2 Line Demultiplexer with basic logic gate truth table

C	A	F1	F2
0	0	1	1
0	1	1	0
1	0	1	1
1	1	0	1

3.3.9 Constructing 1-to-8 Line Demultiplexer with CMOS IC

The block in the Figure 14 called De-multiplexer 4051(U6) lied on (IT-3005 block De-multiplexer 2)

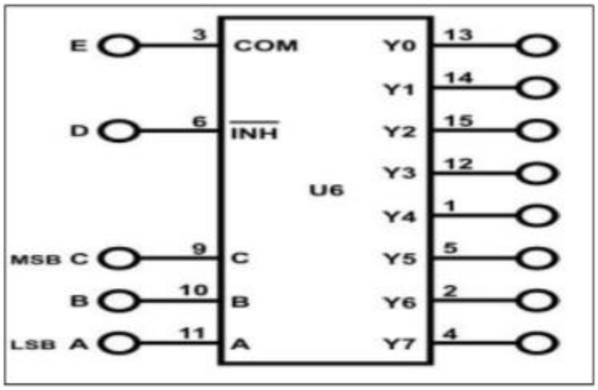
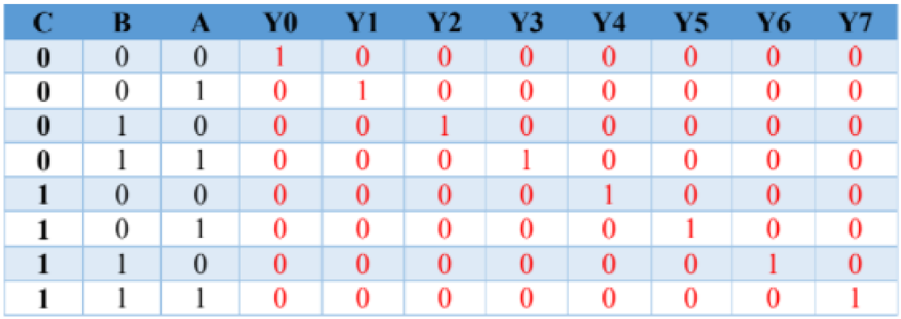


Figure 3.12: 1-to-8 Line Demultiplexer with CMOS IC

The selection A,B,C lines was connected to SW0,SW1,SW2 ,this de-Mux has active low enable so the output observed when D=0, the output was recorded in Table 9

Table 3.9: Demultiplexer with CMOS IC truth table



C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

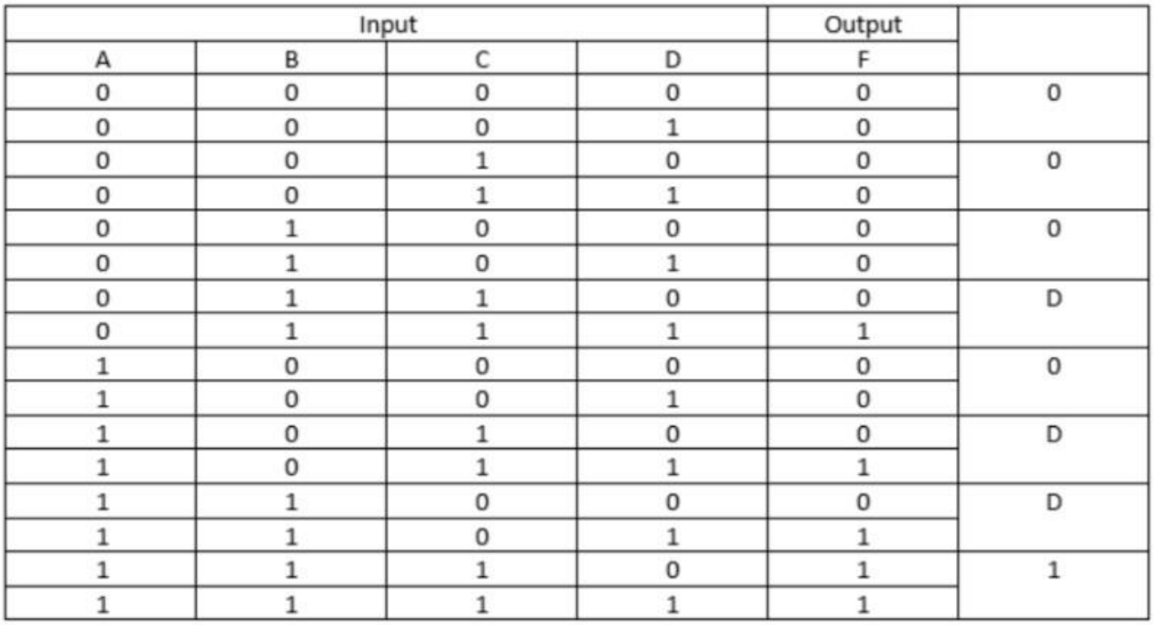
3.4 Post Lab

Using two multiplexers, a circuit takes 4 inputs and one output, it’s active high one three or four inputs are active high. Since the circuit has 1 as output when the output has 3 or 4 ones, then the function of the circuit is all numbers that have 3 or 4 bits which are, 7, 11, 13, 14, 15, so F is written as follows:

F (A, B, C, D) = Σ (7, 11, 13, 14, 15)

So, to design this circuit, we must derive the truth table firstly.

Table 3.10: System truth table



Input				Output	
A	B	C	D	F	
0	0	0	0	0	0
0	0	0	1	0	
0	0	1	0	0	0
0	0	1	1	0	
0	1	0	0	0	0
0	1	0	1	0	
0	1	1	0	0	D
0	1	1	1	1	
1	0	0	0	0	0
1	0	0	1	0	
1	0	1	0	0	D
1	0	1	1	1	
1	1	0	0	0	D
1	1	0	1	1	
1	1	1	0	1	1
1	1	1	1	1	

Since there are two multiplexers, then there are 2 inputs as selection lines. So, the MSB bit is used as enable to the two muxes, while B and C are selectors, and D is used as input in the two muxes.

A is used as enable, therefore, it has two values 0 and 1, when A is 0 the first MUX is activated, and when A is 1 the second MUX is activated.

Table 3.11: MUX1 truth table

Enable	Selectors		Input
A	B	C	F
0	0	0	0
0	0	0	
0	0	1	0
0	0	1	
0	1	0	0
0	1	0	
0	1	1	D
0	1	1	

Table 3.12: MUX2 truth table

Enable	Selectors		Input
A	B	C	F
1	0	0	0
1	0	0	
1	0	1	D
1	0	1	
1	1	0	D
1	1	0	
1	1	1	1
1	1	1	

Now, The enable of this component is active low, so it takes the complement of the input, hence MUX1 enable is A, and MUX2 enable is A'. Hence, when A = 0, the second MUX is enabled because A' = 1 and the enable is (A')' which is 0. Moreover, when A = 1, the enable is (A)' = 0 so the first MUX is enabled.

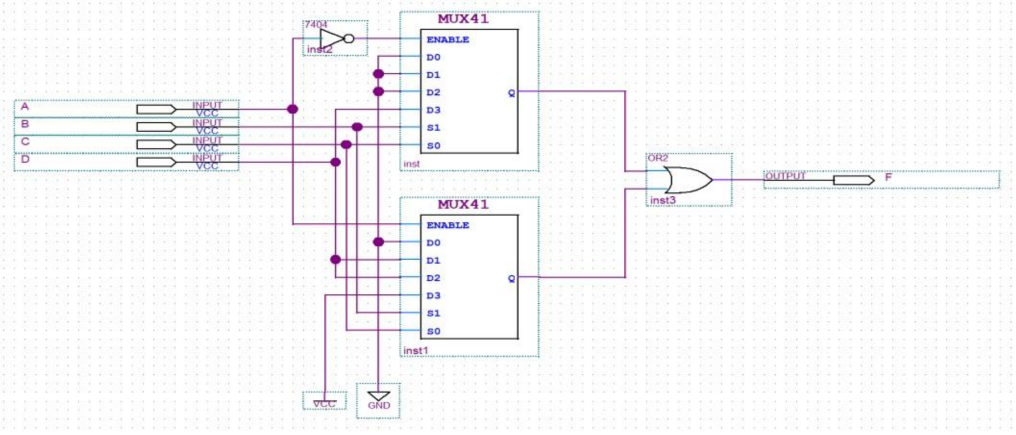


Figure 3.13: Whole system circuit

3.5 Conclusion

To conclude, the aim of this experiment is achieved. Four types of combinational circuits are learned which are decoders, encoders, multiplexers, and demultiplexers. During the experiment, we knew how to use Modules and how to construct these circuits using two modules IT-3004 and IT-3005. Encoder, decoder, MUX, and DEMUX were implemented using both basic gates and ICs. And, we achieved that encoders perform the reverse operation of the decoder and the demultiplexer performs the reverse operation of the multiplexer.

3.6 References

[1] https://www.geeksforgeeks.org/encoder-in-digital-logic/

[2]https://www.tutorialspoint.com/digital_circuits/digital_circuits_decoders.htm#:~:text=Decoder%20is%20a%20combinational%20circuit,decoder%20detects%20a%20particular%20code

[3] https://www.geeksforgeeks.org/multiplexers