Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Digital Lab (ENCS2110)

Experiment No.5 Pre-Lab

Title: Sequential Logic Circuits

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Design the Logic Diagram, function table of the SR latch using NOR gates, and explain how it works

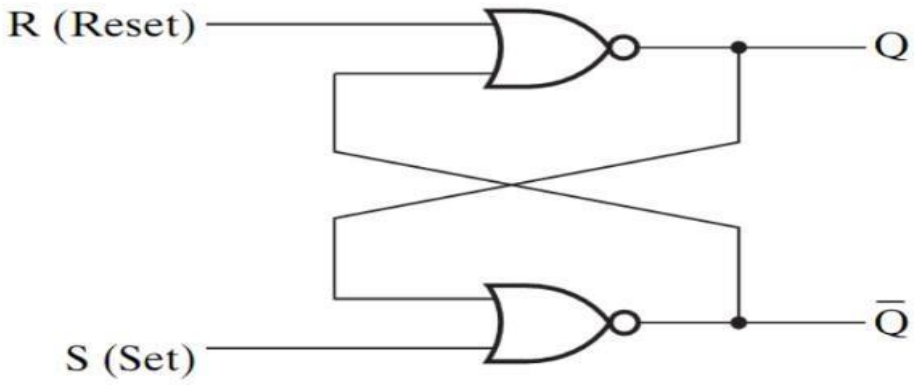

Figure 1.1:SR latch with NOR gates (Logic diagram)

Table1.1:Function table

S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	Undefined

- If S = 1 and R = 0 then Set (Q = 1, Q = 0)
- If S = 0 and R = 1 then Reset (Q = 0, Q = 1)
- When S = R = 0, Q and Q are unchanged
- The latch stores its outputs Q and Q as long as S = R = 0
- When S = R = 1, Q and Q are undefined (should never be used)