Faculty of Engineering & Technology
Electrical & Computer Engineering Department

Digital Electronics and Computer Organization Lab ENCS 2110
Report #3

Experiment No. 7 - Constructing Memory Circuits Using Flip−Flops

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7.1 Abstract

The experiment aims to study Random Access Memory (RAM), understand the basic structure of RAM, implement it using D flip-flops or pre-implemented IC\chip, and to understand and test 64-bit RAM and its functionalities using Proteus.

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7.2 Theory

When data is manipulated using the computer, the results are temporarily stored in RAM, Random access memory, to be used later.

RAMs are memory storage for the data. It's implemented using registers that are previously constructed using flip-flops. As mentioned in previous experiments, registers are used to store data, so they are the perfect IC to be used in RAMs.

7.2.1 Building RAM with a D flip-flop

There are two various types of the basic structure for RAM, one has dependent input and output, and the second has independent input and output. Both represent the RAM and work the same.

7.2.1.1 1-bit and 4-bit RAMs

These two circuits are implemented using the structure of dependent input and output. Regarding Figure 7.1 (a), the W/R terminal is W for writing/input, R for reading/output, and enable terminal where both are control terminals.

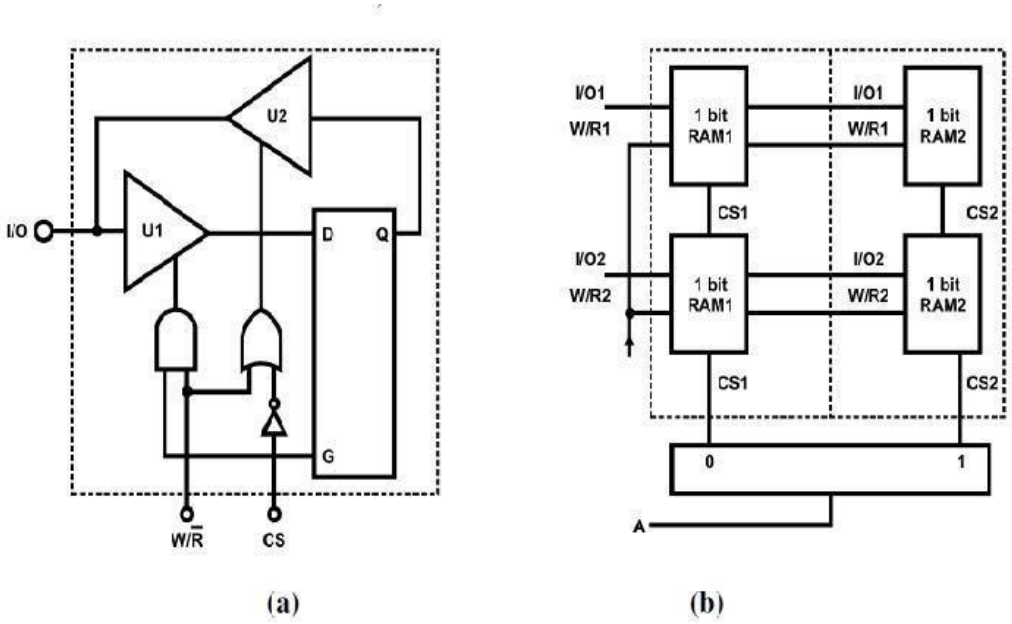


Figure 7.1: (a) 1-bit RAM circuit, (b) 4-bit RAM circuit

Circuit (a) performs only when CS is 1 (enabled), otherwise, it's not. By using the control terminals, different operations can be done upon this circuit such as reading/writing from or to memory.

It's known that the use of memory is increasing, and applications need larger memory capacities. So, Figure 7.1 (b) demonstrates how to increase the capacity of the RAM up to 4-bits.

7.2.1.2 2-bit RAM

This circuit is a 2-bit RAM, as mentioned in the title. This circuit is implemented using dual D flipflops and other basic gates. This circuit is input and output independent.

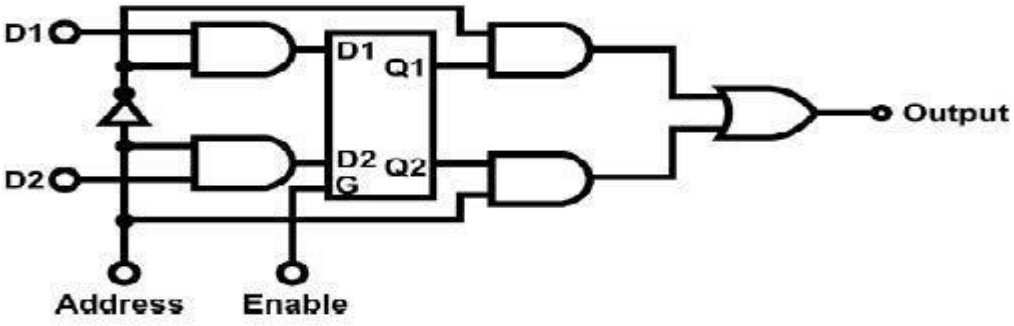


Figure 7.2: 2-bit RAM circuit

This circuit has an address that selects which input is going to be stored in the output, so that the value of D1 is selected if D1 is 0, by the same way D2 is moved to the output if the address is 1. The enable terminal enables the flip-flop to operate.

7.2.2 Implementation of the two-bit memory presented in Figure 7.1 (a)

Commercial random-access memories may have a capacity of thousands of words and each word may range from. The logical construction of a large capacity memory would be a direct extension of the configuration as shown in Figure 7.3. The two address inputs go through a 2x4 decoder to select one of the four words.

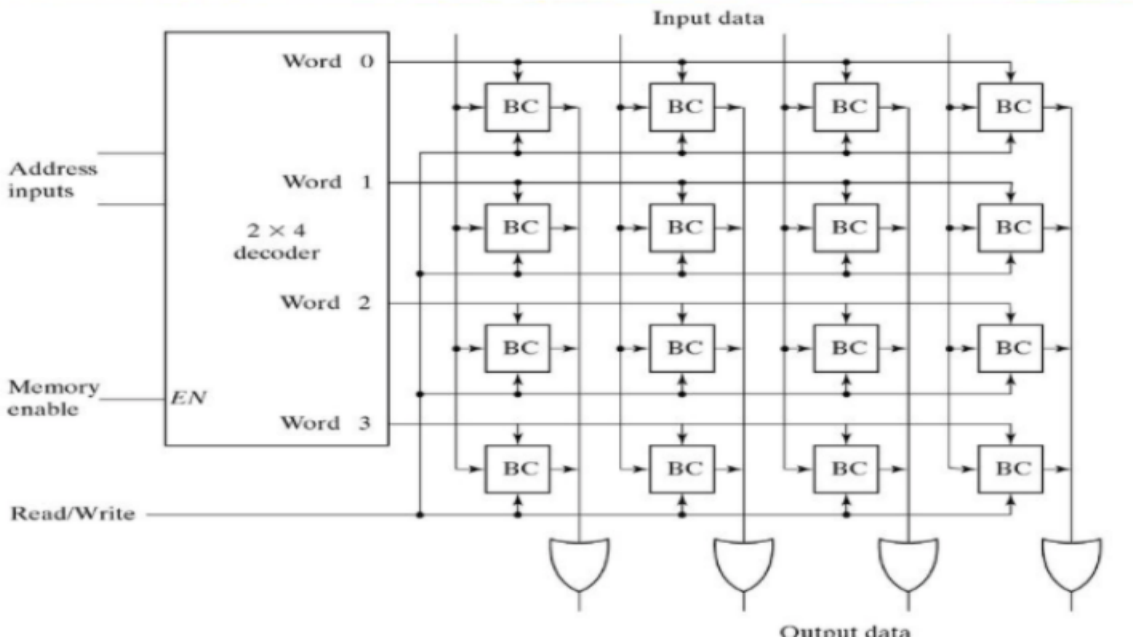
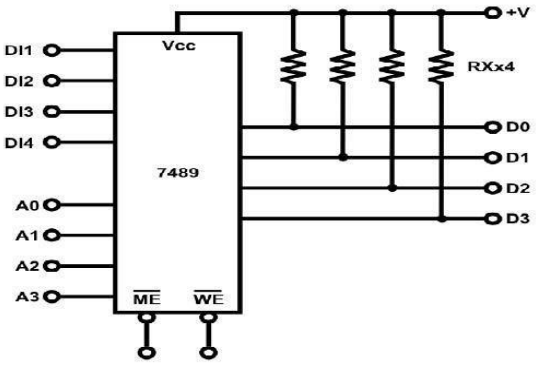


Figure 7.3. Logical construction of a 4x4 RAMS

7.2.3 64-bit RAM

RAM is a memory element, like ROM. The capacity of the RAM can be determined by the number of data variations and number of locations. If there are 4 data and 4 address lines, then there are 2^4 or 16 locations. So, each 4-bits can be stored in one of the 16 locations. Hence, the capacity is 4*16 which is 64 bits. This chip can be used in implementing larger RAMs such as 256-bits.



$\overline{ME}$	$\overline{WE}$	
0	0	Write
0	1	Read
1	0	Inhibit storage
1	1	Do nothing

Figure 7.4: 4-bit RAM circuit and truth table

According to the truth table, this RAM has four operations which are write, read, inhibit storage (delete the stored value) and do nothing (stores the previous output).

When ME' = 0 and WE' = 0, the memory is enabled, and the input process starts. The input and output terminals are separated. The output terminals are open-collector type so resistors “RX×4” must be addedto the supply voltage. Since the output terminal of 7489 is open-collector type, the outputs can be connected in parallel, as shown in Figure 7.4. The operating sequence will be controlled by ME' and WE'. When A4A5=00, A is selected, ME' and WE' of B, C and D all equal to “1”. Similarly, when A4A5=01, B is selected, ME' and WE' of C and D all equal to “1”. E is 2-4 decoders with “0” as its output. The unselected outputs are in high or “1” state. Since the outputs will have high impedance when ME' and WE' are both “1”, each R/W' control of 7489 are connected to an OR gate to ensure that when ME' = “1”, WE' will be equal to “1” too. When ME' = “0”, WE' is controlled by external R/W' control so that the “READ” operation is performed if R/W'= “1”. The “WRITE” operation is performed when R/W'= “0”. The 7488 is a 256-bit open-collector ROM which has similar structure as the 7489. Their methods of expansion are similar as well.

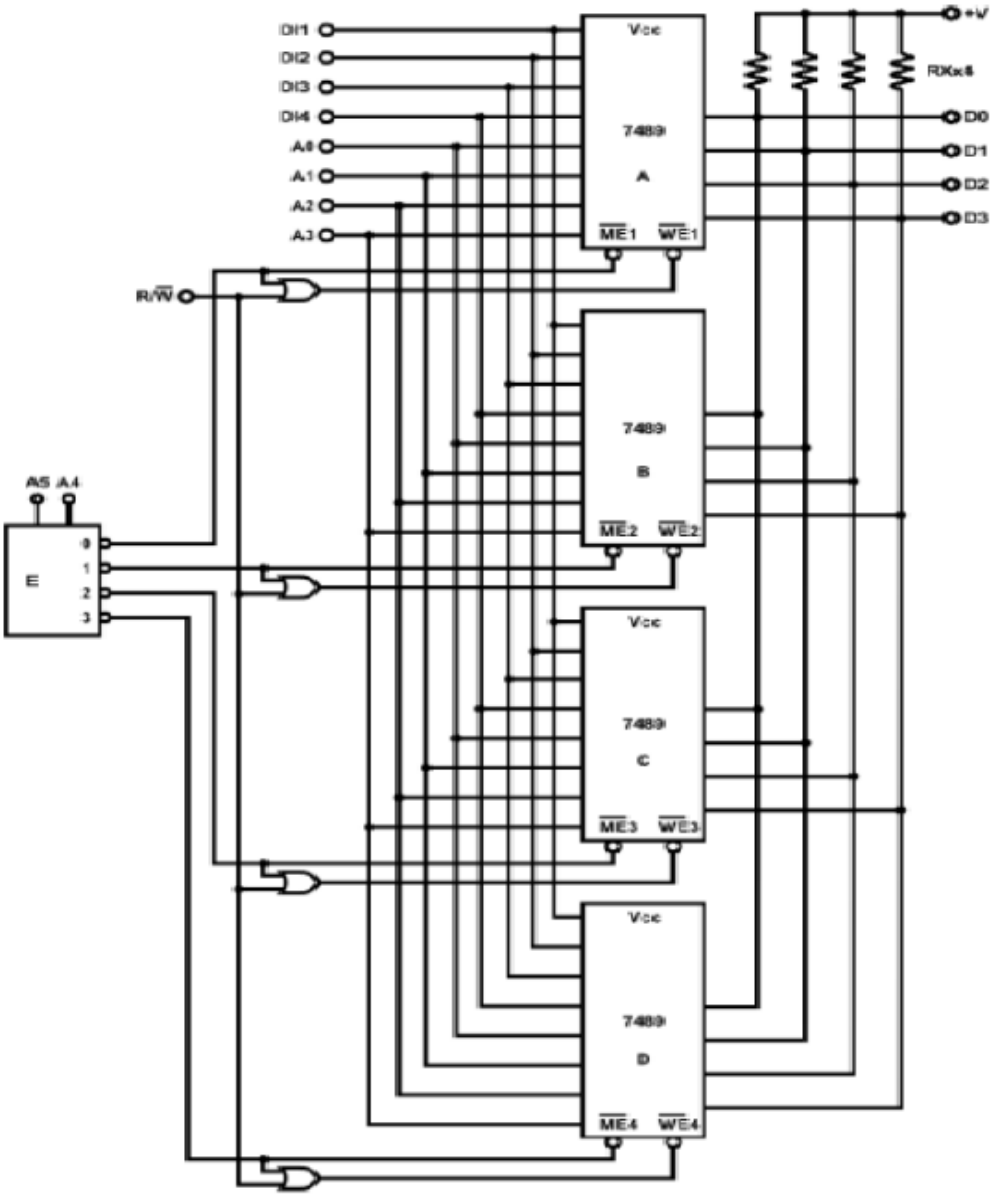


Figure 7.5. Logical construction of a 6x4 RAM using four 4x4 RAMS

7.3 Procedure & Discussion

7.3.1 2-bit RAM using D flip-flop

This circuit was implemented using basic gates, AND, NAND, and two D flip-flops. It was wired to represent a 1-bit RAM using Proteus.

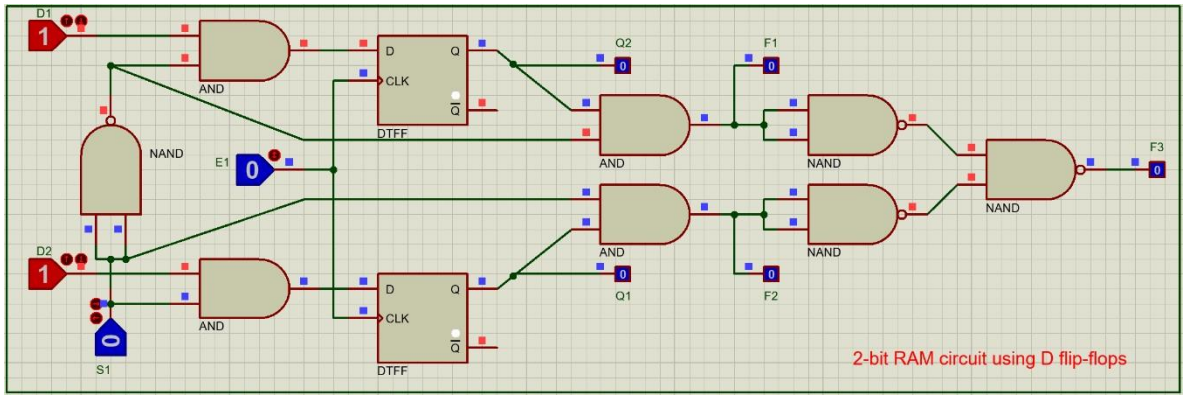


Figure 7.6: 2-bit RAM using D flip-flop circuit

Table 7.1: 2-bit RAM using D flip-flop truth table

Input				Output		
E1	S1	D2	D1	F3	F2	F1
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	0	0	0
1	0	0	1	1	0	1
1	0	1	0	0	0	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	1	1	0
1	1	1	1	1	1	0

First of all, the circuit proceeds to work only when it's enabled aka when E1 is one, otherwise there's no output. Whenever the circuit is enabled, the output of the ram changes depending on the selected flip-flop according to S1. When S1 is 0, the upper D flip-flop is selected, and the input of it is moved to the output without any changes. And, when S1 is 1, the output of this circuit is the same as in the input of the bottom D flip-flop.

7.3.2 64-bit RAM

This RAM was implemented using a 7489 chip to perform the circuit operations and light indicators were used to indicate the status of the output and to realize how the circuit works.

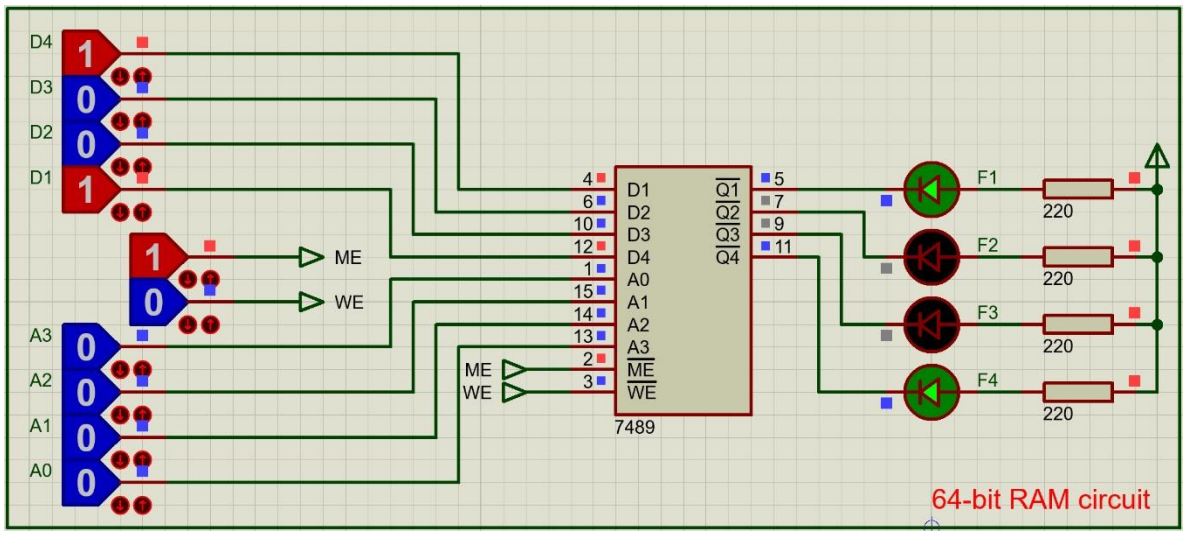


Figure 7.7: 64-bit RAM circuit

Table 2: 64-bit RAM truth table

Address				Write						Read					
A3	A2	A1	A0	ME	WE	D4	D3	D2	D1	ME	WE	F4	F3	F2	F1
0	0	0	0	↓	0	0	0	0	0	↑	1	0	0	0	0
0	0	0	1	↓	0	0	0	0	1	↑	1	0	0	0	1
0	0	1	0	↓	0	0	0	1	0	↑	1	0	0	1	0
0	0	1	1	↓	0	0	0	1	1	↑	1	0	0	1	1
0	1	0	0	↓	0	0	1	0	0	↑	1	0	1	0	0
0	1	0	1	↓	0	0	1	0	1	↑	1	0	1	0	1
0	1	1	0	↓	0	0	1	1	0	↑	1	0	1	1	0
0	1	1	1	↓	0	0	1	1	1	↑	1	0	1	1	1
1	0	0	0	↓	0	1	0	0	0	↑	1	1	0	0	0
1	0	0	1	↓	0	1	0	0	1	↑	1	1	0	0	1
1	0	1	0	↓	0	1	0	1	0	↑	1	1	0	1	0
1	0	1	1	↓	0	1	0	1	1	↑	1	1	0	1	1
1	1	0	0	↓	0	1	1	0	0	↑	1	1	1	0	0
1	1	0	1	↓	0	1	1	0	1	↑	1	1	1	0	1
1	1	1	0	↓	0	1	1	1	0	↑	1	1	1	1	0
1	1	1	1	↓	0	1	1	1	1	↑	1	1	1	1	1

As required, the value of the input is the same as its address. The most two used controls are reading and writing which is seen in the table above. These two operations were performed on the circuit and it's obvious that it worked as it must.

7.4 Conclusion

To conclude, in this experiment we understood the detailed implementation of RAMs and we knew that flip-flops are the main part of RAMs. During the experiment, we constructed various types of RAMs (2-bit, 64-bit, and 256-bit RAMs) using Proteus. Each RAM output was compared to its theoretical part, the results were fitted perfectly. Also, we knew how to size the memory up by using more flip-flops or 64-bit RAM chips. Finally, we saw practically how data are read or stored to/from memory which was very helpful.

7.5 References

1.Electrical and Computer Engineers Department, Digital lab Manual

2. https://www.techtarget.com/searchstorage/definition/RAM-random-access-memory