Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Digital Lab (ENCS2110)

Experiment No.8 Pre-Lab

Title: Introduction to QUARTUS Software

Prepared by:

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Section: 2

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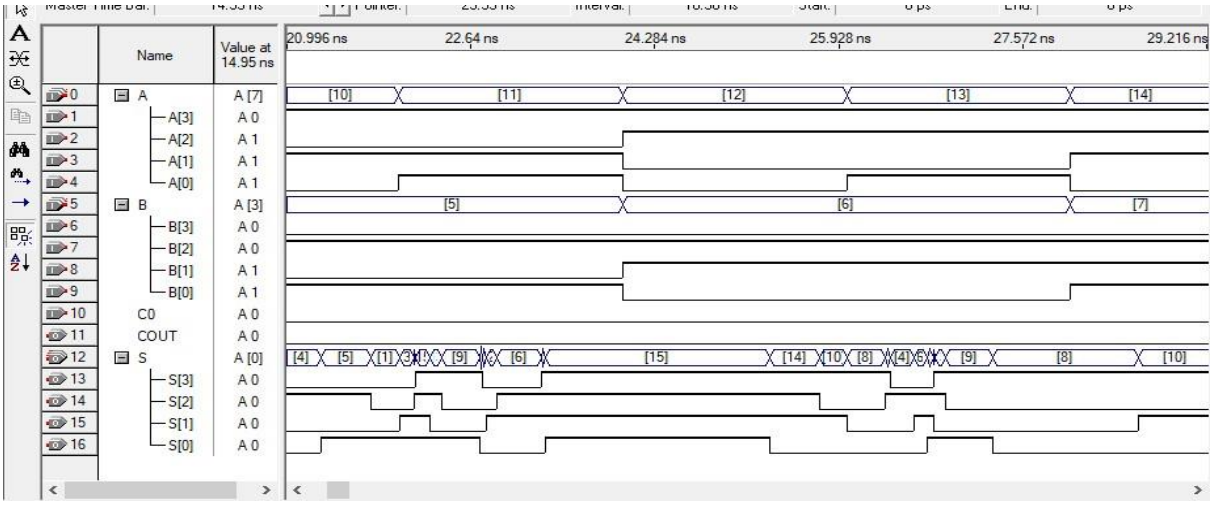
1) HDL Code for 4-bit adder

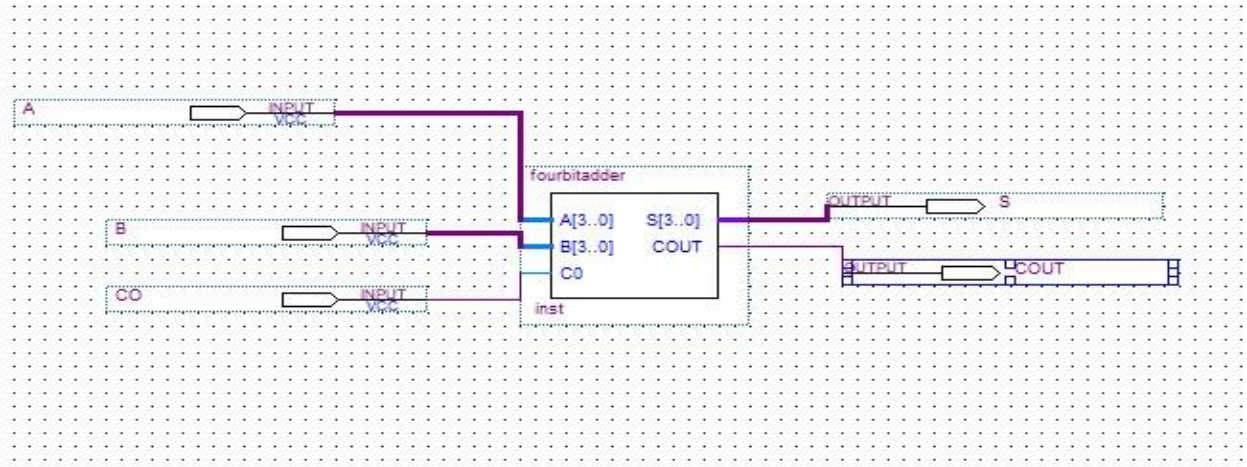
- Verilog code:

```
module fourbitadder(A,B,C0,S,COUT);
input [3:0] A,B;
input C0;
output [3:0]S;
output COUT;
assign {COUT,S} = A+B+C0;
endmodule
```

- Wave Form:



- Block Diagram:



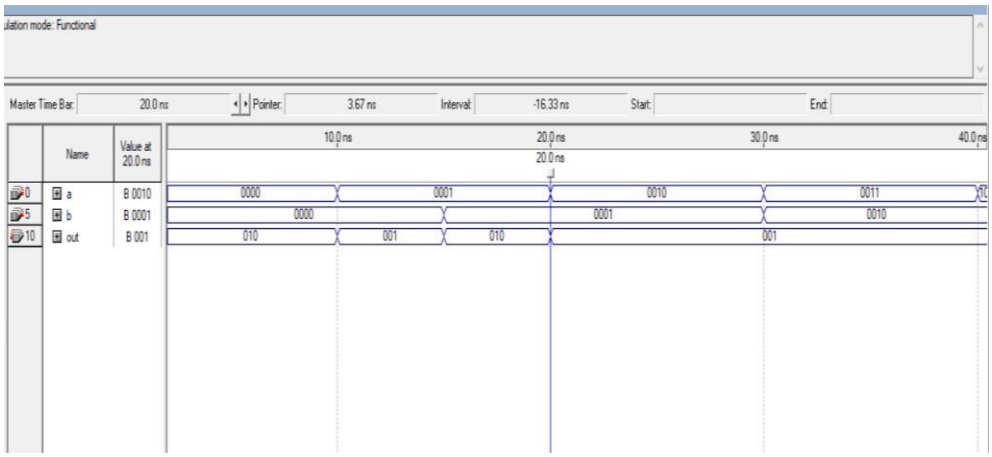
2) 4bit-comparator

- Verilog code:

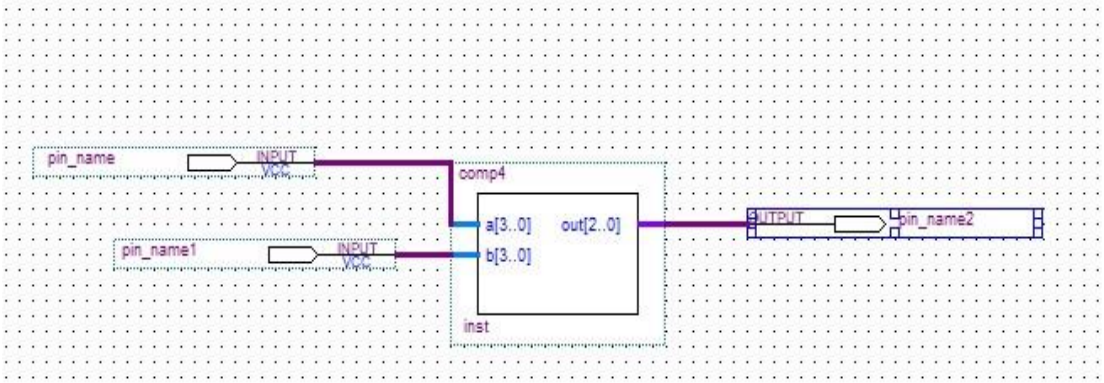
comp4.v | Compilation Report - Flow Summary

```
1  module comp4(a,b,out);
2   input [3:0] a,b;
3   output [2:0] out;
4   reg [2:0] out;
5   always @(a,b)
6   if(a>b)
7  begin
8   out =3'b001;
9   end
10  else if (a<b)
11 begin
12  out = 3'b100;
13  end
14  else
15 begin
16  out = 3'b010;
17  end
18  endmodule
19
```

- Wave Form:

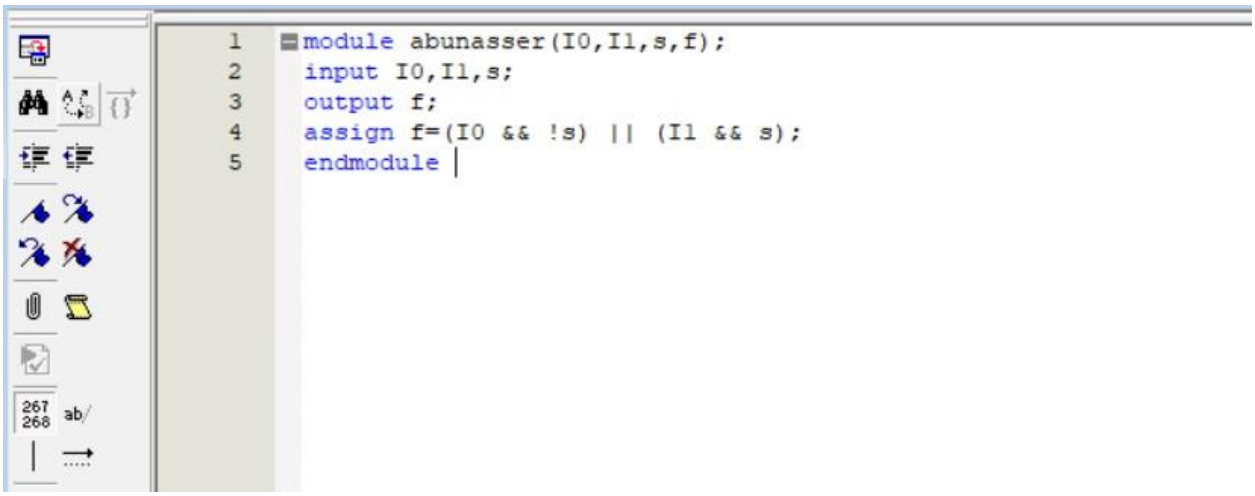


- Block Diagram:



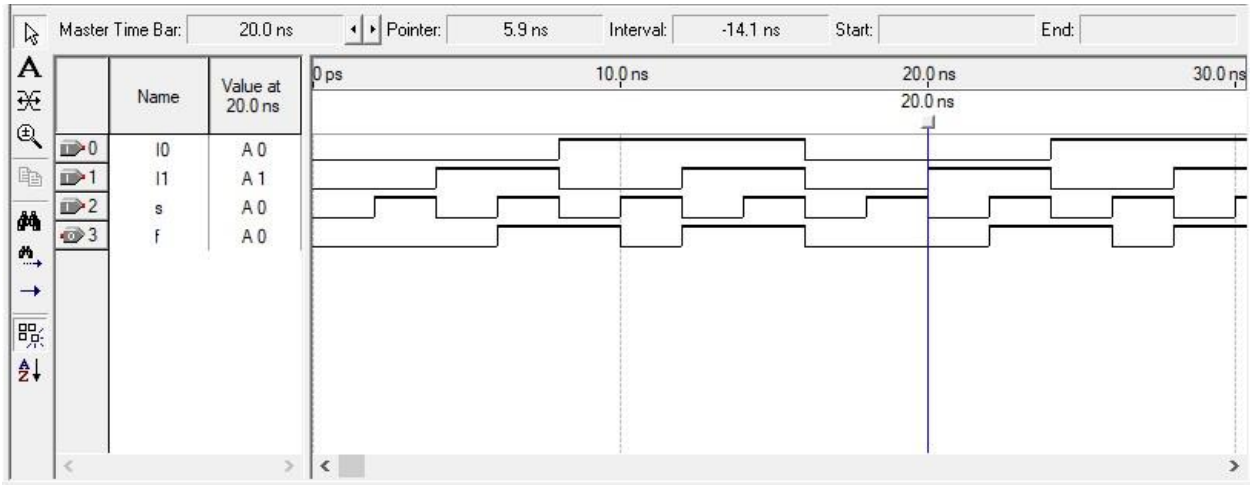
3) HDL Code of 2x1 MUX :

- Verilog code:



```
1  module abunasser(I0,I1,s,f);
2  input I0,I1,s;
3  output f;
4  assign f=(I0 && !s) || (I1 && s);
5  endmodule
```

- Wave Form:



- Block Diagram: