I2S TX Specification

MIRIAM ASH

29/05/2024

Table of contents

Introduction

The I2S (Inter-IC Sound) transmitter module supports the original two-channel I2S format. this I2S transmitter follows the I2S bus protocol and has an audio stream transmit function.

I2S transmitter allows serial streaming communication between the host MCU and various peripheral devices. It uses only three external signal pins.

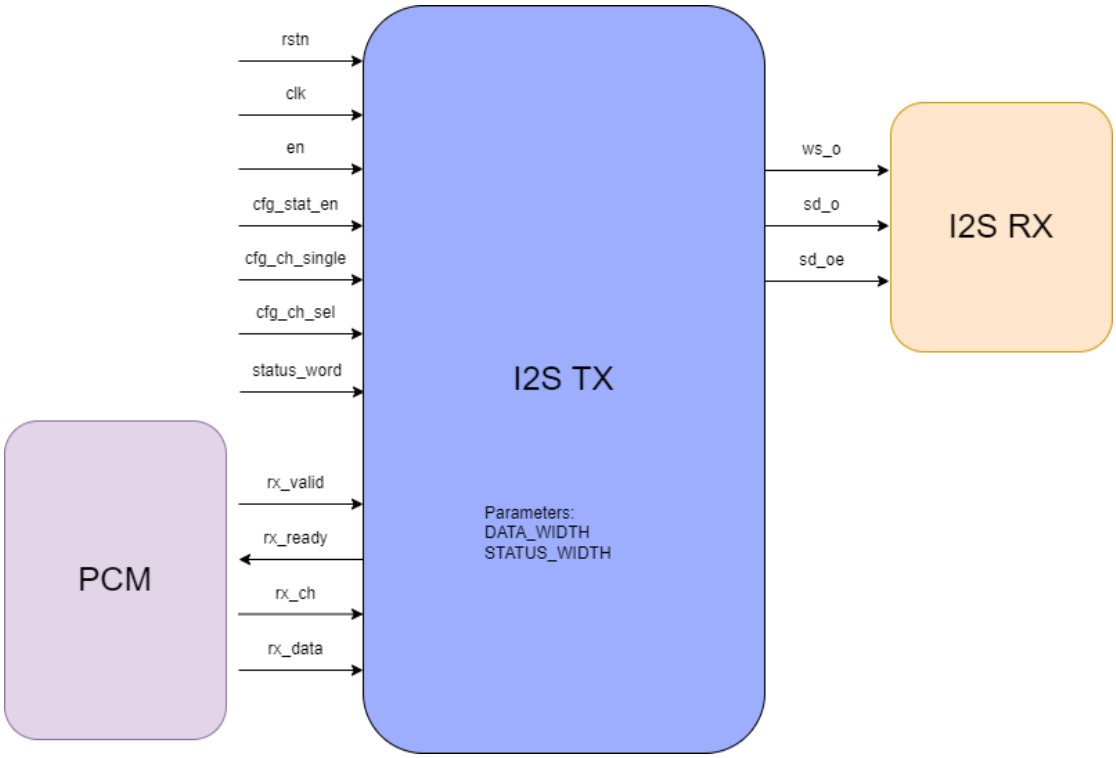
Reference

The following standards and specifications contain provisions, which through reference in this document constitute provisions of this specification. All the standards and specifications listed are normative references. At the time of publication, the editions indicated were valid.

I2S - web.archive.org/web/20070102004400/http://www.nxp.com/acrobat_download/various/I2SBUS.pdf

AXI4-STREAM - zipcpu.com/doc/axi-stream.pdf

I2S TX Interface



Parameters

Name	Default Value	Description
DATA_WIDTH	24	Data width for audio payload
STATUS_WIDTH	8	Status word width

Ports

Name	Dir	Width	Description
System signals			
clk	in	1	Master clock signal
rstn	in	1	Asynchoronous Reset (active low level)
en	in	1	Enable signal
I2S signals			
sd_o	out	1	I2S data output
sd_oe	out	1	I2S data output enable
ws_o	out	1	I2S word select output
PCM interface			
rx_data	in	DATA_WIDTH	PCM data
rx_valid	in	1	PCM valid
rx_ch	in	1	PCM channel marker: 0 - Left; 1 - Right
rx_ready	out	1	PCM ready data

Configuration			
cfg_ch_single	in	1	Channel mode: • 0 - dual channel mode • 1 - single channel mode
cfg_ch_sel	in	1	Select channel for single channel mode: • 0 - select left channel • 1 - select right channel
cfg_stat_en	in	1	Enable sending the status word: • 0 - normal work • 1 - send status word in bits[N-1:0] of output word
status_word	in	STATUS_WIDTH	Status word for I2S inband payload

I2S TX Behavior

The main use case for I2S transmitter is emulating signal from MEMS microphones and transmit its. The I2S transmitter can acts as a I2S master (provider the SCK and WS signals) or as a I2S slave (consumer the SCK and WS signals).

The Over Sampling Rate is fixed at 64 therefore the WS signal must be SCK/64 and synchronized to the SCK.

I2S transmitter Configuration Guidelines for the MEMS microphone mode:

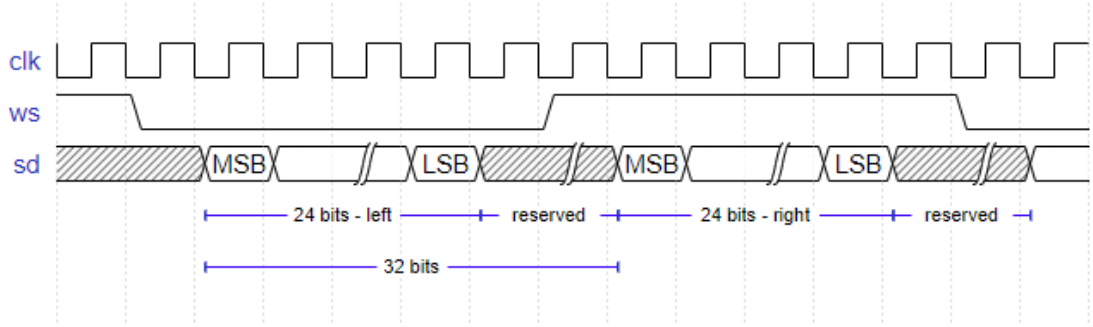
• The Data Format is 24 bit, 2's compliment, MSB first

• The Data Precision is 18 or 24 bits (unused bits are used for Status word if required)

• The mode must be I2S with MSB delayed 1 SCK cycle after WS changes

• WS must be SCK/64

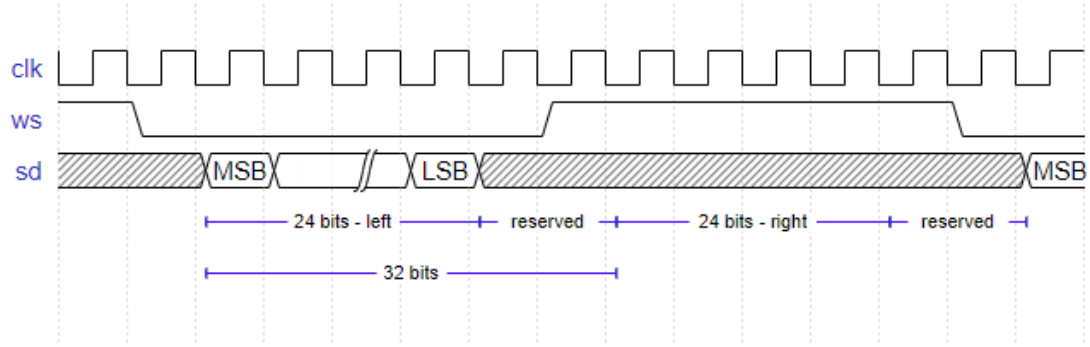
• MSB of each data word is delayed by one SCK cycle from the start of each half-frame



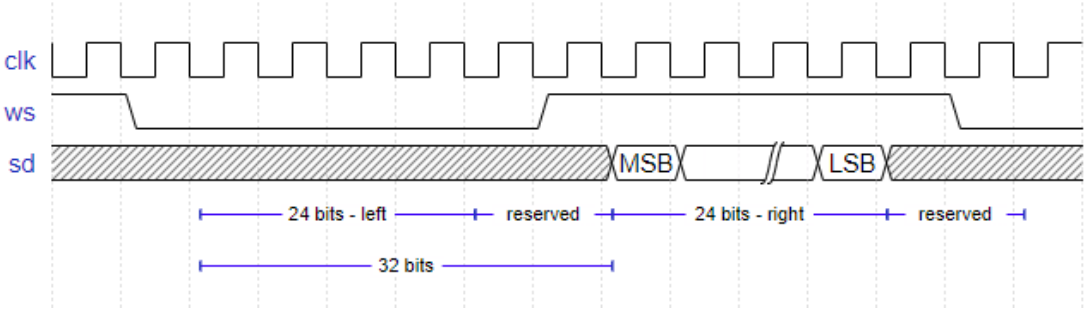
Single Channel mode

The format of a I2S data stream can be stereo, mono left and mono right. Following figures show the formats of mono data stream for left and right channels' sources, respectively.

Example for cfg_ch_single=1, cfg_ch_sel=0:



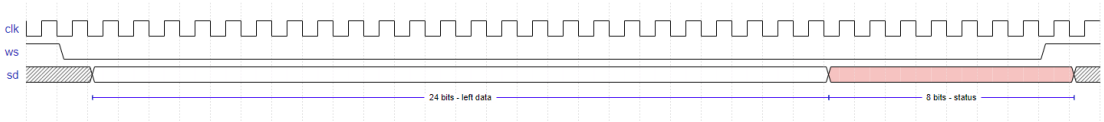
Example for cfg_ch_single=1, cfg_ch_sel=1:



Status Configuration

cfg_stat_en enable sending the status word:

- 0 - normal work (no status word sends)
- 1 - send status word in bits[N-1:0] of output word



PCM Interface

The I2S transmitter module uses data stream protocol very similar to the AXI-Stream protocol for transfering all internal data streams. The data streams transfered in parallel form (N-bits data using N-bits bus for transfering).

The prefixes used for:

- The prefix rx used for all signals of incoming data streams
- The prefix tx used for all signals of outcoming data streams

The suffixes used for the data streams are follow:

- data[N-1:0] – data payload (similar to TDATA from AXI-Stream)
- valid – stream handshake: validity signal (indicates that the master is driving a valid transfer) (similar to TVALID from AXI-Stream)
- ready – stream handshake: readyness signal (indicates that the slave can accept a transfer in the current cycle) (similar to TREADY from AXI-Stream)
- ch – channel marker for stereo mode; don't care for mono mode (similar to TID from AXI-Stream)

A transfer takes place only when both valid and ready are asserted.

The valid and ready handshake determines when information is passed across the interface. A two-way flow control mechanism enables both the master and slave to control the rate at which the data and control information is transmitted across the interface. For a transfer to occur both the valid and ready signals must be asserted.

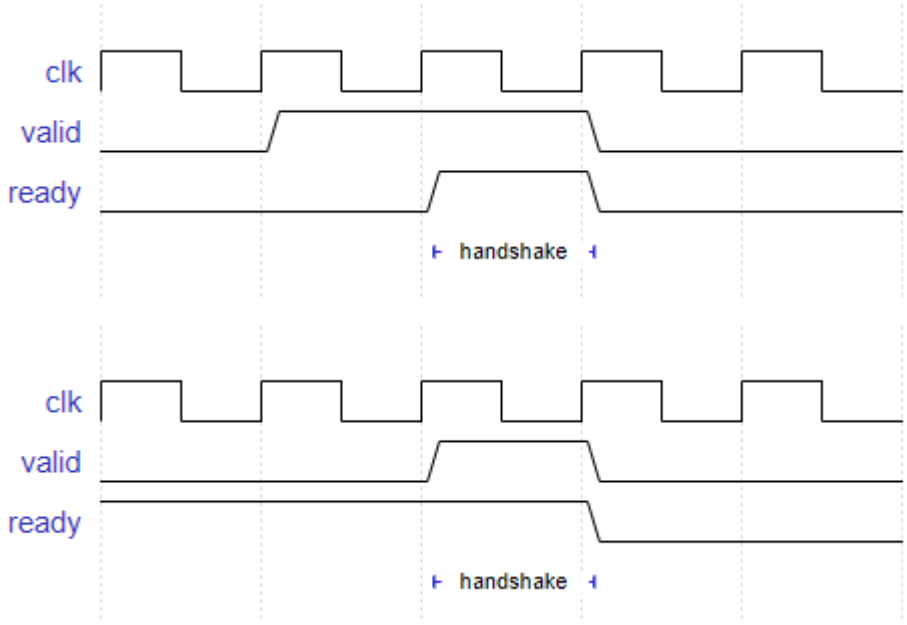
Either valid or ready can be asserted first or both can be asserted in the same clk cycle.

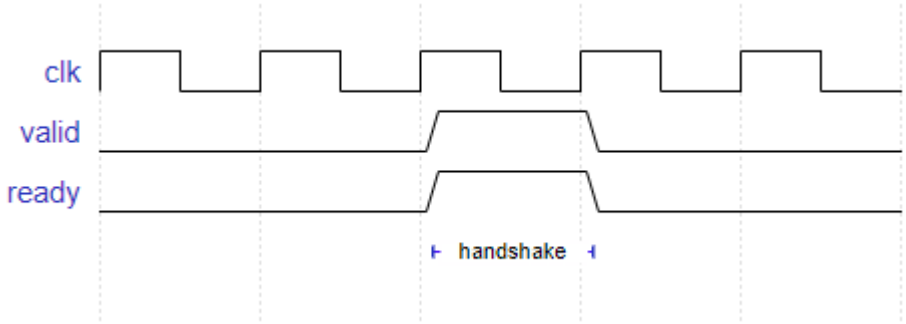
A master is not permitted to wait until ready is asserted before asserting valid. Once valid is asserted it must remain asserted until the handshake occurs.

A slave is permitted to wait for valid to be asserted before asserting the corresponding ready.

If a slave asserts ready, it is permitted to deassert ready before valid is asserted.

Examples for 3 possible conditions:




clk
valid
ready
handshake