Lab 5 Report

Name:

UT EID:

Section:

Checklist:

Part 1 –

   i.   Design file (.v) for the Ripple Carry Adder

  ii.   Test-bench

 iii.   Complete Table 1 from the simulation

A[3:0]	B[3:0]	Cin	Sum[3:0]	Cout
0001	0101	0	?	?
0111	0111	0	?	?
1000	0111	1	?	?
1100	0100	0	?	?
1000	1000	1	?	?
1001	1010	1	?	?
1111	1111	0	?	?

Table 1. Testcases for Ripple Carry Adder Verification

  iv.   Constraints File (Just the uncommented portion)

   v.   Simulation waveform for the above test-cases

Part 2 –

  vi.   All the equations for C_i's and S_i's

 vii.   Design files (.v) for the Carry Lookahead Adder and Register Logic

viii.   Test-bench

  ix.   Complete Table 2 from the simulation

A[3:0]	B[3:0]	Cin	Sum[3:0]	Cout
0000	0101	0	?	?
0101	0111	0	?	?
1000	0111	1	?	?
1001	0100	0	?	?
1000	1000	1	?	?
1101	1010	1	?	?
1110	1111	0	?	?

Table 2. Testcases for Carry Lookahead Adder Verification

    x.   Constraints File (Just the uncommented portion)

    xi.   Simulation waveform for the above test-cases

Part 3 –

  xii.   Screenshots of the gate-level schematics for both the adder techniques

 xiii.   Delay and area for both the adder techniques showing all the work

 xiv.   Brief conclusion regarding the pros and cons of each of the techniques

***Note* –>** *The Verilog codes and the uncommented portions of the constraint files should be copied in your lab report and the **actual Verilog (.v), Constraint (.xdc) files and Bitstream (.bit) files** need to be zipped and submitted as well on Canvas. You are not allowed to change your codes after final submission as the TAs may download the submitted codes or bitstream files from Canvas during checkouts. For the truth Table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*