Ayan Basu [redacted]

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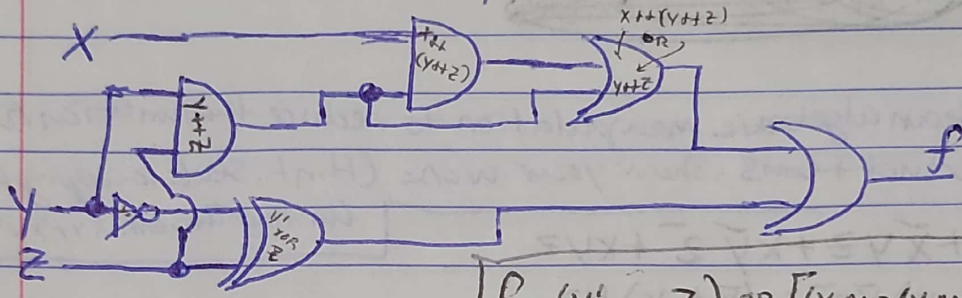
Lab 1: Combinational Logic; Simulation + Design

1. Using a logic simulator, either the one embedded in Section 1.4.3 of the interactive textbook or the one available at https://simulator.io/board, determine the function f implemented by the circuit in this figure



$$f = (Y' \text{ XOR } Z) \text{ OR } [(X \text{ AND } (Y \text{ AND } Z)) \text{ OR } (Y \text{ AND } Z)]$$

a) Show the truth table

X	Y	Z	Y'	Y' AND Z	Y' XOR Z	X AND (Y AND Z)	(X++(Y++Z)) OR (Y++Z)	(Y' XOR Z) OR (f) [(X++(Y++Z)) OR (Y++Z)]
0	0	0	1	0	1	0	0	1
0	0	1	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0
0	1	1	0	1	1	0	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	1	0	1	1	1	1	1

Inputs — Output

$$f = (Y' \text{ XOR } Z) \text{ OR } [(X \text{ AND } (Y \text{ AND } Z)) \text{ OR } (Y \text{ AND } Z)]$$

FINAL TRUTH TABLE w/ f + inputs

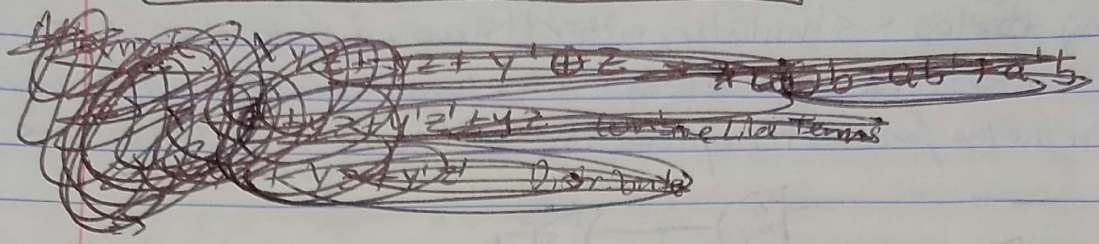
X	Y	Z	f = (Y' XOR Z) OR [(X AND (Y AND Z)) OR (Y AND Z)]
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

INPUTS

b. Write down the SOP (Sum-Of-Products) of the function.

$\bar{x}\bar{y}\bar{z} + \bar{x}yz + x\bar{y}\bar{z} + xyz \Rightarrow$

$\boxed{F = \bar{x}\bar{y}\bar{z} + \bar{x}yz + x\bar{y}\bar{z} + xyz}$



c) Use Boolean algebraic manipulation to reduce the function to two product terms. Show your work (Hint: seek to apply the Uniting theorem: $XY + XY' = X$)

$\bar{x}\bar{y}\bar{z} + \bar{x}yz + x\bar{y}\bar{z} + xyz$

$\Rightarrow (\bar{x} + x)\bar{y}\bar{z} + (\bar{x} + x)yz$

$\Rightarrow$ (applying the Uniting theorem) $\Rightarrow \boxed{F = \bar{y}\bar{z} + yz}$

2. Realize the function from part 1c in terms of only the following gates: 2-input OR, AND, NOR, NAND, and INV. (No XORs can be used). Use as few gates as possible. (Each inverter is counted as a gate. (Hint: seek to apply De Morgan's laws). Using the simulator, prove the equivalence of your new circuit to the original circuit.

$yz + y'z'$ (5 gates) De Morgan's $:= y'z' = (y+z)'$

$\Rightarrow yz + (y+z)'$ ~~(4 gates)~~ (3 gates) · AND · OR · NOR

y	z	g
0	0	1
0	1	0
1	0	0
1	1	1

· x variable doesn't affect output and it is shown that the truth table from 1a is repeated twice as y + z change

Circuit Diagram for Lab 1

Top Circuit: Question 1 – Original Circuit

Bottom Circuit: Question 2 – New Equivalence-Original Circuit