# LAB 3 Report

**Name:**

**UT EID:**

**Section:**

## Checklist:

### Part 1 -

i. Waveform of the structural AND gate (Just the uncommented portion)
ii. Constraint File (Just the uncommented portion)

### Part 2 -

iii. Constraint File (Just the uncommented portion)

### Part 3 -

iv. Truth Table of the function
v. K-maps showing minimization of the logic functions (outputs)
vi. Algebraic expression of the minimized logic functions (outputs)
vii. Verilog codes of module and testbench for structural modelling
viii. Simulation waveform for structural modelling
ix. Constraint File (Just the uncommented portion)

***Note*** → *The Verilog codes and the uncommented portions of the constraint files should be copied in your lab report and the actual Verilog (.v) and Constraint (.xdc) files need to be zipped and submitted as well on Canvas. You are not allowed to change your Verilog codes after final submission as the TAs may download the submitted codes from Canvas during checkouts. For the truth Table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*