***EE 316 – Lab 2 Report*: Combinational Logic with Verilog**

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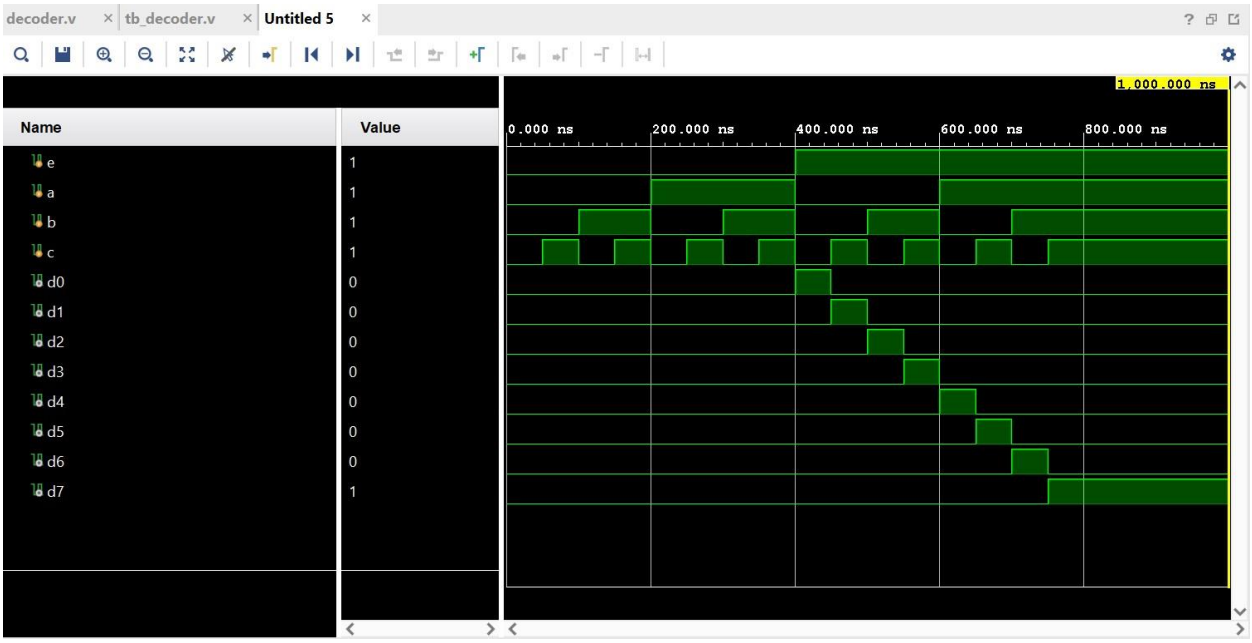
***Part 1*: Decoder**



***Part 2*: Multiplexer**

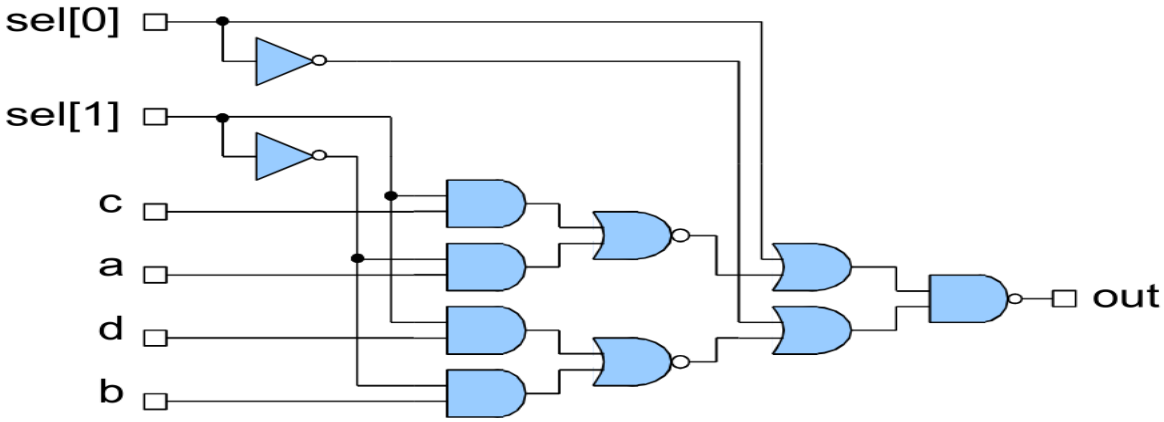
ii) Truth Table

iii) Algebraic Expression of Function

S_1	S_0	d
0	0	i_0
0	1	i_1
1	0	i_2
1	1	i_3

$d = S_1' S_0' i_0 + S_1' S_0 i_1 + S_1 S_0' i_2 + S_1 S_0 i_3$

iv) Logic Circuit Schematic



v) Verilog codes for module and testbench for structural modelling

Mux_structural.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/16/2021 10:21:45 PM
// Design Name:
// Module Name: Mux_structural
// Project Name:
// Target Devices:
```

```
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Mux_structural(
    input [1:0] sel,
    input i0, i1, i2, i3,
    output d
    );

    wire [1:0] sel_b;
    not not0 (sel_b[0], sel[0]);
    not not1 (sel_b[1], sel[1]);
    wire n0, n1, n2, n3;
    and and0 (n0, i2, sel[1]);
    and and1 (n1, i0, sel_b[1]);
    and and2 (n2, i3, sel[1]);
    and and3 (n3, i1, sel_b[1]);

    wire x0, x1;
```

```
    nor nor0 (x0, n0, n1);
    nor nor1 (x1, n2, n3);

    wire y0, y1;
    or or0 (y0, x0, sel[0]);
    or or1 (y1, x1, sel_b[0]);
    nand nand0 (d, y0, y1);

endmodule
```

Tb_Mux_structural.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/16/2021 10:26:21 PM
// Design Name:
// Module Name: tb_Mux_structural
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
```

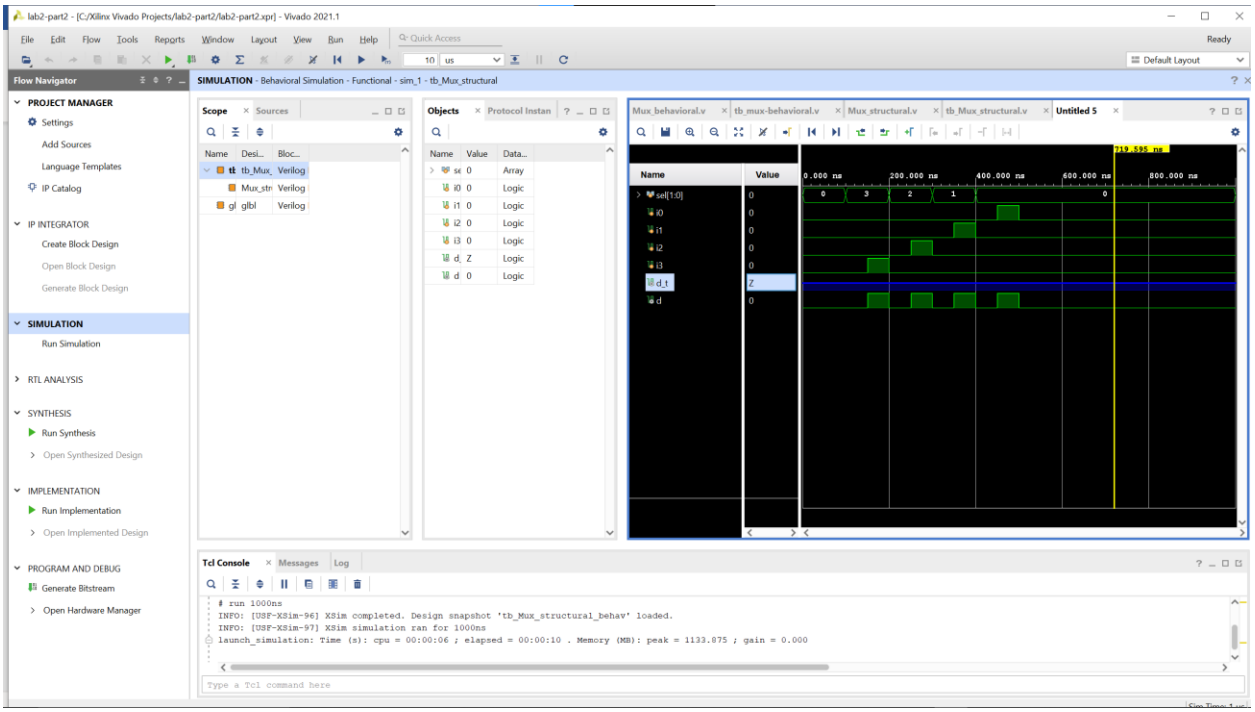
```
//
////////////////////////////////////////////////////////////////////////////////


module tb_Mux_structural;
   // Inputs te be define as registers
   reg [1:0] sel;
   reg i0;
   reg i1;
   reg i2;
   reg i3;

   // Outputs to be defined as wires
   wire d_t;

   // Instantiate the Unit Under Test (UUT)
   Mux_structural uut (
      .sel(sel),
      .i0(i0),
      .i1(i1),
      .i2(i2),
      .i3(i3),
      .d(d)
   );

   initial begin
      // Initialize inputs
      i0 = 1'b0;
      i1 = 1'b0;
```

```
i2 = 1'b0;
i3 = 1'b0;
sel = 2'b0;

#100;
// Stimulus - All imput combinations followed by some wait time to observe the o/p
sel = 3;
#50;
i3 = 1'b1;
#50;
i3 = 1'b0;

sel = 2;
#50;
i2 = 1'b1;
#50;
i2 = 1'b0;

sel = 1;
#50;
i1 = 1'b1;
#50;
i1 = 1'b0;

sel = 0;
#50
i0 = 1'b1;
#50;
i0= 1'b0;
```

end

endmodule

vi) Simulation Waveform of Structural Modeling



vii) Verilog codes for module and testbench for behavioral modelling

Mux_behavioral.v

`timescale 1ns / 1ps

//

// Company:

// Engineer:

//

// Create Date: 09/16/2021 10:23:11 PM

// Design Name:

```
// Module Name: Mux_behavioral
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module tb_Mux_behavioral;
   // Inputs te be define as registers
   reg [1:0] sel;
   reg i0;
   reg i1;
   reg i2;
   reg i3;

   // Outputs to be defined as wires
   wire d;

   // Instantiate the Unit Under Test (UUT)
   Mux_behavioral uut (
      .sel(sel),
```

```
    .i0(i0),
    .i1(i1),
    .i2(i2),
    .i3(i3),
    .d(d)
);

initial begin
    // Initialize inputs
    i0 = 1'b0;
    i1 = 1'b0;
    i2 = 1'b0;
    i3 = 1'b0;
    sel = 2'b0;

    #100;
    // Stimulus - All imput combinations followed by some wait time to observe the o/p
    sel = 0;
    #50
    i0 = 1'b1;
    #50;

    i0= 1'b0;
    sel = 1;
    #50;
    i1 = 1'b1;
    #50;

    i1 = 1'b0;
```

```
        sel = 2;
        #50;
        i2 = 1'b1;
        #50;

        i2 = 1'b0;
        sel = 3;
        #50;
        i3 = 1'b1;
        #50;
        i3 = 1'b0;

        end

endmodule
```

Tb_Mux_behavioral.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/16/2021 10:10:52 PM
// Design Name:
// Module Name: tb_mux-behavioral
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
```

```
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module tb_Mux_behavioral;
   // Inputs te be define as registers
   reg [1:0] sel;
   reg i0;
   reg i1;
   reg i2;
   reg i3;

   // Outputs to be defined as wires
   wire d;

   // Instantiate the Unit Under Test (UUT)
   Mux_behavioral uut (
      .sel(sel),
      .i0(i0),
      .i1(i1),
      .i2(i2),
      .i3(i3),
      .d(d)
```

```
);

initial begin
    // Initialize inputs
    i0 = 1'b0;
    i1 = 1'b0;
    i2 = 1'b0;
    i3 = 1'b0;
    sel = 2'b0;

    #100;
    // Stimulus - All imput combinations followed by some wait time to observe the o/p
    sel = 0;
    #50
    i0 = 1'b1;
    #50;

    i0= 1'b0;
    sel = 1;
    #50;
    i1 = 1'b1;
    #50;

    i1 = 1'b0;
    sel = 2;
    #50;
    i2 = 1'b1;
    #50;
```

```
        i2 = 1'b0;
        sel = 3;
        #50;
        i3 = 1'b1;
        #50;
        i3 = 1'b0;

        end

endmodule
```

viii) Simulation Waveform of Behavioral Modeling