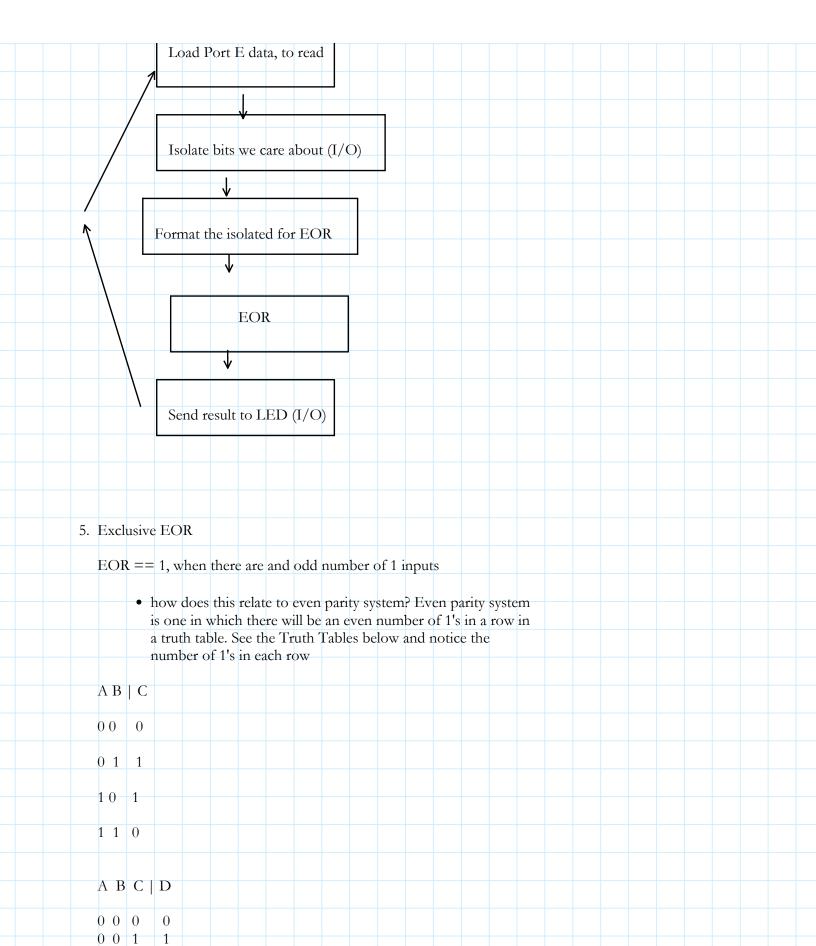
	anuary 21, 2021 3:39 PM
Ag	genda:
1	. Lab Procedures
	. Lab Requirements
	. Inititialization
	. Neg vs Pos Logic . EOR
	. Algorithms
	. Keil Basics -> see Canvas > EE319K > Files > Lab Lectures > "Keil5 Basics".pdf or "Keil5 Basics".mov
1	. Lab Procedures
1	Lab Froccures
	You do the labs the before, and then you do lab CHECKOUTS during your lab time.
	Van dan dan Carana dan anala dan a
	You signed up for a spot on google docs: https://docs.google.com/spreadsheets/d/1AxttUCjkirYM2pLiimbughAxH_G41gWsSGK_AXNI8mY/edit#gid=928541101
	Labs are graded on the key things mentioned in the grading sheets (deliverables, operation, coding stand questions/demo)
	Make sure to submit on canvas before your checkout
	Use Piazza and OH
	During lab 2, make sure to look for a partner
2	. Lab 1 requirements
2	Inputs - Port E 0-2. This connects to a switch using negative logic
2	
2	Inputs - Port E 0-2. This connects to a switch using negative logic negative logic: unpressed -> logical 1
2	Inputs - Port E 0-2. This connects to a switch using negative logic negative logic: unpressed -> logical 1 pressed -> logical 0
2	Inputs - Port E 0-2. This connects to a switch using negative logic negative logic: unpressed -> logical 1 pressed -> logical 0 Outputs - Port 4. Use positive logic positive logic: logical 0 -> LED off
2	Inputs - Port E 0-2. This connects to a switch using negative logic negative logic: unpressed -> logical 1 pressed -> logical 0 Outputs - Port 4. Use positive logic

csample truth rable for this lab: PEZ PEI PEO PE4 1		icial 1 Steam and a LED
example truth table for this lab: PE2 PB1 PD0 PB4 1		if it's 1 -> turn on the LED
PE2 PE1 PE0 PE4		cise -> tulli on the LLD
PE2 PE1 PE0 PE4		
1		
1		PE2 PE1 PE0 PE4
so on and so forth 3. Initialization a - turn on clock LDR R1, =SYSCTL_RCGCGPIO_R LDR R0, [R1] ORR R0, Wos10 STR R0, [R1] b - wait nop nop c - DIR LDR R1, =GPIO_PORTF_DIR_R LDR R0, [R1] AND R0, #0s18; to set bit 0-2 to 0 ORR R0, #0x10; to set bit 4 to 1 STR R0, [R1] AND R0, #0x18; to set bit 4 to 1 STR R0, [R1] ORR R0, #0x10; to set bit 4 to 1 STR R0, [R1] ORR R0, #0x10; to set bit 4 to 1 STR R0, [R1] 4 3 2 1 0 • NOTE, USE AND to clear bits; OR to set bits d - DEN LDR R1, =GPIO_PORTE_DEN_R LDR R0, #0x10 STR R0, #1 ORR R0, #0x17 STR R0, [R1] 4 3 2 1 0 4 5 2 1 0 4 5 2 1 0 Init the port and pin		1 1 1 bc there are 0 switched pressed
3. Initialization a - turn on clock LDR R1, =SYSCTI_RCGCGPIO_R LDR R0, [R1] ORR R0, #0x10 STR R0, [R1] b - wait nop nop nop c - DIR LDR R1, =GPIO_PORTE_DIR_R LDR R0, [R1] AND R0, #0x10 ; to set bit 0-2 to 0 ORR R0, #0x10 ; to set bit 4 to 1 STR R0, [R1] • NOTE, USE AND to clear bits; OR to set bits d - DEN LDR R1, =GPIO_PORTE_DEN_R LDR R0, [R1] ORR R0, #0x17 STR R0, [R1] A 3 2 1 0 4 3 2 1 0 4 5 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1 1 0 0 bc 1 switch is pressed
LDR R1, =SYSCTL_RCGCGP O_R		so on and so forth
LDR R1, =SYSCTL_RCGCGP O_R	3.	Initialization
LDR R1, =SYSCTL_RCGCGPIO_R LDR R0, [R1] ORR R0, #0x10 STR R0, [R1] b - wait nop nop c - DIR LDR R1, =GPIO_PORTE_DIR_R LDR R0, #0x10 STR R0, [R1] AND R0, #0x18 ORR R0, #0x10 STR R0, [R1] AND R0, #0x18 ORR R0, #0x10 STR R0, [R1] AND R0, #0x10 STR R0, [R1] • NOTE, USE AND to clear bits; OR to set bits d - DEN LDR R1, =GPIO_PORTE_DEN_R LDR R0, [R1] ORR R0, #0x17 STR R0, [R1] 4 3 2 1 0 4. Flowchart/Algorithm Init the port and pin		
1.DR R0, [R1]		a - turn on clock
1.DR R0, [R1]		LDR R1, =SYSCTL_RCGCGPIO_R // pseudocode style turn on clock for port E;
ORR R0, #0x10 STR R0, [R1] b - wait nop nop c - DIR LDR R1, =GPIO_PORTE_DIR_R LDR R0, [R1] AND R0, #0xF8; to set bit 0-2 to 0 ORR R0, #0x10; to set bit 4 to 1 STR R0, [R1] • NOTE, USE AND to clear bits; OR to set bits d - DEN LDR R1, =GPIO_PORTE_DEN_R LDR R0, [R1] ORR R0, #0x17 STR R0, [R1] ORR R0, #0x17 STR R0, [R1] 4. Flowehart/Algorithm Init the port and pin		LDR R0, [R1]
b - wait nop nop c - DIR LDR R1, =GPIO_PORTE_DIR_R LDR R0, [R1] AND R0, #0x18; to set bit 0-2 to 0 ORR R0, #0x10; to set bit 4 to 1 STR R0, [R1] • NOTE, USE AND to clear bits; OR to set bits d - DEN LDR R1, =GPIO_PORTE_DEN_R LDR R0, [R1] ORR R0, #0x17 STR R0, [R1] 4. Flowchart/Algorithm Init the port and pin		ORR R0, #0x10 E D C B A, therefore 0x10
nop nop nop		STR R0, [R1]
C - DIR		b - wait
C - DIR		
C - DIR LDR R1, =GPIO_PORTE_DIR_R Set bit to 1 when it's output, else 0 LDR R0, [R1] AND R0, #0xF8 to set bit 0-2 to 0 ORR R0, #0x10 to set bit 4 to 1 STR R0, [R1] 4 3 2 1 0		
LDR R1, =GPIO_PORTE_DIR_R LDR R0, [R1] AND R0, #0xF8 ; to set bit 0-2 to 0 ORR R0, #0x10 ; to set bit 4 to 1 STR R0, [R1] • NOTE, USE AND to clear bits; OR to set bits d - DEN LDR R1, =GPIO_PORTE_DEN_R LDR R0, [R1] ORR R0, #0x17 STR R0, [R1] 4. Flowchart/Algorithm Init the port and pin		
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AND R0, #0xF8 ; to set bit 0-2 to 0 1 0 0 0 0 STR R0, R1		
ORR R0, #0x10 ; to set bit 4 to 1 STR R0, [R1] • NOTE, USE AND to clear bits; OR to set bits d - DEN LDR R1, =GPIO_PORTE_DEN_R LDR R0, [R1] ORR R0, #0x17 STR R0, [R1] 4. Flowchart/Algorithm Init the port and pin		
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LDR R0, [R1] ORR R0, #0x17 STR R0, [R1] 4. Flowchart/Algorithm Init the port and pin		d - DEN
LDR R0, [R1] ORR R0, #0x17 STR R0, [R1] 4. Flowchart/Algorithm Init the port and pin		IDD D1 -CDIO DODTE DEN D
ORR R0, #0x17 STR R0, [R1] 4. Flowchart/Algorithm Init the port and pin		
STR R0, [R1] 4 3 2 1 0 4. Flowchart/Algorithm Init the port and pin		ORR R0 #0x17 1 0 1 1 1
Init the port and pin		
Init the port and pin		Eleveles of / Alexaides
	4.	
		Init the port and pin
Load Port E data, to read		
		Load Port E data, to read



1

1

0

1

0 1 0

0 1 1

1 0 0

		1 0	1	0																		-
		1 0 1 1	0	0																		
		1 1 1 1	1	1																		
	6.	Misc																				
		ARE	ΕΑΓ	OATA	\ -> (obje	cts in	ı RA	M													
		ARE	A C	CODI	<u>∃</u> -> (obje	cts to) RC)M													
		EQU	J to assign value to a constant																			
																						_