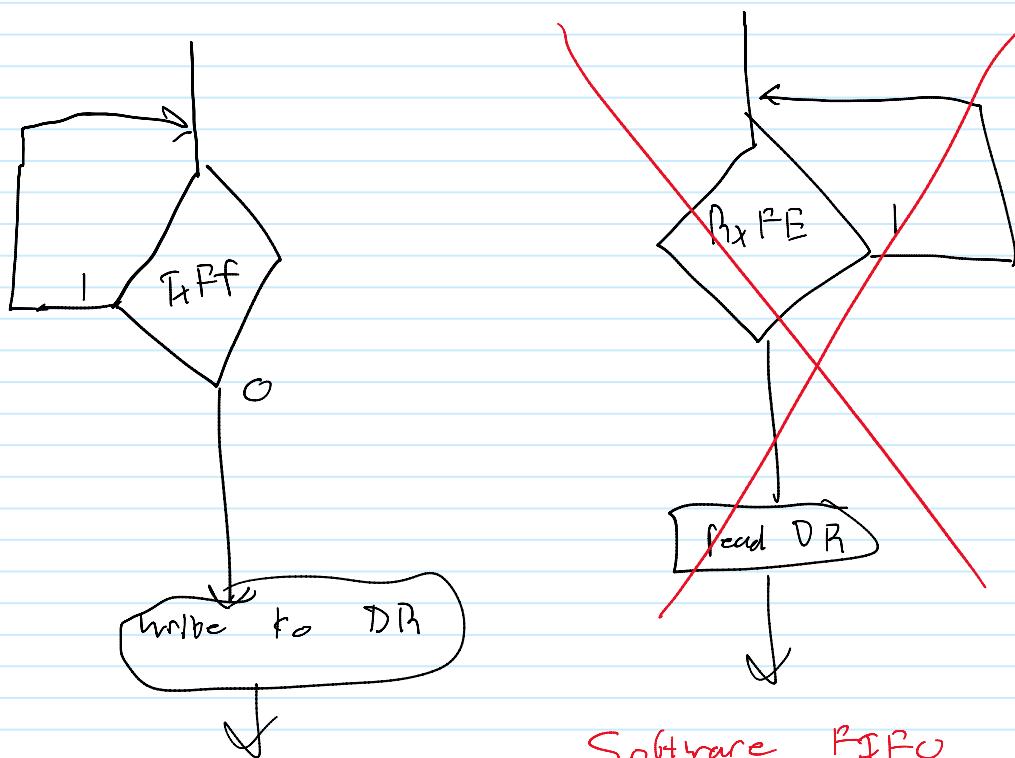
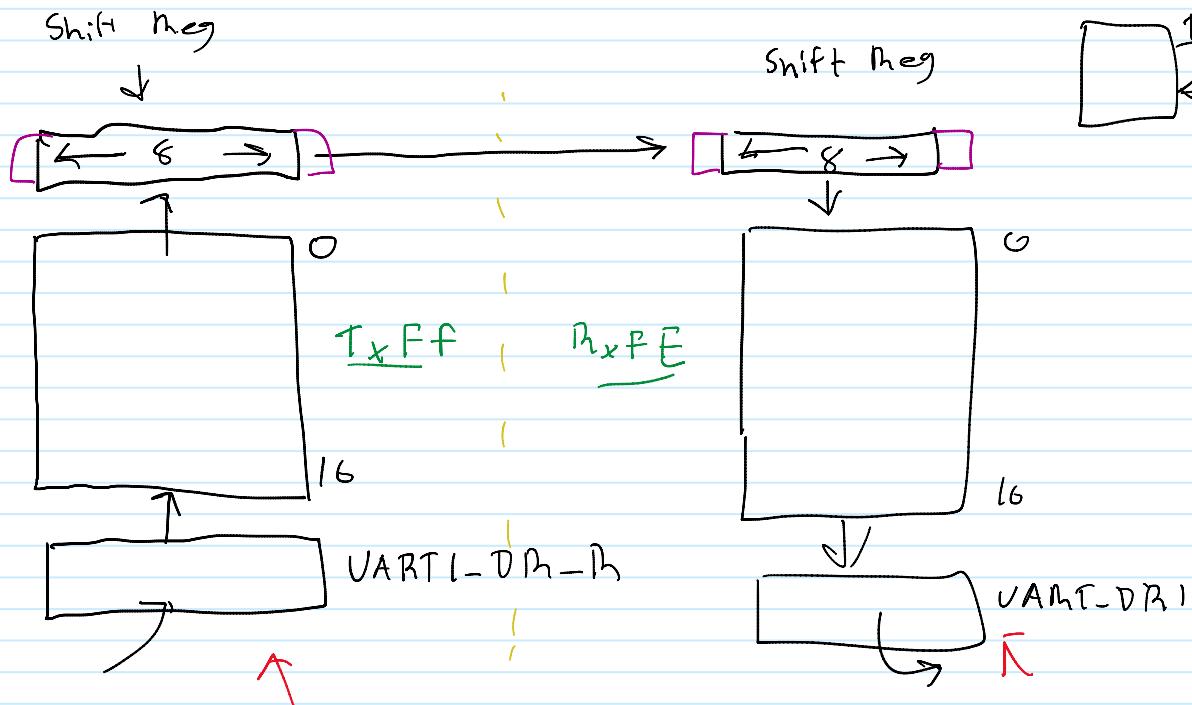
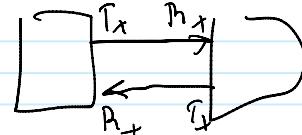
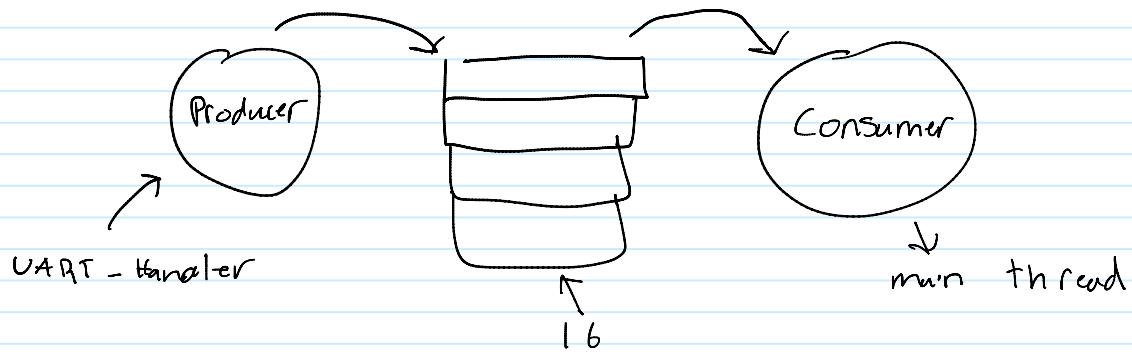


Lab 9 Lecture Notes

Monday, April 19, 2021 6:33 PM

Communication through UART





- ① NVIC_EN0_R } UART - Init
- ② NVIC_PRI1_R }
- ③ UART1_ICR_R → UART - Handler

UART Init



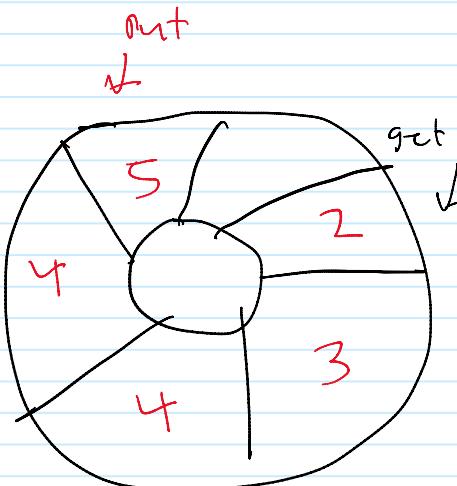
```
// Assumes a 50 MHz bus clock, create 115200 baud rate
void UART_Init(void){
    SYSCTL_RCGCUART_R |= 0x0001; // activate UART0
    SYSCTL_RCGCGPIO_R |= 0x0001; // activate port B
    while((SYSCTL_PRCGPIOR&0x01) == 0){};
    UART0_CTL_R &= ~0x0001; // disable UART
    UART0_IBRD_R = 27; // 80MHz
    // IBRD=int(50000000/(16*115,200)) = int(27.1267)
    UART0_FBRD_R = 8; // 80MHz
    // FBRD = round(0.1267 * 64) = 8
    UART0_LCRH_R = 0x0070; // 8-bit length, enable FIFO
    UART0_CTL_R = 0x0301; // enable RXE, TXE and UART
    GPIO_PORTB_AFSEL_R |= 0x03; // alt funct on PB1-0
    GPIO_PORTB_PCTL_R =
        (GPIO_PORTB_PCTL_R&0xFFFFF00)+0x00000011;
    GPIO_PORTB_DEN_R |= 0x03; // digital I/O on PB1-0
    GPIO_PORTB_AMSEL_R &= ~0x03; // No analog on PB1-0
}
```

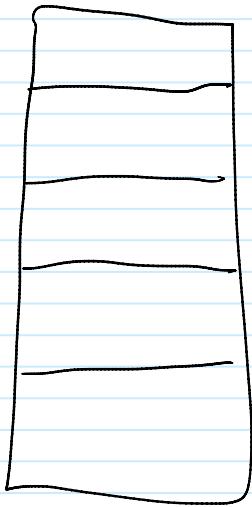
Lab 7



FIFO

FIFO - get → 1





Note: Other lab lecture can be viewed in announcements