Lab 9 grading sheet Circle professor

1) Name Last_____ First_____ EID_____ AC, VT, JV, RY

2) Name Last_____ First_____ EID_____ AC, VT, JV, RY

Use same spelling as listed on Canvas

1. Deliverables 20%:

*Submit your UART1.c, Fifo.c, and Lab9.c as three **INDIVIDUAL** C files to Canvas. Combine the following components into one pdf file and upload this file also to Canvas. Have the pdf file and Keil open on the computer during demonstration*

.

0) Your names, professors, and EIDs.
1) A circuit diagram showing position sensor, the UART, and the LCD.
2) Four screenshots of the TExaSdisplay logic analyzer traces and answer Q1 Q2 Q3 and Q4
3) This is a very hard question. The sampling rate is 10 Hz, what changes would you have to make to sample 100 times faster, at 1000 Hz? Refer to measurements taken in Lab 7

2. Performance 35%:
Does it handle correctly all situations as specified?
How pretty is the software?

3. Adhere to coding standard 5%:
Good Names have meaning
Variables have units in comments
Consistent indentation
Consistent use of braces
C99 style

1) 2)

4. Demonstration 40% (TAs will ask similar, but not exactly identical questions):

You will show the TA your program operation on one TM4C123 board with PC4 connected to PC5. You will run TExaSdisplay logic analyzer to visualize heartbeats and TxD→RxD. We expect you to explain the relationship between your executing software and the signals displayed on the TExaSdisplay logic analyzer. Also be prepared to explain how your software works and to discuss other ways the problem could have been solved. How do you initialize UART? How do you input and output using UART? What is the difference between busy-wait and interrupt synchronization? What synchronization method does the transmitter UART use? What synchronization method does the receiver UART use? What sets RXFE, TXFF, RXRIS, RTRIS and when are they set? What clears RXFE, TXFF, RXRIS, RTRIS and when are they cleared? What does the PLL do? Why is the PLL used? There are both hardware and software FIFOs in this system. There are lots of FIFO code in the book and on the web that you are encouraged to look at, but you are responsible for knowing how your FIFO works. What does it mean if the FIFO is full? Empty? What should your system do if the FIFO is full when it calls PUT? Why? What should your system do if the FIFO is empty when it calls GET? Why?

1) 2)

Total:

There will be a 10 points penalty if you do not use your Lab 7 software.