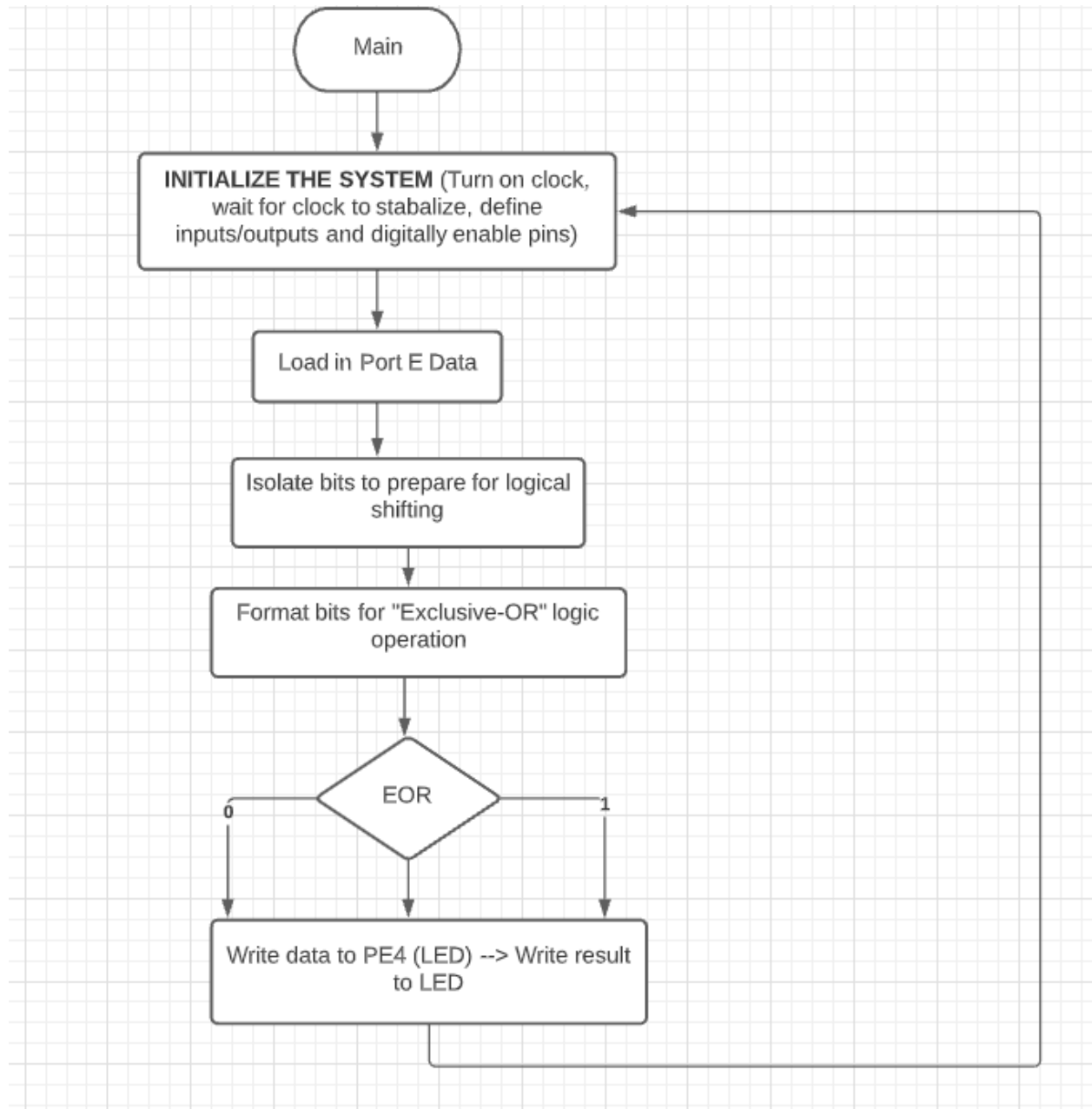


Ayan Basu (EID: ab73287)
Dr. Yerraballi - Unique #17070
EE319K - Intro. To Emb. Sys.
02 February 2021

Lab 1 - Digital Logic on TM4C123

Part B - Flowchart



Part C - Pseudocode

- Start
- Activate clock for port (Read/Modify/Write) (E = 1)
 - Wait for clock to stabilize
 - Define inputs and outputs
 - Digitally enable PE0, PE1, PE2, PE4 pins
 - Make PE0, PE1, PE2 (switch) pins as input
 - Make PE4 (LED) pin as output
- Loop
- Read input from switch
 - Isolate and format bits for logical shifting
 - Display output (0 or 1 → LED ON or OFF)
 - Branch Loop

Part D - Results

The image displays three screenshots of the TExaS Lab 1 software interface, showing the configuration of Port E hardware and registers. The interface is divided into three main sections: Port E Hardware, Port E Registers, and Grading Controls.

Port E Hardware: This section shows a schematic diagram of the Port E hardware. It includes a 16 MHz clock source, a TM4C123 microcontroller, and three switches (SW1, SW2, SW3) connected to pins PE0, PE1, and PE2. Pin PE4 is connected to an LED. The switches are labeled with their respective pin numbers (PE0, PE1, PE2) and the LED is labeled with its pin number (PE4).

Port E Registers: This section displays the configuration of the Port E registers. The registers shown are DATA, DIR, DEN, PUR, PDR, RCGCGPIO, LOCK, and CR. The values for these registers are as follows:

Register	Value
DATA	0x03
DIR	0x10
DEN	0x1F
PUR	0x00
PDR	0x00
RCGCGPIO	0x00000010
LOCK	0x00
CR	0xFF

The "Clock enabled" checkbox is checked.

Grading Controls: This section contains a "Number from EdX" input field, a "Grade" button, a "Score" field (set to 0), and a "Copy this to EdX" button.

The three screenshots show the same interface, but with different values in the "DATA" register (0x03, 0x11, and 0x00) and the "LED" status (ON, OFF, and ON).