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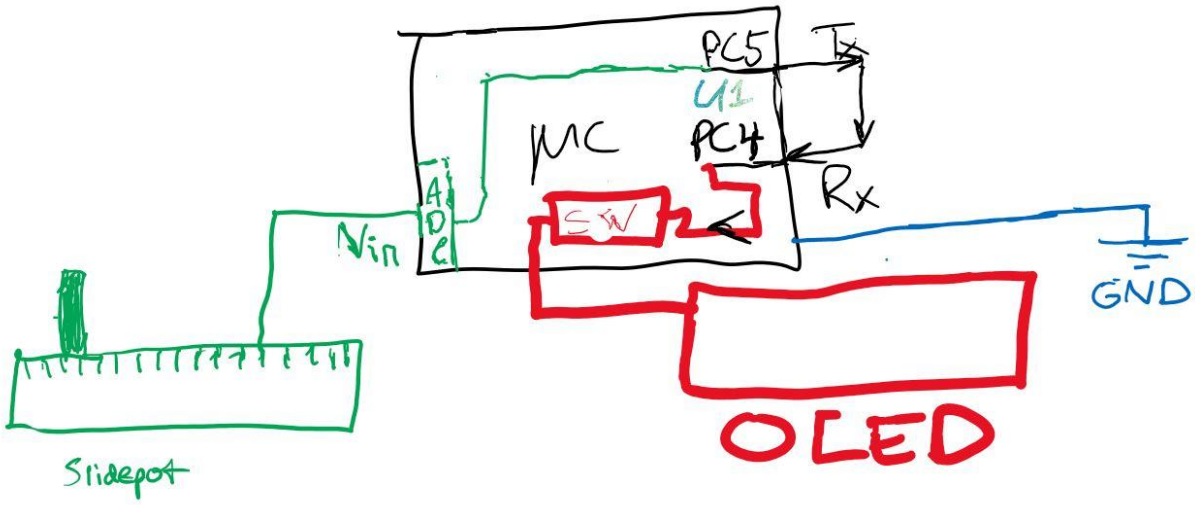
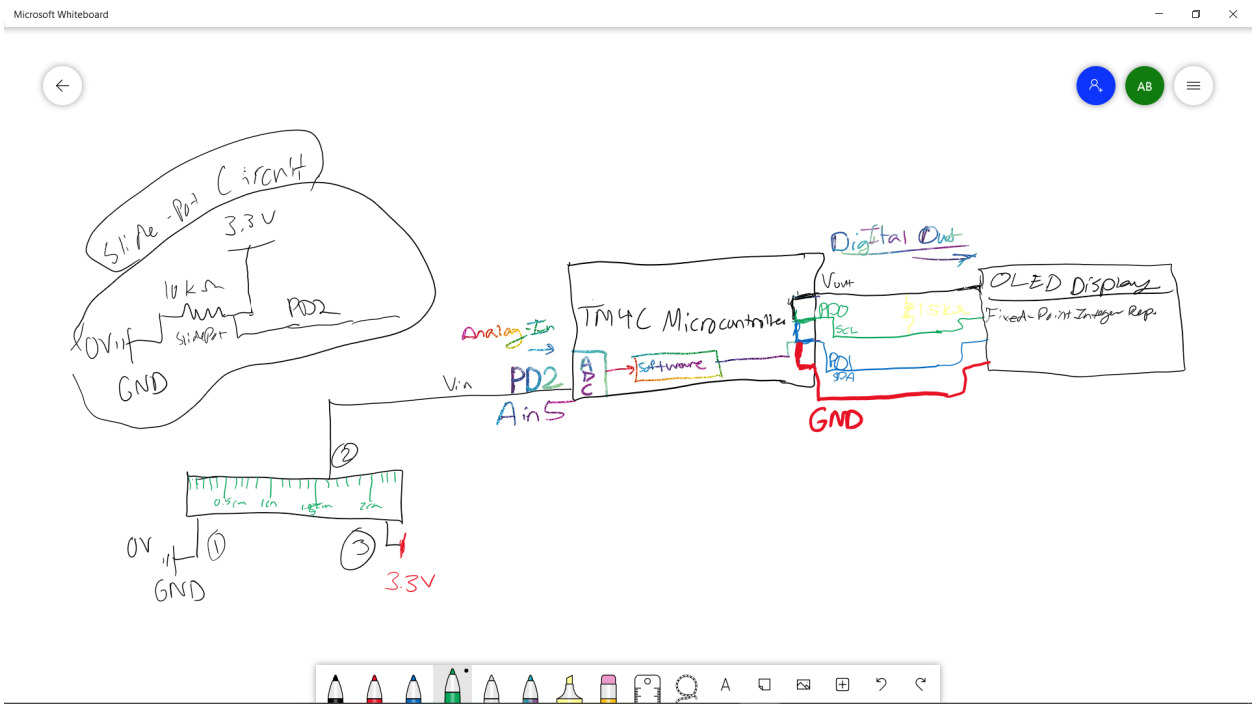
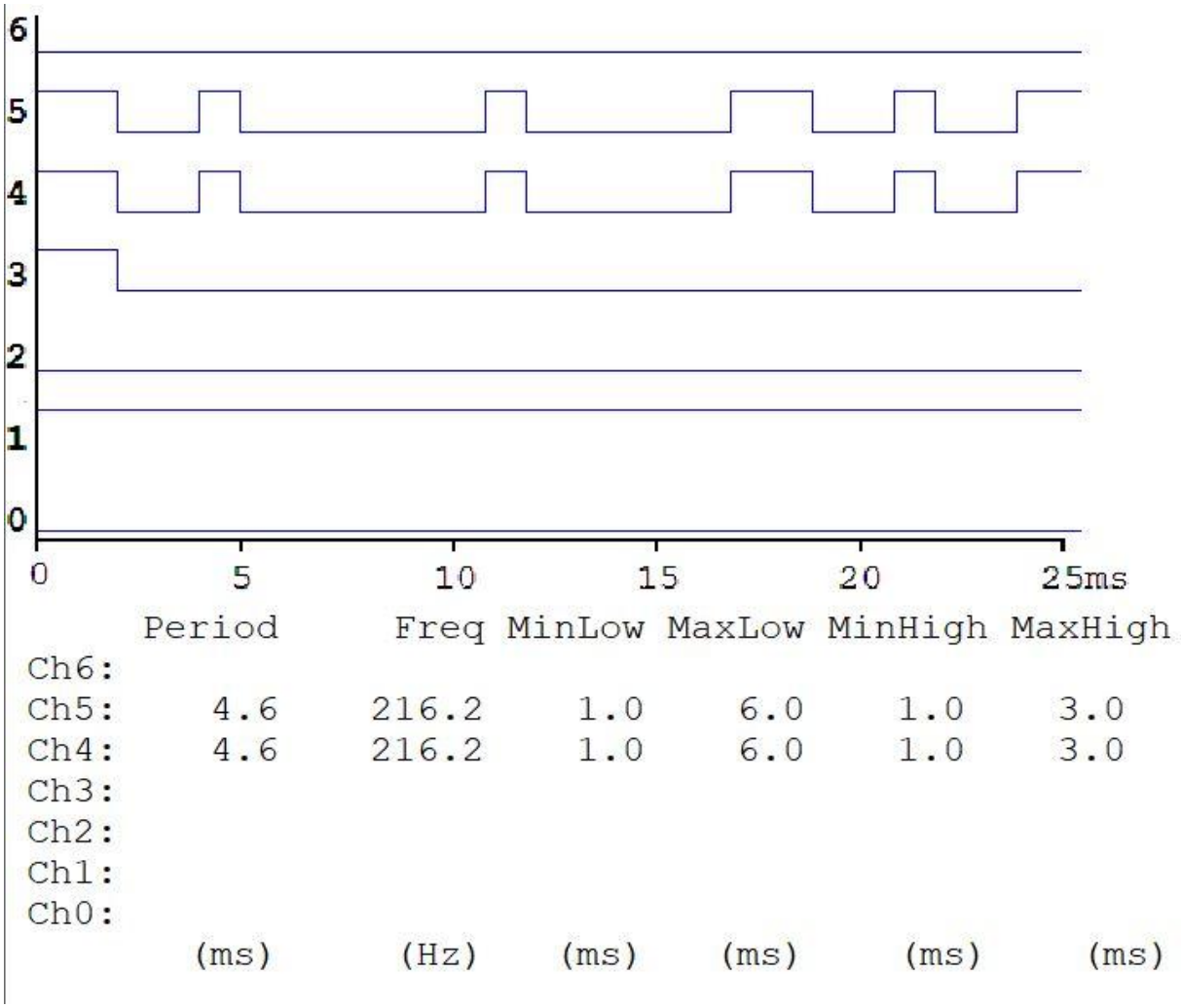
Lab 9 Deliverables

PART A: CIRCUIT DIAGRAM (with Position Sensor, UART & LCD)





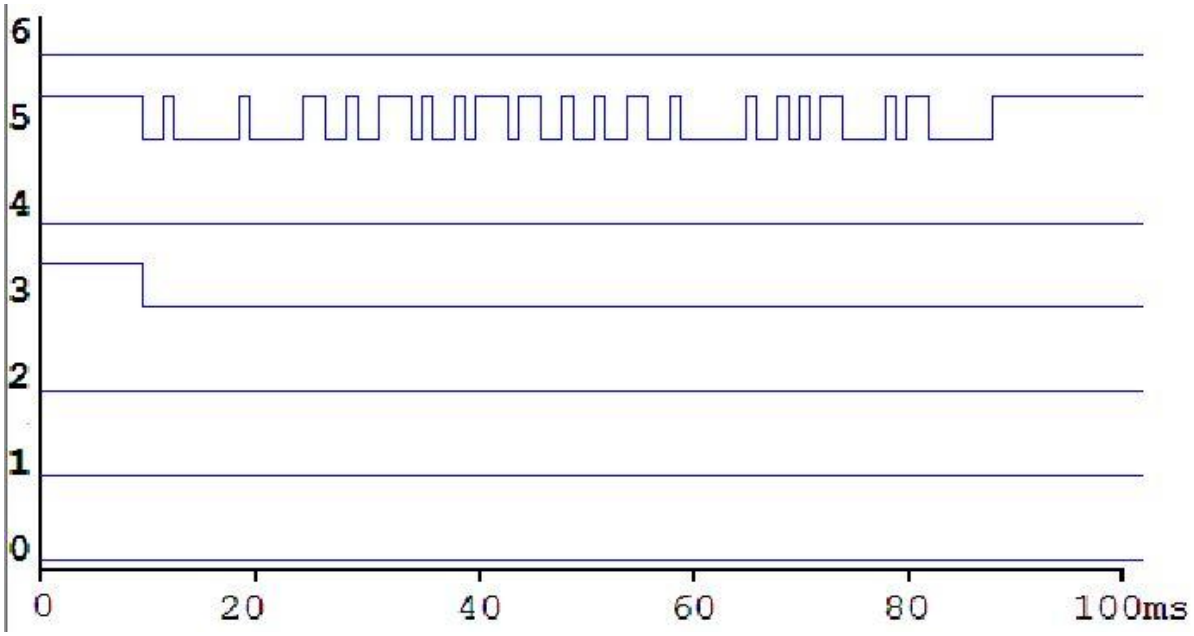
PART B: ScreenShots of Texas Display Logic Analyzer & Answers to Q1, Q2, Q3, Q4



	Period	Freq	MinLow	MaxLow	MinHigh	MaxHigh
Ch6:						
Ch5:	4.6	216.2	1.0	6.0	1.0	3.0
Ch4:	4.6	216.2	1.0	6.0	1.0	3.0
Ch3:						
Ch2:						
Ch1:						
Ch0:						
	(ms)	(Hz)	(ms)	(ms)	(ms)	(ms)

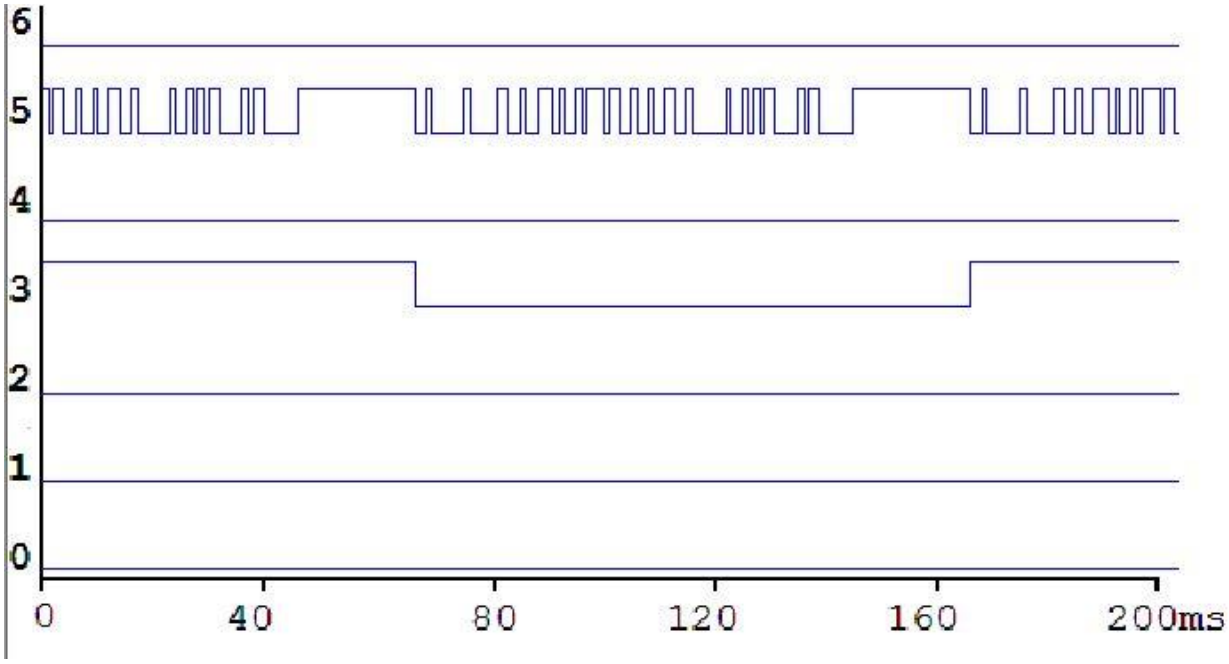
***Q1*: What is the baud rate?**

Baud rate is total number of bits per unit time. The baud rate is like the bits per sec that the UART transmits data. For this lab, the baud rate is **1000 bits per second**



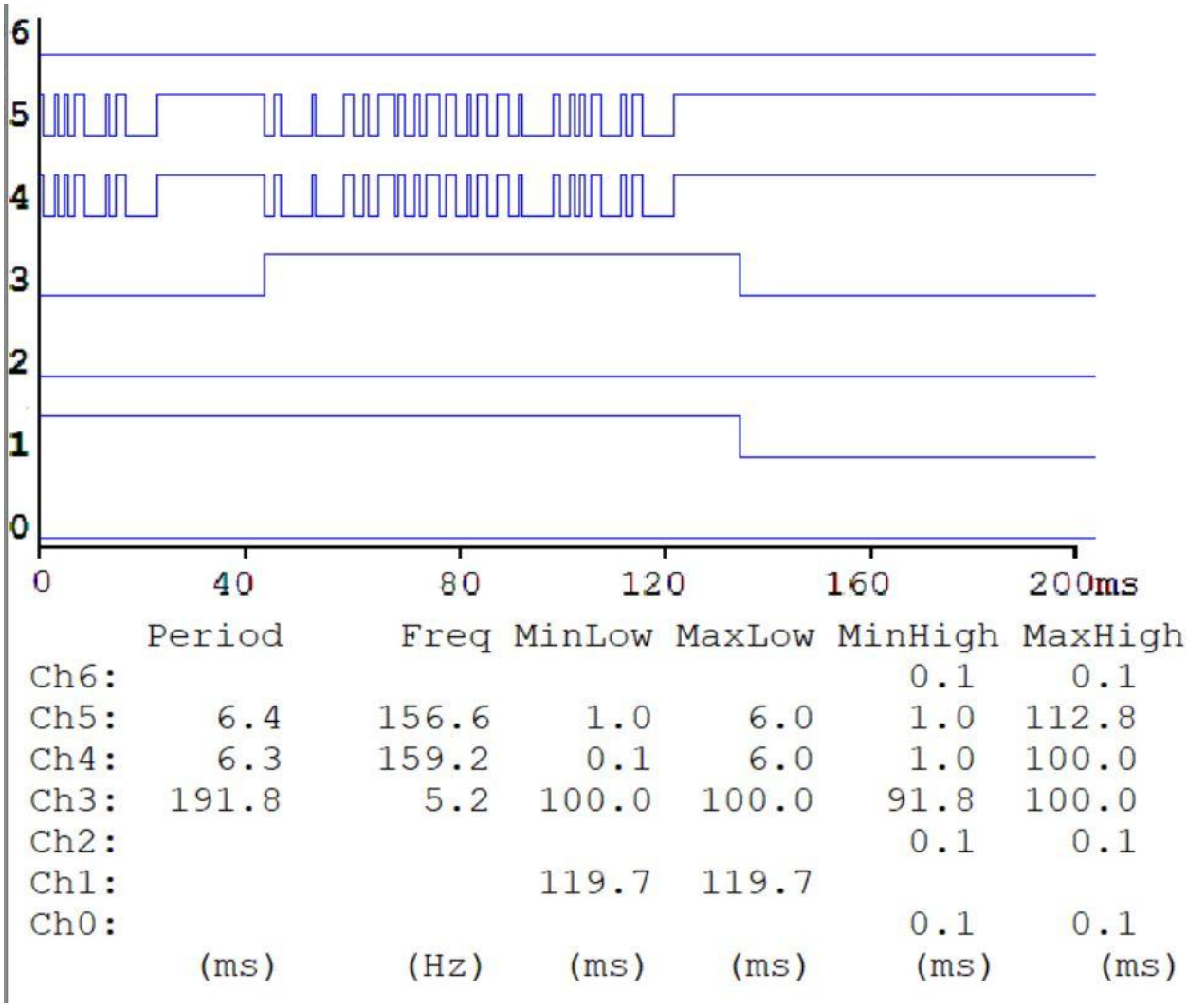
***Q2:** How long does it take to send an entire message?*

The time it takes to send a message through the UART is 10 times the inverse of the baud rate (i.e. if each bit takes x seconds to send, then 10 bits will take 10x seconds to send)



***Q3**: What is the sampling rate?*

Sampling rate is the number of times something measures something per second. In Lab 8, we were sampling the voltage level of the potentiometer, so the sampling rate was the number of times we measured its voltage per second



	Period	Freq	MinLow	MaxLow	MinHigh	MaxHigh
Ch6:					0.1	0.1
Ch5:	6.4	156.6	1.0	6.0	1.0	112.8
Ch4:	6.3	159.2	0.1	6.0	1.0	100.0
Ch3:	191.8	5.2	100.0	100.0	91.8	100.0
Ch2:					0.1	0.1
Ch1:			119.7	119.7		
Ch0:					0.1	0.1
	(ms)	(Hz)	(ms)	(ms)	(ms)	(ms)

***Q4*: Approximately how long does it take between ADC sampling in the SysTick ISR and the start of the OLED output in the main program?**

In Lab 8, there was a part where you measured how many microseconds your ADC took to convert a voltage level into a digital value. If the Systick ISR is mainly that part, then it'll approximately take that long before the main program runs.

PART C: 3) This is a very hard question: The sampling rate is 10 Hz, what changes would you have to make to sample 100 times faster, at 1000 Hz? Refer to measurements taken in Lab 7?

Referring to ADC sampling → referring to just systick → refers to its reload rate → grabbing the values from its adc based on the interrupt timings from systick → change sampling rate → change reload value; sac register for successive approximations.

Transmitter --. Through systick -- busy wait

Receiver - interrupt based - receiver when is half bull
Rxfe flag set when receiver fifo is empty
Txff flag set when transmitter fifo full
Know about rx & tx
Know how fifo is implemented
Know how uart communicates

LAB 9 DEMONSTRATION QUESTIONS

You will show the TA your program operation on one TM4C123 board with PC4 connected to PC5. You will run TExaSdisplay logic analyzer to visualize heartbeats and TxD→RxD. We expect you to explain the relationship between your executing software and the signals displayed on the TExaSdisplay logic analyzer. Also be prepared to explain how your software works and to discuss other ways the problem could have been solved. How do you initialize UART? How do you input and output using UART? What is the difference between busy-wait and interrupt synchronization? What synchronization method does the transmitter UART use? What synchronization method does the receiver UART use? What sets RXFE, TXFF, RXRIS, RTRIS and when are they set? What clears RXFE, TXFF, RXRIS, RTRIS and when are
they cleared? What does the PLL do? Why is the PLL used? There are both hardware and software FIFOs in this system. There are lots of FIFO code in the book and on the web that you are encouraged to look at, but you are responsible for knowing how your FIFO works. What does
it mean if the FIFO is full? Empty? What should your system do if the FIFO is full when it calls PUT? Why? What should your system do if the FIFO is empty when it calls GET? Why?