Lab Lecture 1

Thursday, January 21, 2021 3:39 PM

Agenda:

1. Lab Procedures
2. Lab Requirements
3. Inititialization
4. Neg vs Pos Logic
5. EOR
6. Algorithms
7. Keil Basics -> see *Canvas > EE319K > Files > Lab Lectures > "Keil5 Basics".pdf or "Keil5 Basics".mov*

1. Lab Procedures

   You do the labs the before, and then you do lab CHECKOUTS during your lab time.

   You signed up for a spot on google docs:
   https://docs.google.com/spreadsheets/d/1AxttUCjkirYM2pLiimbughAxH_G41gWsSGK_AXNI8mY/edit#gid=928541101

   Labs are graded on the key things mentioned in the grading sheets (deliverables, operation, coding standard, questions/demo)

   Make sure to submit on canvas before your checkout

   Use Piazza and OH

   During lab 2, make sure to look for a partner

2. Lab 1 requirements

   Inputs - Port E 0-2. This connects to a switch using negative logic

   negative logic: unpressed -> logical 1
   pressed -> logical 0

   Outputs - Port 4. Use positive logic

   positive logic: logical 0 -> LED off
   logical 1 -> LED on

   Goal: If there are an even number of switched pressed (even includes 0) then the output is 1, else it's 0.

if it's 1 -> turn on the LED
else -> turn off the LED

example truth table for this lab:

PE2	PE1	PE0	PE4
1	1	1	1 bc there are 0 switched pressed
1	1	0	0 bc 1 switch is pressed

so on and so forth

3. Initialization

a - turn on clock

```
LDR R1, =SYSCTL_RCGCGPIO_R
LDR R0, [R1]
ORR R0, #0x10
STR R0, [R1]
```

// pseudocode style || turn on clock for port E;
1 | 0 0 0 0
E | D C B A, therefore 0x10

b - wait

```
nop
nop
```

c - DIR

```
LDR R1, =GPIO_PORTE_DIR_R
LDR R0, [R1]
AND R0, #0xF8   ; to set bit 0-2 to 0
ORR R0, #0x10   ; to set bit 4 to 1
STR R0, [R1]
```

set bit to 1 when it's output, else 0

1 | 0 0 0 0

4 | 3 2 1 0

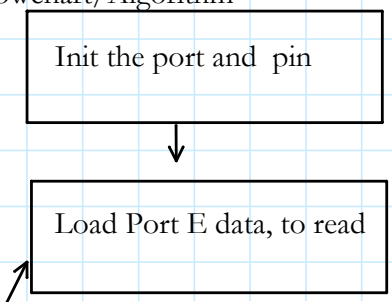
- NOTE, USE AND to clear bits; OR to set bits

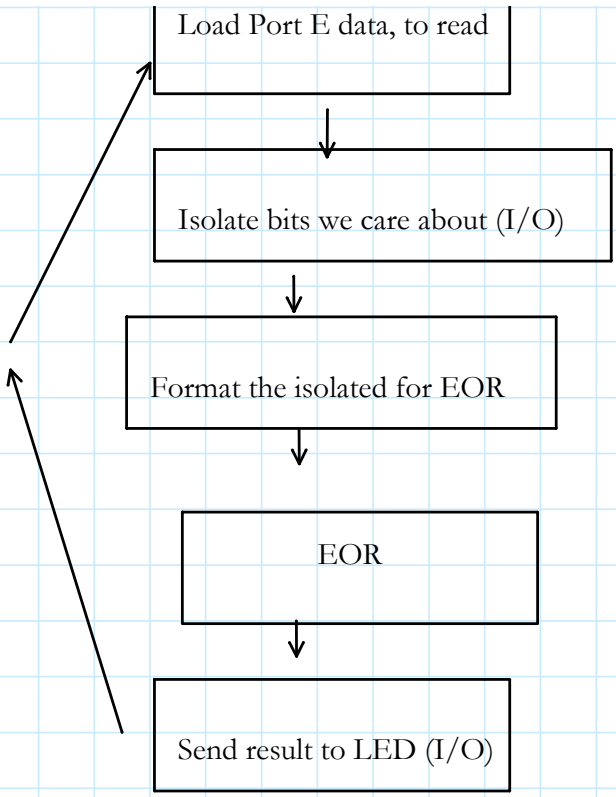
d - DEN

```
LDR R1, =GPIO_PORTE_DEN_R
LDR R0, [R1]
ORR R0,  #0x17
STR R0, [R1]
```

1 | 0 1 1 1
4 | 3 2 1 0

4. Flowchart/Algorithm





5. Exclusive EOR

   EOR == 1, when there are and odd number of 1 inputs

   - how does this relate to even parity system? Even parity system is one in which there will be an even number of 1's in a row in a truth table. See the Truth Tables below and notice the number of 1's in each row

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1

1 0 1 0
1 1 0 0
1 1 1 1

6. Misc.

   AREA DATA -> objects in RAM

   AREA CODE -> objects to ROM

   EQU to assign value to a constant