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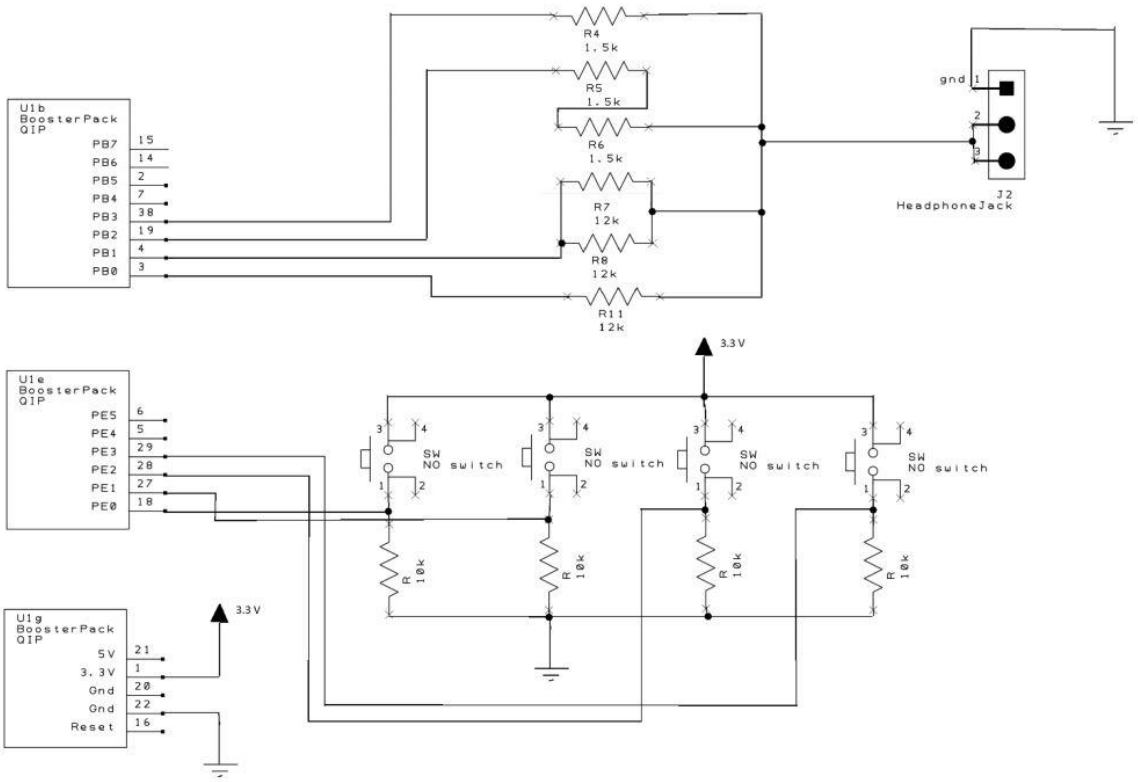
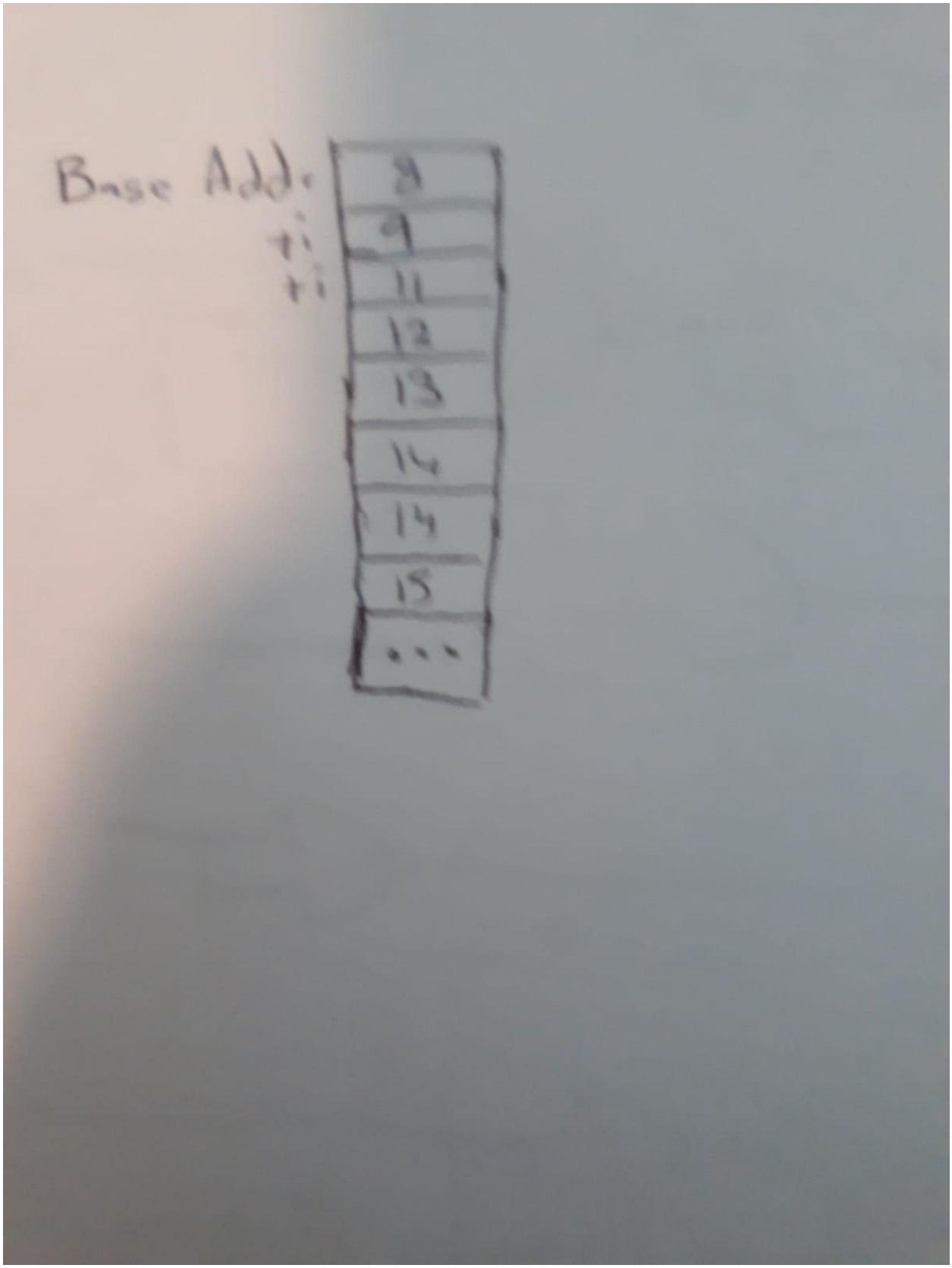
## ***Lab 6 Deliverables***

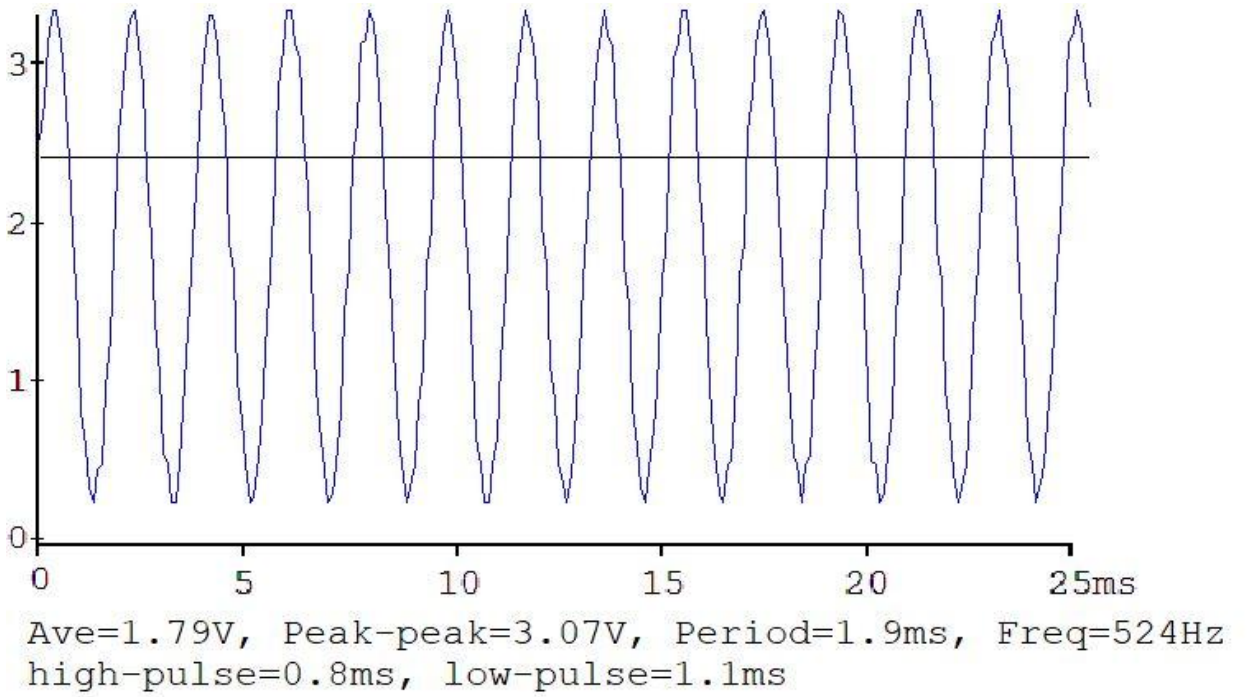
## ***PART A: DAC CIRCUIT DIAGRAM***

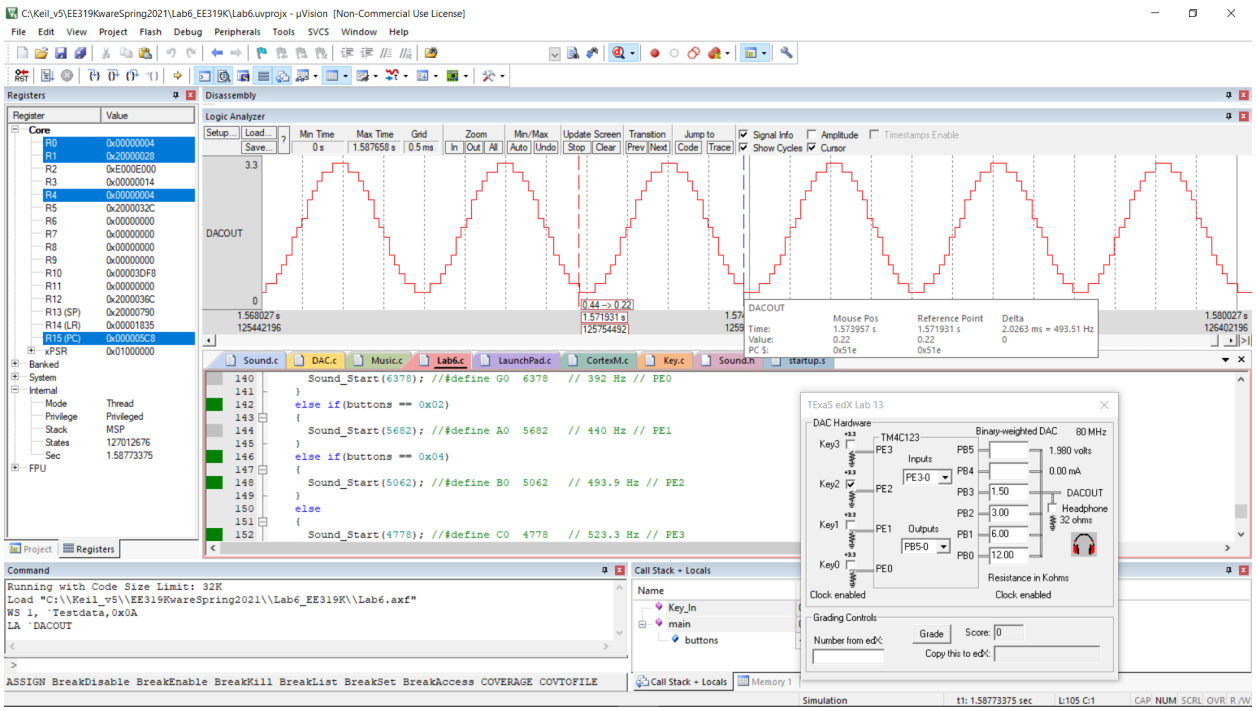



## ***PART B: SOFTWARE DESIGN (DRAWING OF DATA STRUCTURES)***


Base Add.
8
9
11
12
13
14
14
15
...

## ***PART C: TExaS Scope Display (part G)***



***PART D: Measurement Data***

| Bit3 bit2 bit1 bit0 | Theoretical DAC voltage | Measured DAC voltage |
|---|---|---|
| 0 | 0 | 0.002 |
| 1 | 0.22 | 0.229 |
| 2 | 0.44 | 0.444 |
| 3 | 0.66 | 0.682 |
| 4 | 0.88 | 0.894 |
| 5 | 1.10 | 1.124 |
| 6 | 1.32 | 1.348 |
| 7 | 1.54 | 1.578 |
| 8 | 1.76 | 1.731 |
| 9 | 1.98 | 1.954 |
| 10 | 2.2 | 2.177 |
| 11 | 2.42 | 2.405 |
| 12 | 2.64 | 2.613 |
| 13 | 2.86 | 2.834 |
| 14 | 3.08 | 3.062 |
| 15 | 3.3 | 3.293 |

*Resolution*: 0.22 V

*Range*: 3.3 V

*Precision*: 16 Alternatives (4-Bits)

*Accuracy*: +/- 0.11 V

***PART E: Deliverable Questions***

**1. When does the interrupt trigger occur?**
When the CURRENT value of the timer changes from 1 to 0.

**2. In which  file is the interrupt vector?**
In Startup.s

**3. List the steps that occur after trigger occurs and before processor executes handler**
- The current function is finished
- Eight registers are pushed into the Stack with R0 on top
- The vector address is loaded into the PC
- The ISR register is set to the interrupt number (15 for SysTick)
- The top 24 bits of LR are set to 0xFFFFFF. The bottom eight bits specify how to return from the interrupt.

**4. It looks like BX LR Instruction simply moves LR into PC, how does this return?**
The program knows that it is returning from an interrupt because the top 24 bits of LR are set to 0xFFFFFF. It follows these steps:
- Pop the eight registers off the stack
- Return to thread mode using Stack Pointer (if the bottom eight bits of the LR are 0xF9)
- The ISR is automatically reset to its previous state

***LAB 6 DEMONSTRATION QUESTIONS***

1. You should be able to demonstrate the three or four notes.

2. Be prepared to explain how your software works.

3. You should be prepared to discuss alternative approaches and be able to justify your solution.

4. The TA may look at your data and expect you to understand how the data was collected and how DAC works.

5. In particular, you should be able to design a DAC with 4 to 6 bits using the binary weighted approach.

6. What is the range, resolution and precision? You will tell the TA what frequency you are trying to generate, and they may check the accuracy with a frequency meter or scope.

7. TAs may ask you what frequency it is supposed to be, and then ask you to prove it using calculations.

8. Just having three different sounding waves is not enough, you must demonstrate the frequency is proper and it is a sinewave (at least as good as you can get with a 4-bit DAC).

9. You will be asked to attach your DAC output to the scope (part g). Many students come for their checkout with systems that did not operate properly.

10. You may be asked SysTick interrupt and DAC questions. If the desired frequency is **f**, and there are **n** samples in the sine wave table, what SysTick interrupt period would you use?

You should be able to demonstrate the four notes. Be prepared to explain how your software works. You should be prepared to discuss alternative approaches and be able to justify your solution. The TA may look at your data and expect you to understand how the data was collected and how DAC works. In particular, you should be able to design a DAC with 5 to 10 bits. What is the range, resolution and precision? You will tell the TA what frequency you are trying to generate, and they may check the accuracy with a frequency meter or scope. TAs may ask you what frequency it is supposed to be, and then ask you to prove it using calculations. Just having three different sounding waves is not enough, you must demonstrate the frequency is proper and it is a sinewave (at least as good as you can get with a 4-bit DAC).

You will be asked to attach your DAC output to the scope (part g). Many students come for their checkout with systems that did not operate properly. You may be asked SysTick interrupt and DAC questions. If the desired frequency is f, and there are n samples in the sine wave table, what SysTick interrupt period would you use?

1/f

2/2
This lab mentions 32 samples per cycle. Increasing the DAC output rate and the number of points in the
table is one way of smoothing out the “steps” that in the DAC output waveform. If we double the number of samples
from 32 to 64 to 128 and so on, keeping the DAC precision at 4-bit, will we keep getting a corresponding increase in
quality of the DAC output waveform?
As you increase the number of bits in the DAC you expect an increase in the quality of the output
waveform. If we increase the number of bits in the DAC from 4 to 6 to 8 and so on, keeping the number of points in

the table fixed at 32, will we keep getting a corresponding increase in quality of the DAC output waveform?