

You should test the hardware by running the SSD1306\_4C123 starter project.

## Part B. 1) C Driver

; sends two bytes to specified slave ; Input: R0 7-bit slave address R1 first 8-bit data to be written. R2 second 8-bit data to be written. ; Output: 0 if successful, nonzero (error code) if error ; Assumes: I2C3 and port D have already been initialized and enabled I2C Send2 -; --UUU--; 1) wait while I2C is busy, wait for I2C3\_MCS\_R bit 0 to be 0 ; 2) write slave address to I2C3\_MSA\_R, MSA bits7-1 is slave address MSA bit 0 is 0 for send data ; 3) write first data to I2C3\_MDR\_R ; 4) write 0x03 to I2C3\_MCS\_R, send no stop, generate start, enable ; add 4 NOPs to wait for I2C to start transmitting ; 5) wait while I2C is busy, wait for I2C3\_MCS\_R bit 0 to be 0 ; 6) check for errors, if any bits 3,2,1 I2C3\_MCS\_R is high ; a) if error set I2C3\_MCS\_R to 0x04 to send stop ; b) if error return R0 equal to error bits 3,2,1 of I2C3\_MCS\_R ; 7) write second data to I2C3\_MDR\_R ; 8) write 0x05 to I2C3\_MCS\_R, send stop, no start, enable ; add 4 NOPs to wait for I2C to start transmitting ; 9) wait while I2C is busy, wait for I2C3\_MCS\_R bit 0 to be 0 ; 10) return R0 equal to bits 3,2,1 of I2C3\_MCS\_R, error bits ; will be 0 is no error

tast Here 71) Load 1263\_MCS\_R

i) Left swift RM ; sends two bytes to specified slave ; Input: R0 7-bit slave address R1 first 8-bit data to be written. ii) Make sure bit 0 ef RO R2 second 8-bit data to be written. ; Output: 0 if successful, nonzero (error code) if error ; Assumes: I2C3 and port D have already been initialized and enabled I2C Send2 2 MSA-Rlocin ; --UUU--; 1) wait while I2C is busy, wait for I2C3\_MCS\_R bit 0 to be 0 ; 2) write slave address to I2C3\_MSA\_R, MSA bits7-1 is slave address MSA bit 0 is 0 for send data ; 3) write first data to I2C3 MDR R ; 4) write 0x03 to I2C3\_MCS\_R, send no stop, generate start, enable ; add 4 NOPs to wait for I2C to start transmitting ; 5) wait while I2C is busy, wait for I2C3\_MCS\_R bit 0 to be 0 ; 6) check for errors, if any bits 3,2,1 I2C3\_MCS\_R is high ; a) if error set I2C3\_MCS\_R to 0x04 to send stop ; b) if error return R0 equal to error bits 3,2,1 of I2C3\_MCS\_R ; 7) write second data to I2C3\_MDR\_R ; 8) write 0x05 to I2C3\_MCS\_R, send stop, no start, enable ; add 4 NOPs to wait for I2C to start transmitting ; 9) wait while I2C is busy, wait for I2C3\_MCS\_R bit 0 to be 0 ; 10) return R0 equal to bits 3,2,1 of I2C3\_MCS\_R, error bits ; will be 0 is no error oad mcs\_R loc moes

; sends two bytes to specified slave ; Input: R0 7-bit slave address R1 first 8-bit data to be written. R2 second 8-bit data to be written. ; Output: 0 if successful, nonzero (error code) if error ame as 12 ; Assumes: I2C3 and port D have already been initialized and enabled I2C\_Send2 ; --UUU--; 1) wait while I2C is busy, wait for I2C3\_MCS\_R bit 0 to be 0 ; 2) write slave address to I2C3\_MSA\_R, MSA bits7-1 is slave address MSA bit 0 is 0 for send data (ii) Right Shift by 1 ; 3) write first data to I2C3 MDR R ; 4) write 0x03 to I2C3\_MCS\_R, send no stop, generate start, enable ; add 4 NOPs to wait for I2C to start transmitting teact bit 2, ; 5) wait while I2C is busy, wait for I2C3\_MCS\_R bit 0 to be 6 ; 6) check for errors, if any bits 3,2,1 I2C3\_MCS\_R is high-; a) if error set I2C3\_MCS\_R to 0x04 to send stop ; b) if error return R0 equal to error bits 3,2,1 of I2C3\_MCS\_R Compare with O ; 7) write second data to I2C3\_MDR\_R ; 8) write 0x05 to I2C3\_MCS\_R, send stop, no start, enable ; add 4 NOPs to wait for I2C to start transmitting ; 9) wait while I2C is busy, wait for I2C3\_MCS\_R bit 0 to be 0 ; 10) return R0 equal to bits 3,2,1 of I2C3\_MCS\_R, error bits ; will be 0 is no error ; j'il mour Paron code to Ro "in") load mcs\_Rloc in reg (11) move 0x04 to rea

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Same as (3) > Same as (4) but write (0x05) Same as (5)

Part C: Dut skring fn. nul terminated array of char hull = 10' void SSD1306\_OutString(char \*ptr){ (00p(i=0) ->> Pfo[i] =='\\()'; i=i+1) SSD1306\_OutChar(ptr[i]);

## Part Do ID Functions

```
#define PF2 (*((volatile unsigned long *)0x40025010)) // PF2
#define PF4 (*((volatile unsigned long *)0x40025040)) // PF4
void IO_Init(void) { volatile uint32_t delay;
 // --UUU-- Code to initialize PF4 and PF2
 SYSCTL_RCGCGPIO_R =
                                       //1) activate clock for Port
delay = SYSCTL_RCGCGPIO_R;
                                      // allow time for clock to start
 GPIO PORTF DIR R =
                                       // 2) PF4 in, PF2<u>`out</u>
 GPIO PORTF PUR R =
                                       // 3) Set pullup register for PF4
 GPIO PORTF DEN R =
                                       // 4) enable digital I/O on PF4<del>,2</del>
                                   & Initalize a variable 1
 uint8_t led = 0x04;
 void IO_HeartBeat(void) {
 // --UUU--
   led ^= :
   PF2 = ;
    Clock_Delay1ms(100);
                                             Use this function
```

> Set bit 5
> Set for Output (=1)
Reset for input (20)
> Set bit 4

-> Set for bit 2,4

```
//-----IO_Touch------
// wait for release and press of
the switch
// Input: none
// Output: none
// 1) wait for release;
// 2) delay for 5ms;
// 3) wait for press; and then
// 4) delay for another 5ms

Wait While
PF4 is 1

We delay func
```

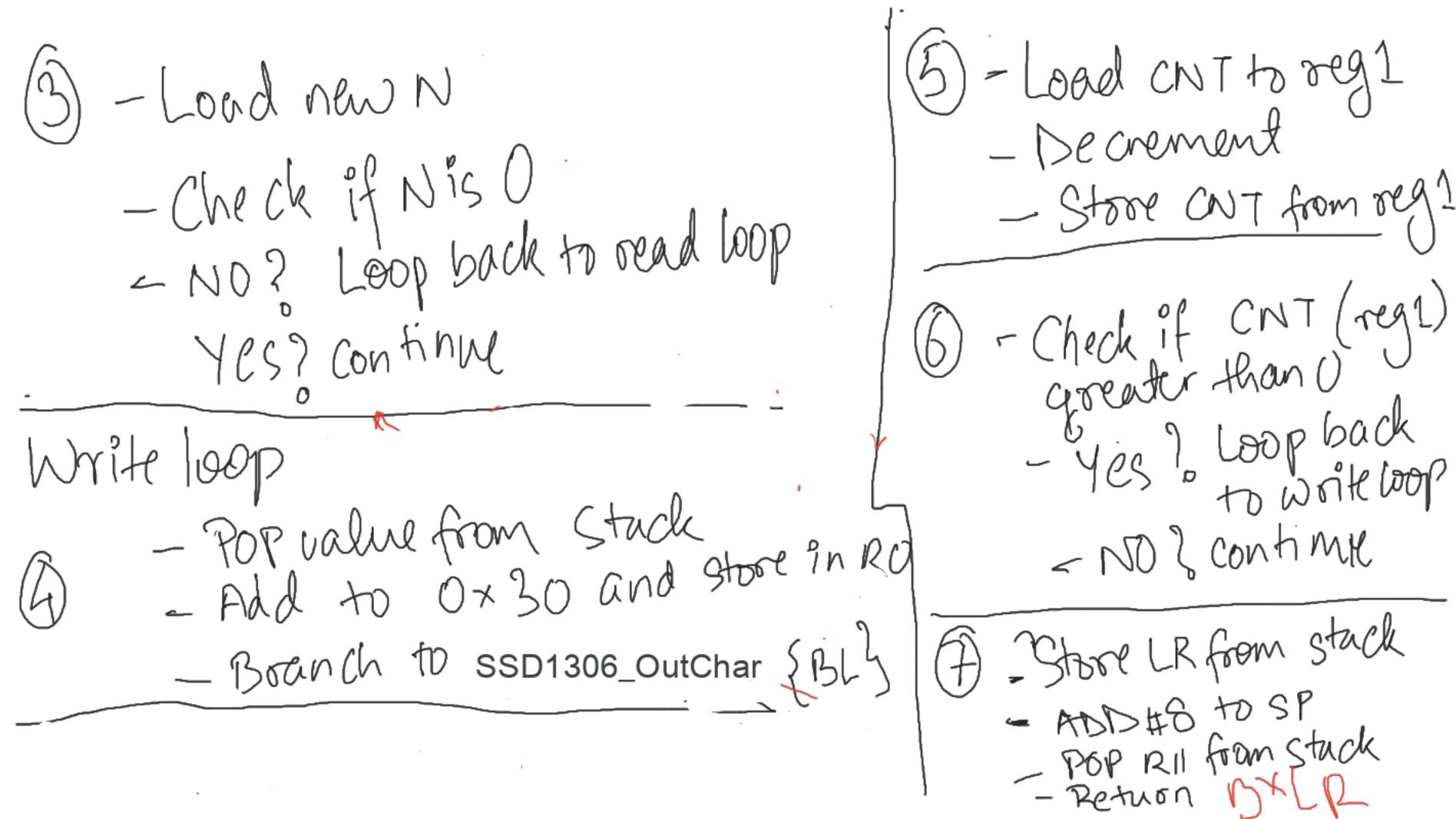
Kart E: LCD Driver (Out Dec) - The number to get units place for - Count of numbers Check for Frame pointer mit. 1 -> 2 -> 3 -> 4 CNTZ SP]Z 181-37-36-35 [ Init to U | [SP] z 5 -> 6 -> 7 -> 8 / CNT 2 1 -> 0 ] CNT z 4 -> 3 -> 2 -> 1 -> 0 ]

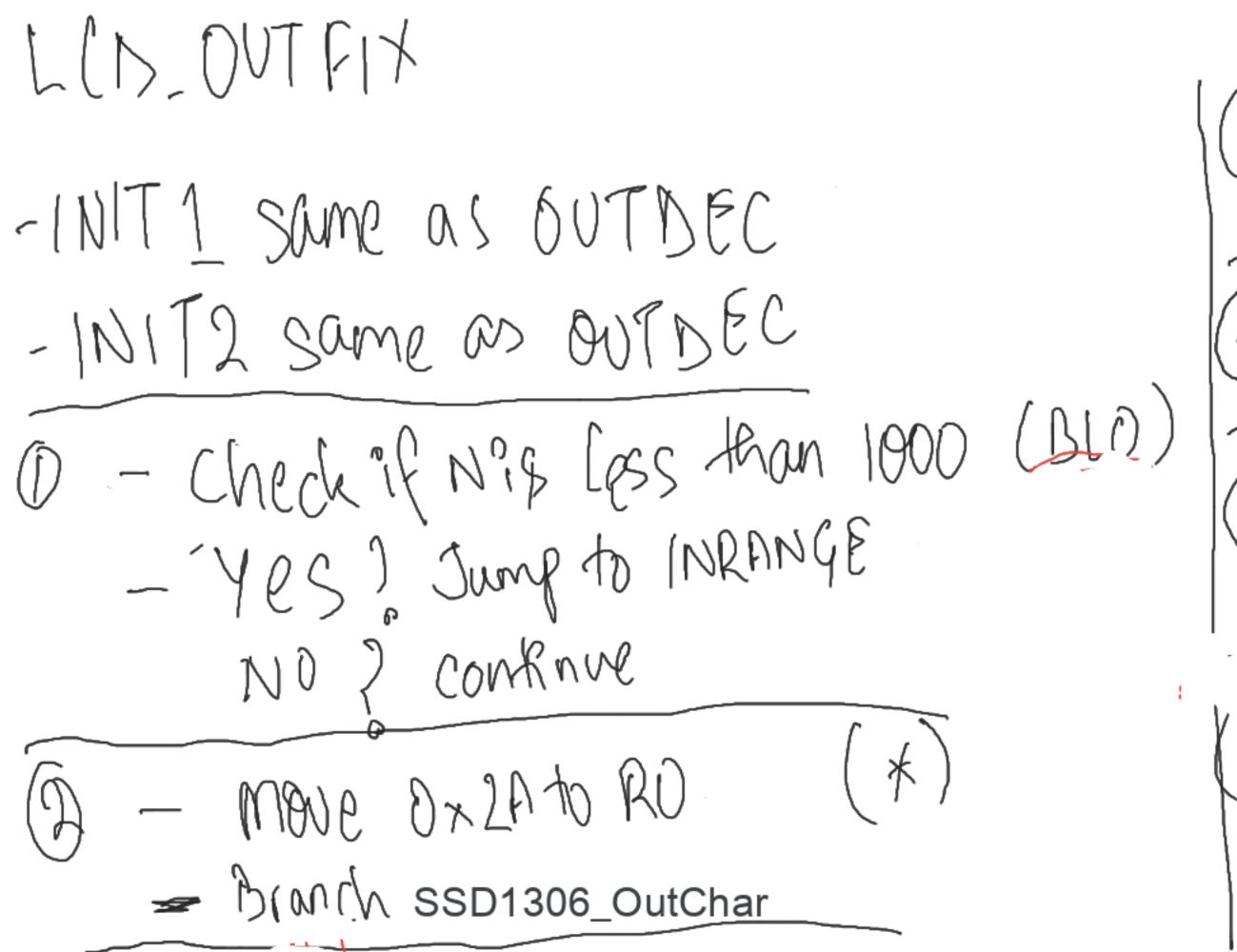
Out Dec Algorithm: (Using recud Nion) (INIT) L(D\_OMDec - Store RII on Stack - Stoge number N on Stack \_ make space for count (Subtract SP by 4) E CNT \$0 - Make SP your frame Pointer \_\_ Store LR on Stack How to access a vas % LDR RO,[FP,#CNT) CNT INT - Start (NT as 0 L) LDR RO, [FP, #CNT]

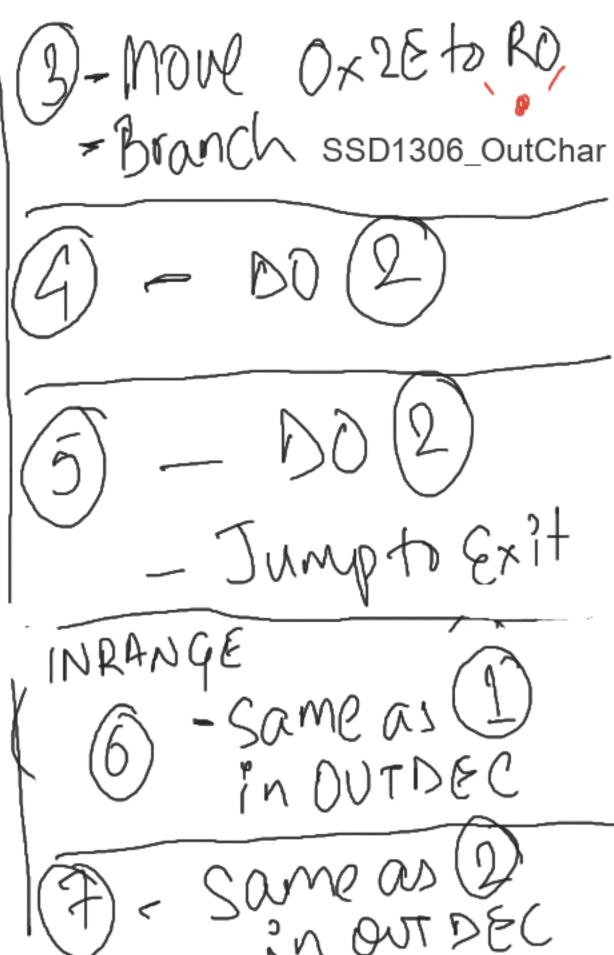
Toad a reg with #10 for division STR RO, [FP, #CNT] defined in bust slide

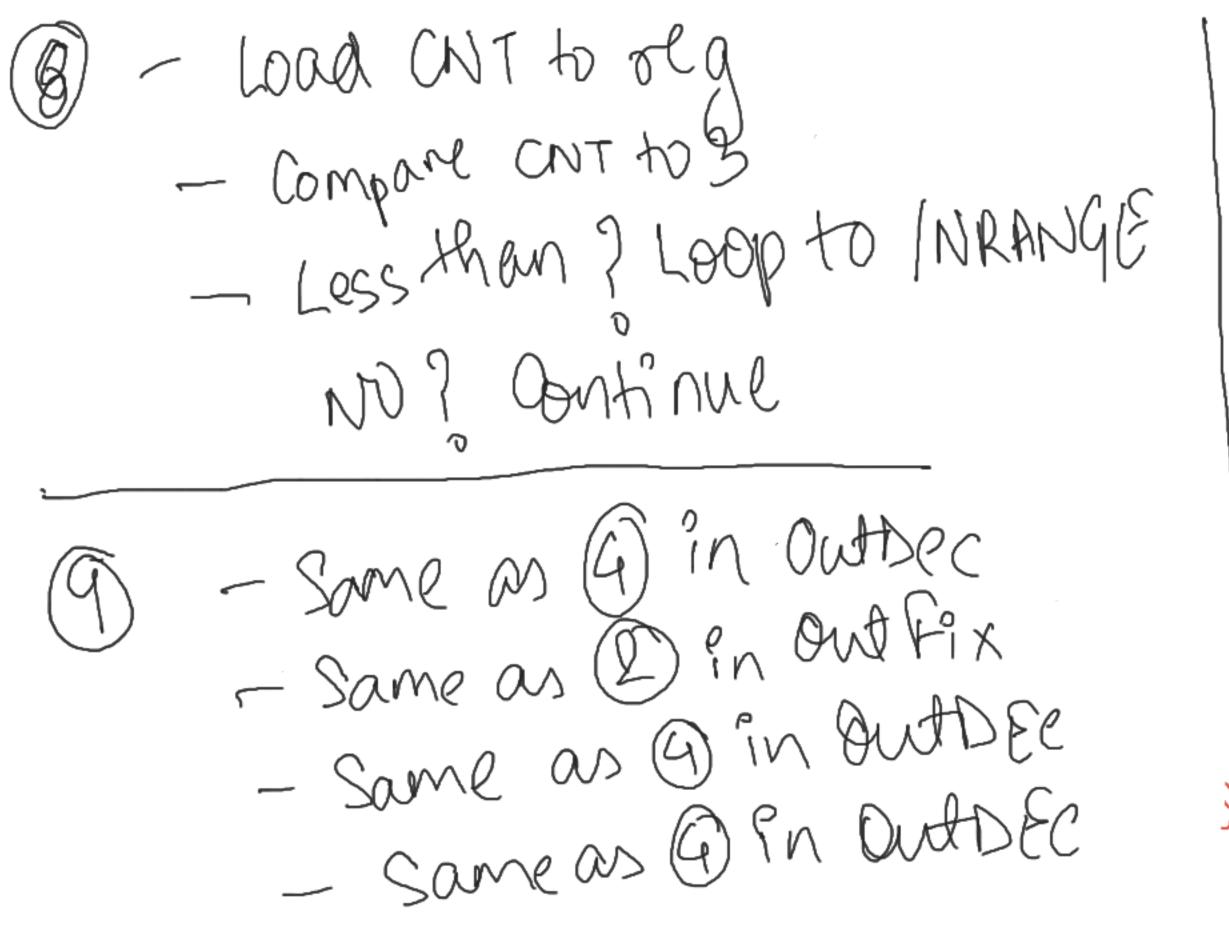
Toud on?, and I, stool Read 1997 1 - Load CNT to veg \_ Store regasion? local N - Load current value of N to reg ?

- Make a copy in reg? NI 'NJ.: - Un signed divide Leg 1 by 10 in reg 1 - Store this reg! as new N - Multiply this org I to 10 in reg I - Substract reg 1 from reg 2 (reg 1. reg 1)
- Store this difference to Stack









EXIT

- Store CR from Strick

- ADD#8 to SP

- Store RII from Stack

- return (BX:LR)