EE663 Frequency Synthesizers, Clock and Data Recovery Circuits

Second Semester of Academic Year 2023 - 2024
Course Project

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1 Objective

To Design a phase-locked loop (PLL) that meets the given criteria, including all sub- blocks (phase frequency detector, voltage-controlled oscillator, loop filters, and divider) using Verilog models and transistor level in Cadence design suit.

2 Target Specification

Input Frequency : 1.5×10^8 Hz
Output Frequency : 1.2×10^9 Hz
Frequency Divider : 8

3 Introduction

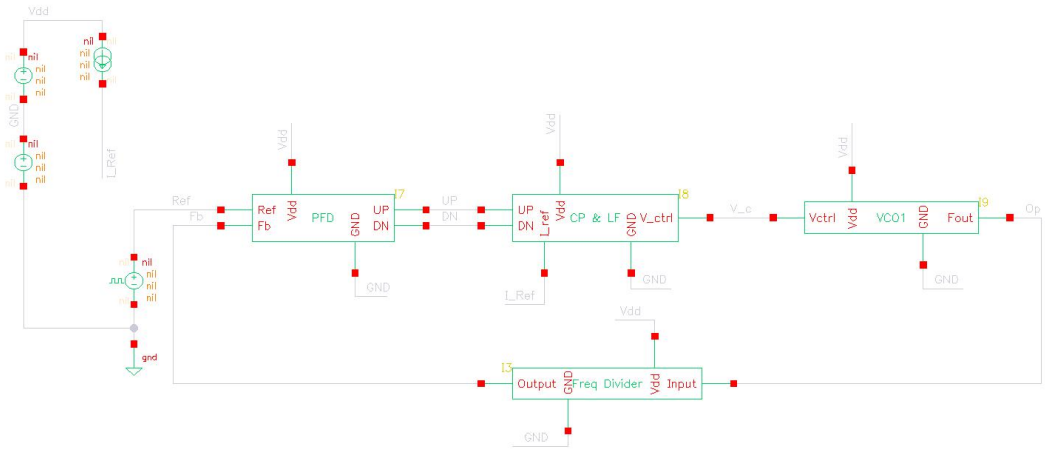

Figure 1: Phase-Locked Loop Schematic For Simulation

A Phase-Locked Loop is a frequency synthesizer which generates a high frequency which is a multiple of a reference frequency. Implementation of PLL has been done at a transistor level. The schematic as shown in fig. 1 has been used for simulation. The transistor level design of each block is shown in the following sections.

4 Phase Frequency Detector (PFD)

A PFD is a circuit architecture that detects phase shifts between input signals and generates a corresponding voltage pulse. A D-flipflop-based PFD has been implemented. The following figure 2 shows the internal circuit of Phase frequency Detector(PFD). [3]
The internal circuits of D-flipflop, Inverter, NOR gate and NAND gate are shown in fig. 3, 4, 5

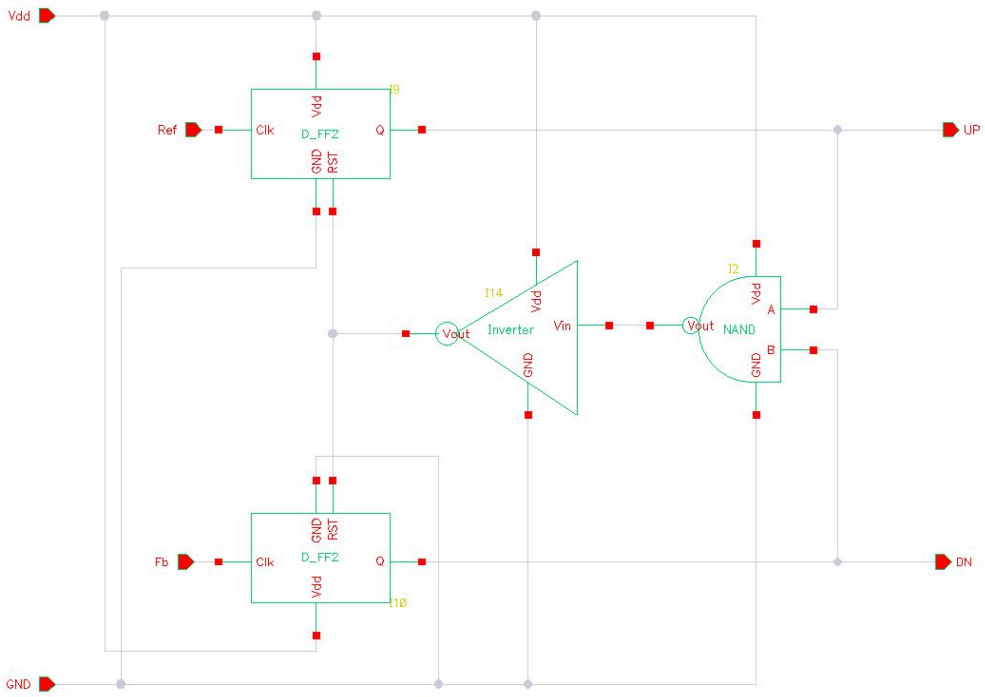

Figure 2: PFD Schematic

and 6 .

It is observed from fig 7 that due to a phase difference between the two inputs, the PFD detects it and sends a corresponding Up or Down signal.

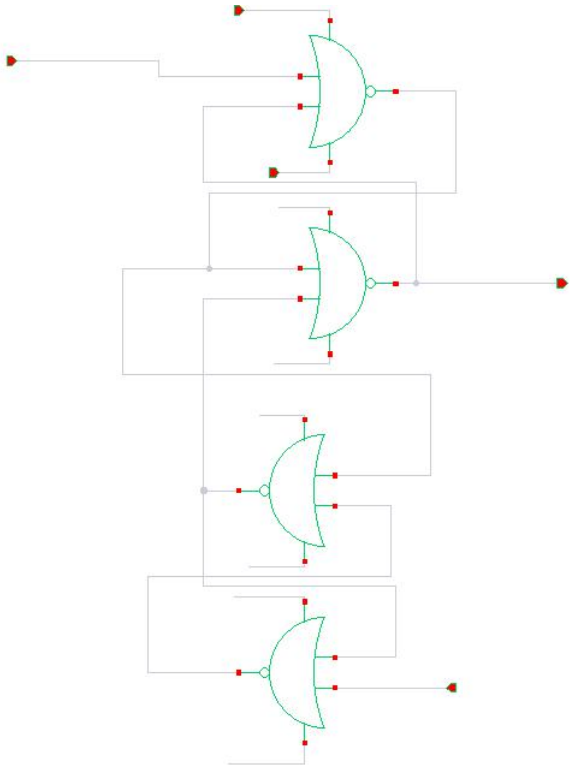

Figure 3: D- Flip Flop Schematic

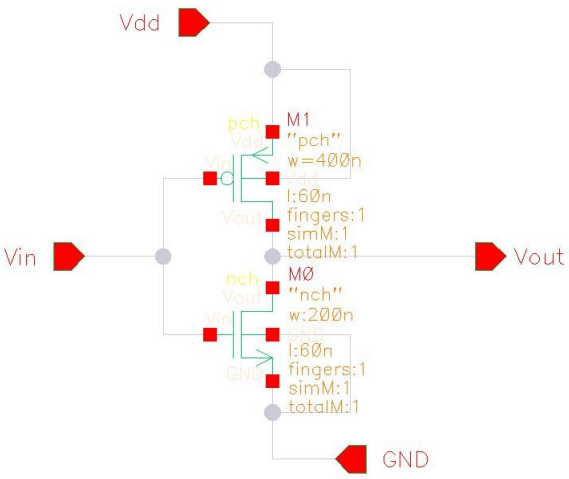

Figure 4: Inverter Schematic

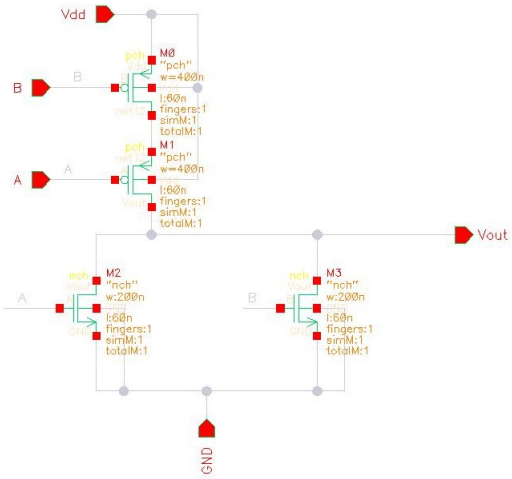

Figure 5: NOR Schematic

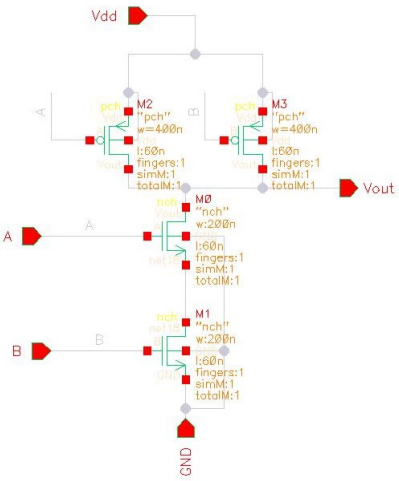

Figure 6: NAND Schematic

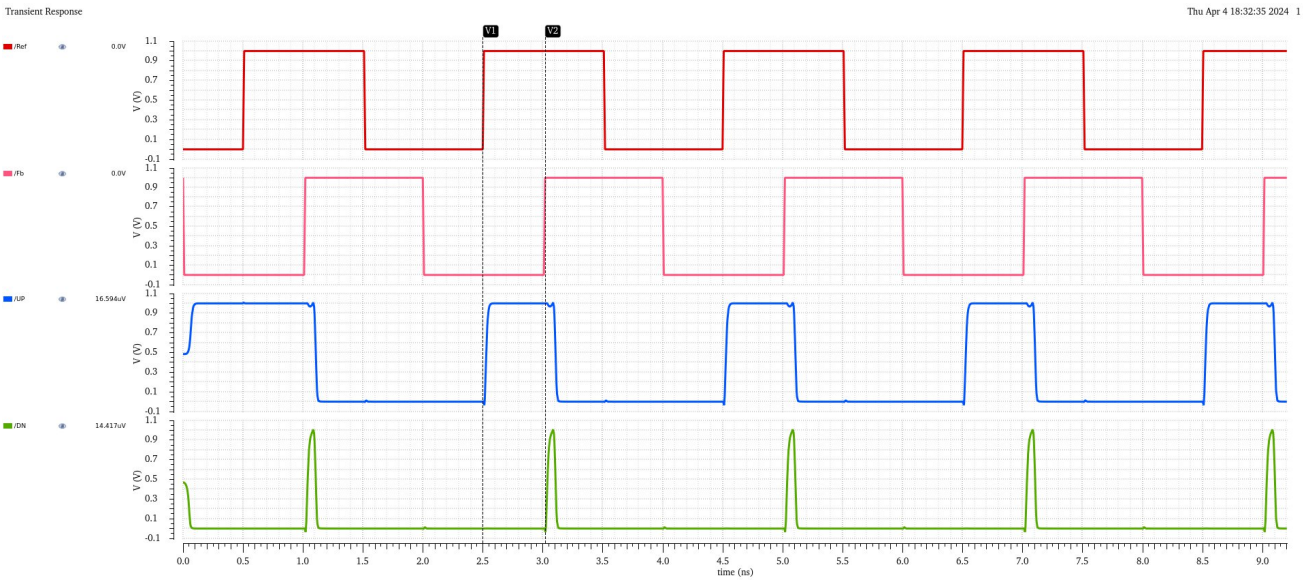

Figure 7: PFD Input (Ref, Fb) and Output (Up, Dn)

5 Charge Pump and Loop Filter

The following figure 8 shows the internal circuit of Charge Pump and Loop Filter [1].
The figure 9 shows the internal schematic of buffer which is a two-stage opamp connected in unity gain configuration .
It is observed from fig 10 that due to a phase difference between the two inputs, the PFD detects it and sends a corresponding signal to a charge pump, which averages the Up and Down signal by accumulating charge on the output capacitor and from it, an output voltage is sent. Due to phase difference, it is observed that the output voltage of the charge pump rises over time.

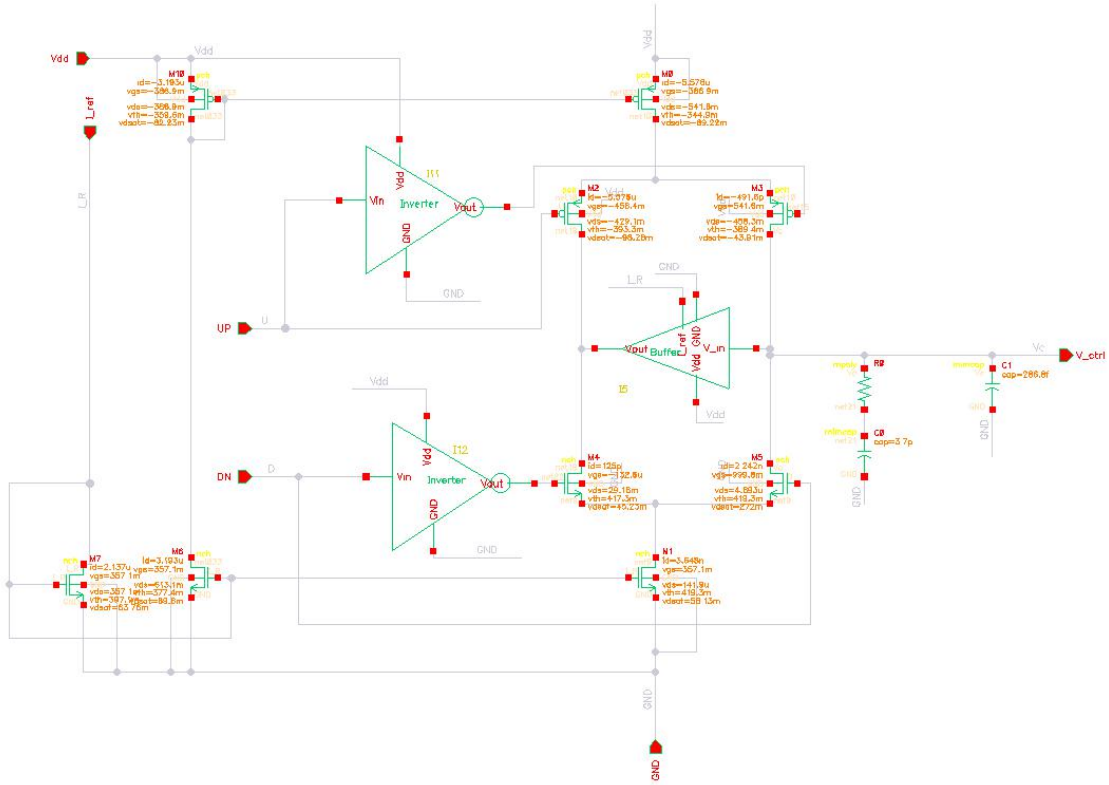

Figure 8: Charge Pump Schematic

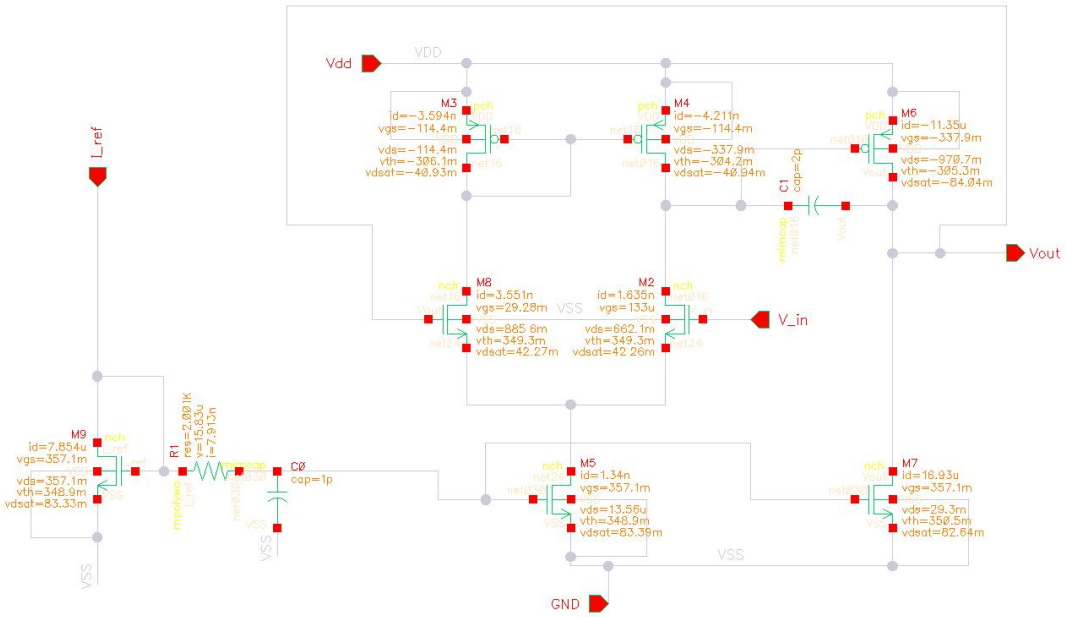

Figure 9: Buffer Schematic

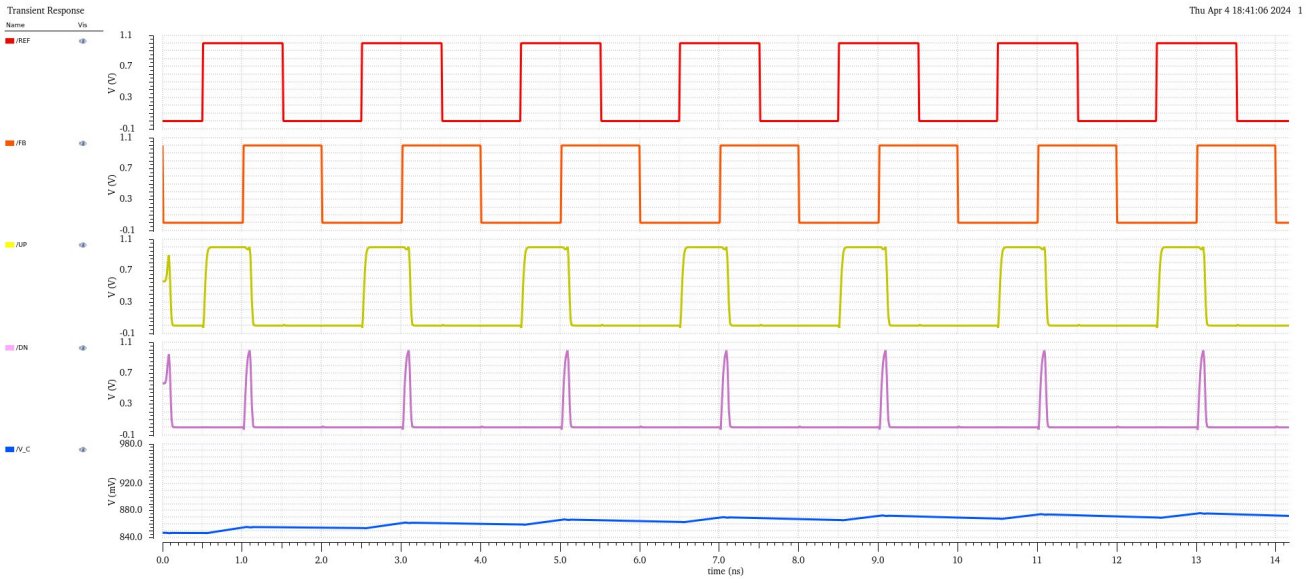

Figure 10: Charge Pump Input and Output(V_C)

6 Voltage Controlled Oscillator (VCO)

A voltage-controlled oscillator generates an output waveform of a particular frequency at a particular input voltage. Such an oscillator design has been implemented at a transistor level, and the design is commonly known as Current- Starved Ring VCO. The following figure 11 shows the internal circuit of Voltage Controlled Oscillator which has been designed using a 5-stage Current-Starved ring oscillator.

The figure 12 input and output of VCO at V = 0 Volts. .

Figure 13 shows the relation of the output oscillation frequency of VCO during a voltage sweep of the control voltage of VCO. From it, the required value of control voltage is found out for the corresponding frequency and a plot of the derivative of the output frequency versus voltage is plotted which is fig. 14, from which the KVCO is observed. The observed value of K_{VCO} for 1.2GHz output frequency is 1.88 $\frac{GHz}{V}$.

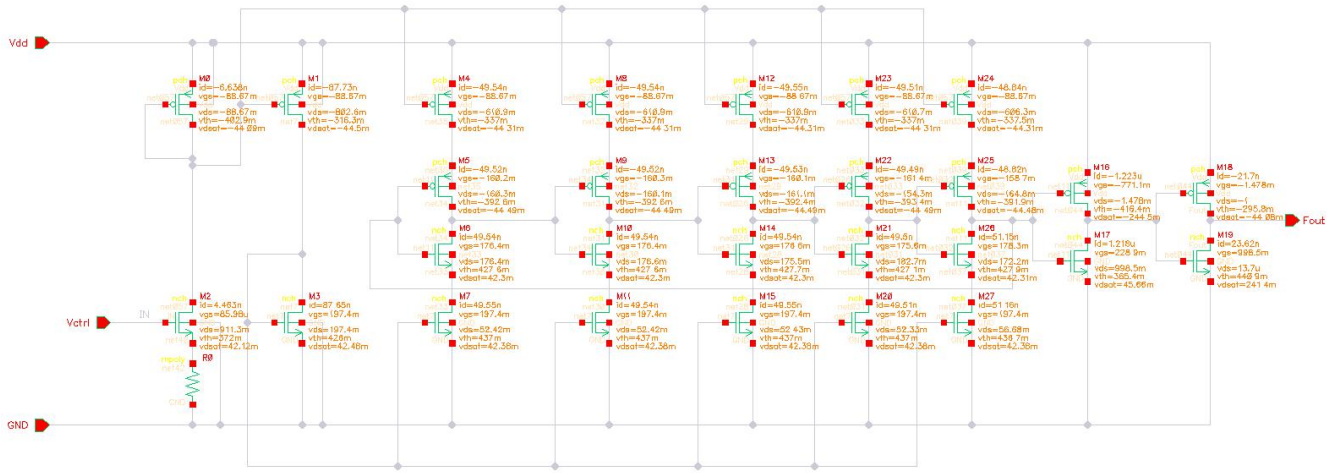

Figure 11: VCO schematic

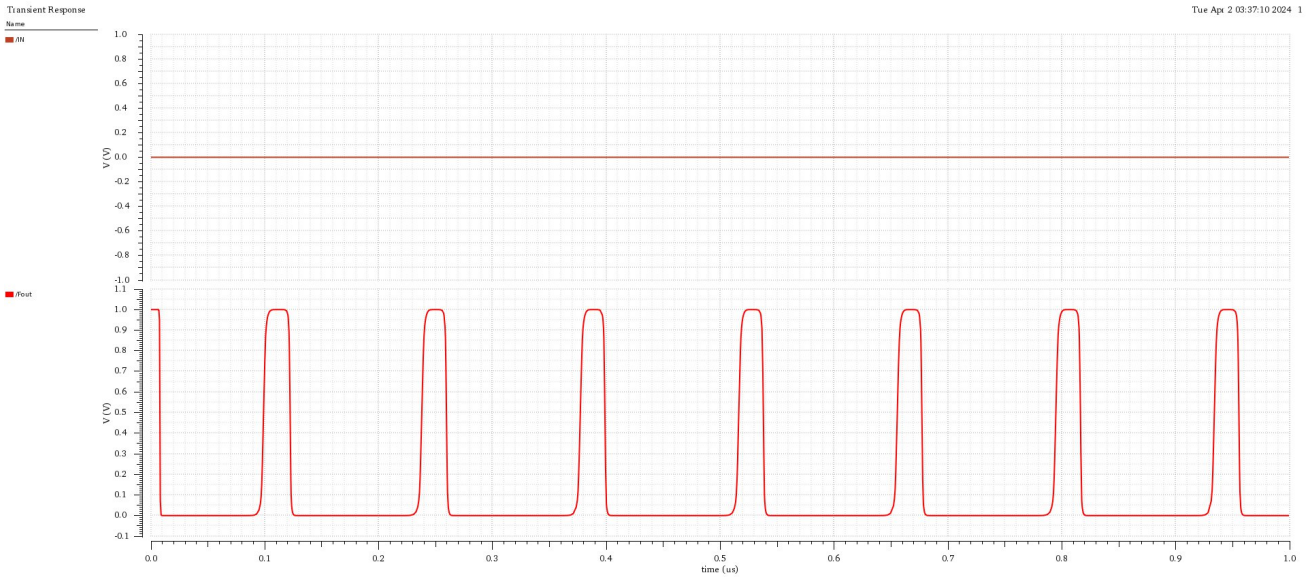

Figure 12: VCO Input and Output

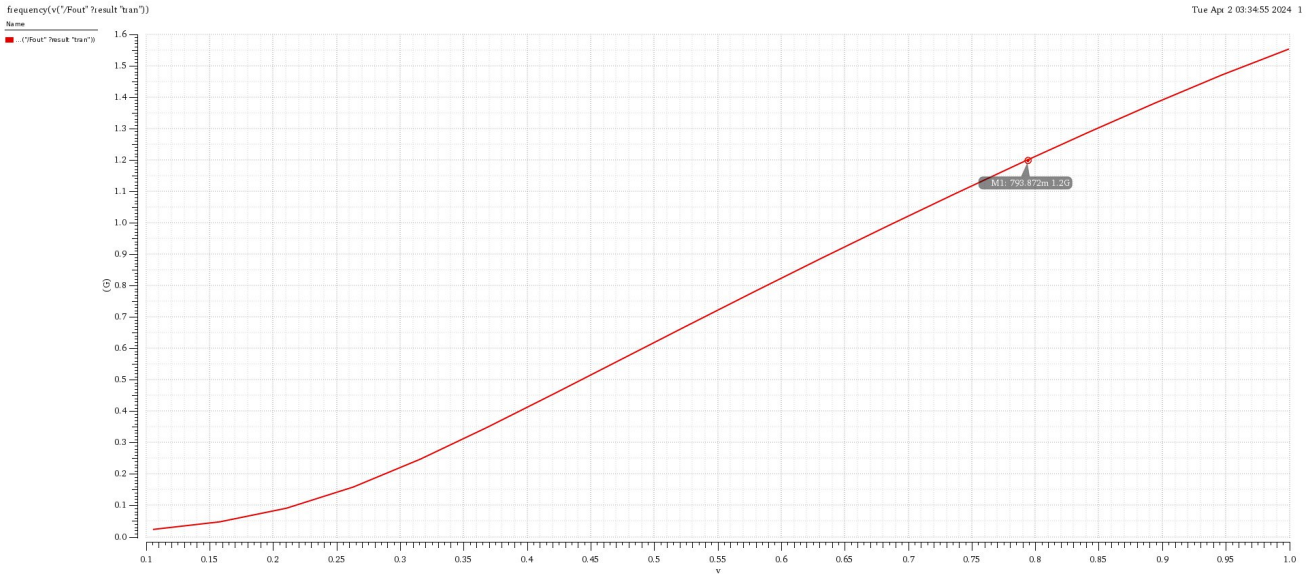

Figure 13: VCO Frequency (Hz) vs Control Voltage (Volts) Plot

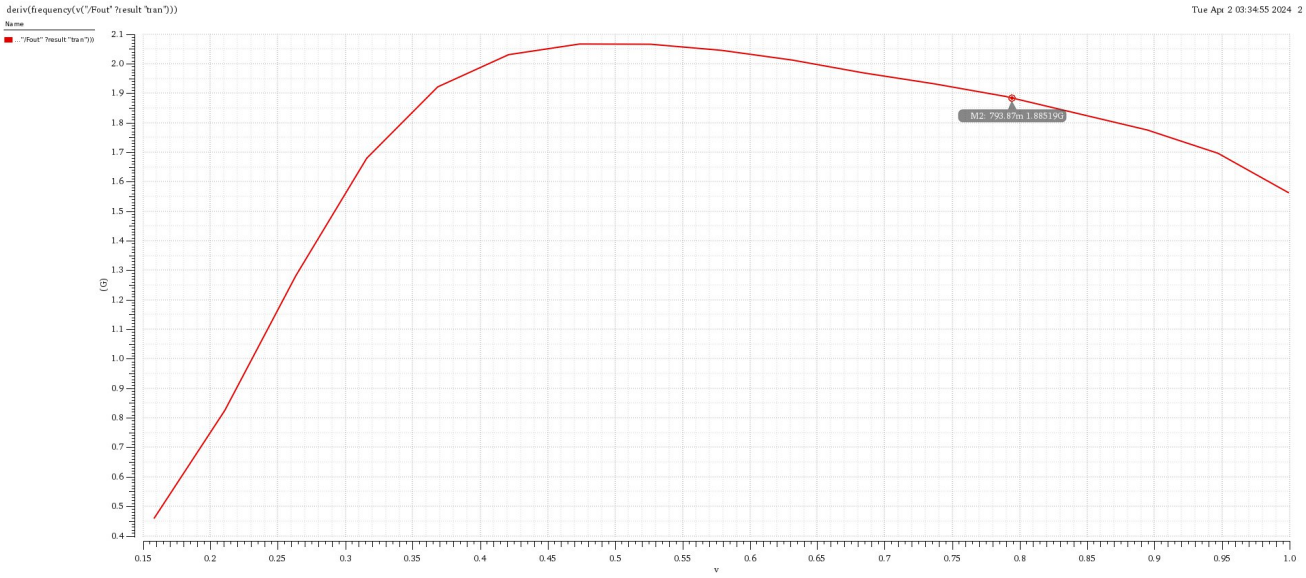

Figure 14: Value of KVCO

7 Frequency Divider

The following figure 15 shows the internal circuit of Frequency Divider which consists of 3 cascaded divide by 2 blocks.

The figure 16 shows the circuit which divides the frequency of input signal by two.

Figure 17 depicts the input and output waveform.

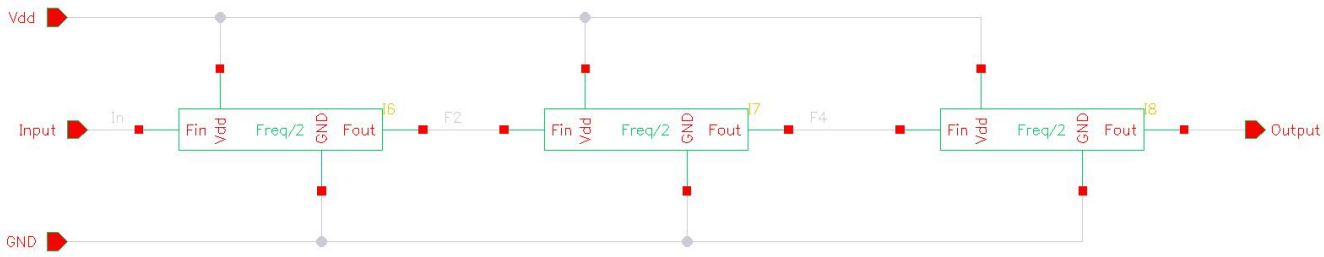

Figure 15: Frequency Divider

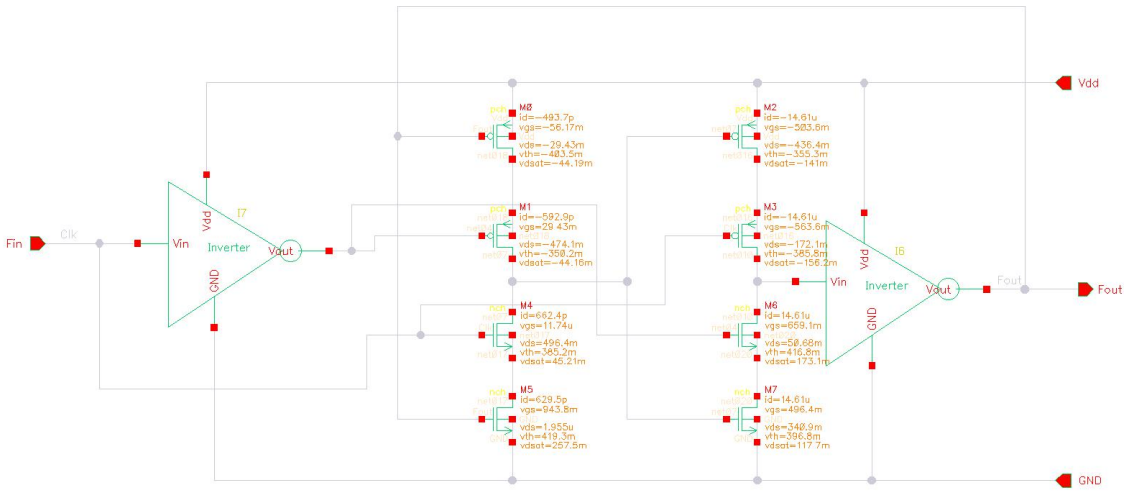

Figure 16: Divide by 2

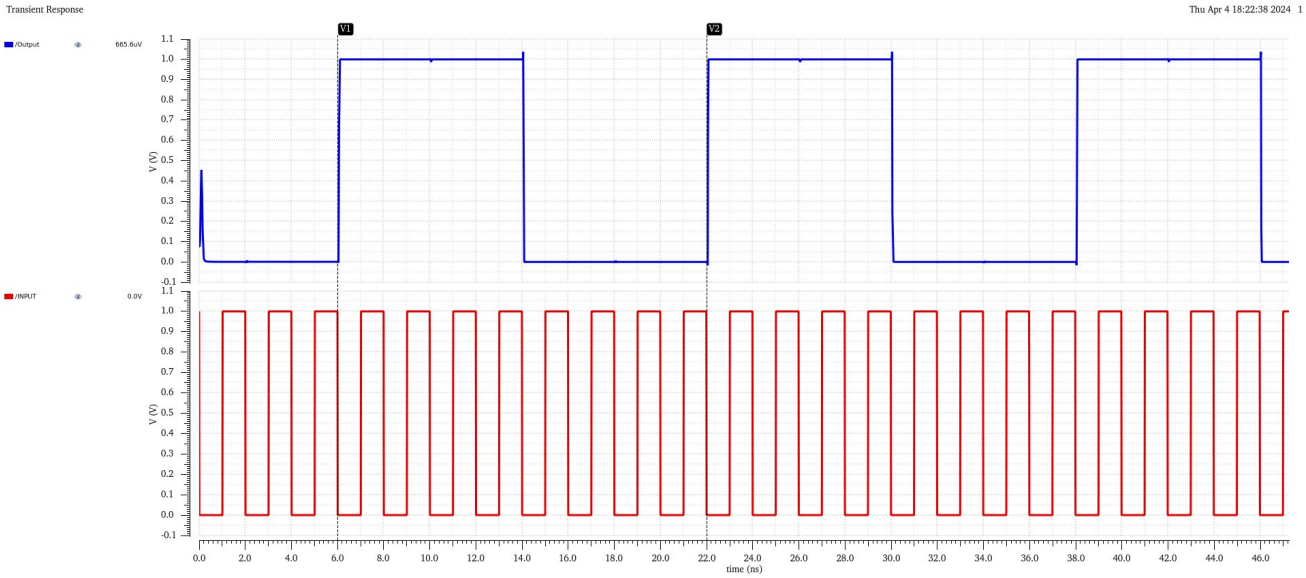

Figure 17: Frequency Divider Input and Output

8 Calculation of C_1 , C_2 and R for Loop Filter [2]

- We find ω_{ref} =2π f_{ref} = 9.42 $\times$ 10^8 rad/sec and ω_{out} =2π f_{out}= 7.53 $\times$ 10^9 rad/sec .
- We find K_{VCO} from simulation which we get around 1.88 $\frac{GHz}{V}$.
- Assuming a phase margin of 60°, we calculate b, where

$$b = 2(\tan^2(\phi_m) + \tan(\phi_m)\sqrt{1 + \tan^2(\phi_m)}) \tag{1}$$

  Thus, we get b = 12.92.

- We know, $\omega_{u,loop} = (\sqrt{b+1})\times$ ω_z. Using Gardener's constraint, $\omega_{u,loop} = \frac{\omega_{ref}}{20}$, we find the $\omega_{u,loop}$ = 4.71 $\times$ 10^7 rad/sec. Thus, ω_z = 1.26 $\times$ 10^7 rad/sec.
- We know the relation,

$$\frac{K_{VCO} \times I_o}{N} = \frac{(b+1)^{\frac{3}{2}}}{b} \times C_1 \times \omega_z \tag{2}$$

  Assuming A charge pump current of 10 μA , we calculate C_1 which turns out to be C_1 = 3.701 pF.
- We know, R = $\frac{1}{\omega_z \times C_1}$ = 21566 Ω .
- $C_2 = \frac{C_1}{b}$ = 286.98 fF

9 Results

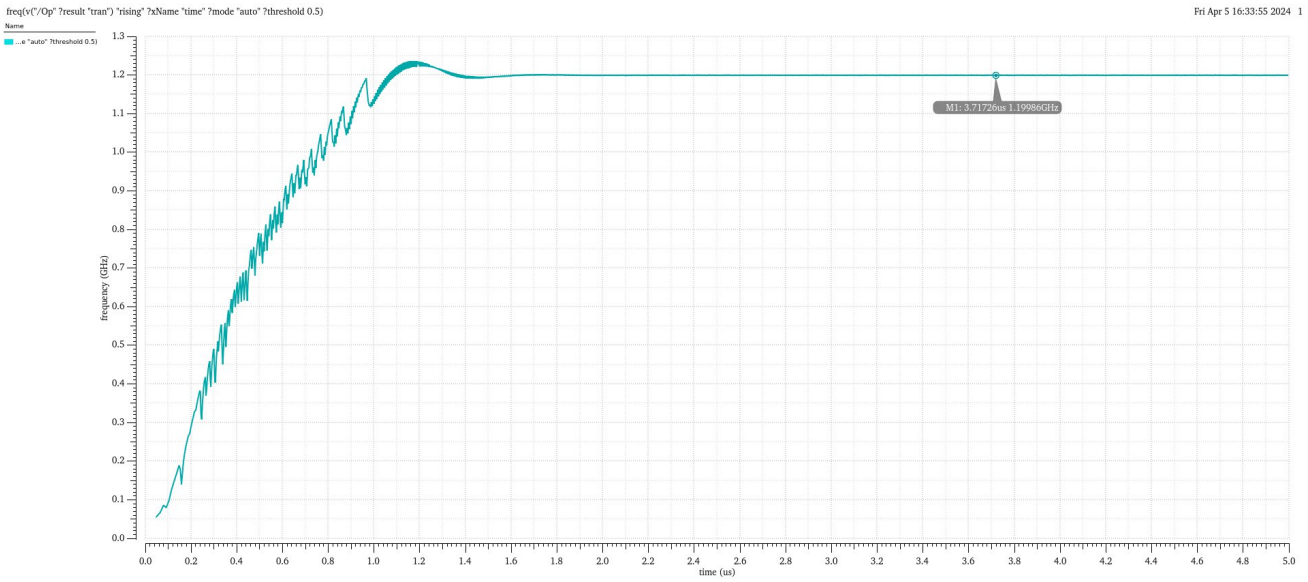

Figure 18: PLL Locking Frequency

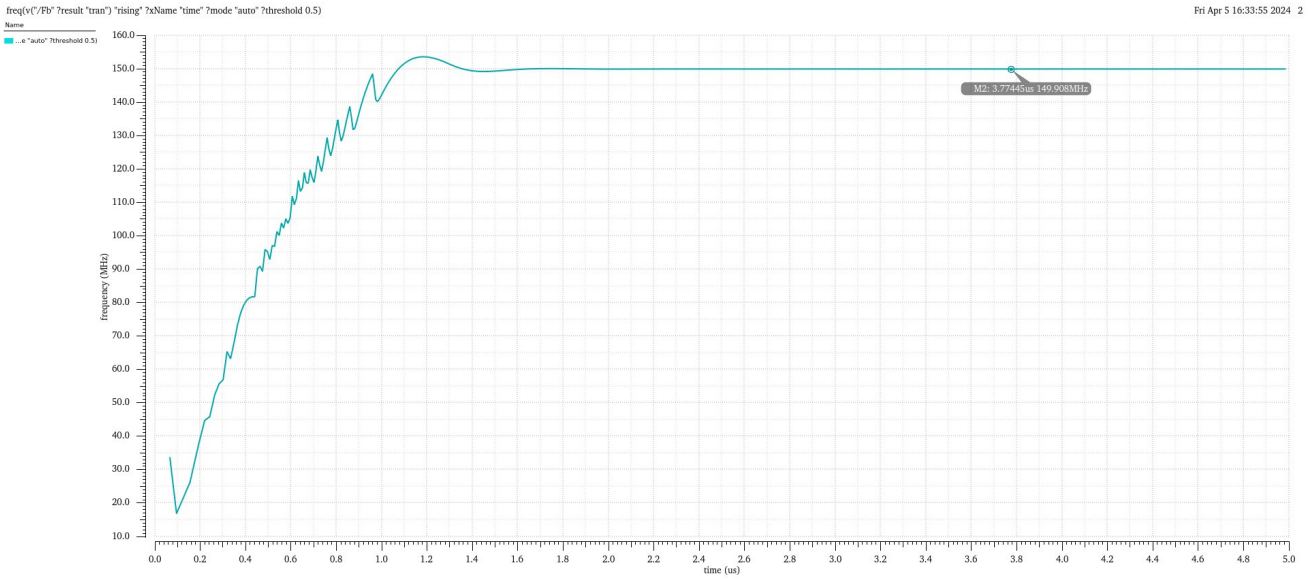

Figure 19: Output of Frequency Divider

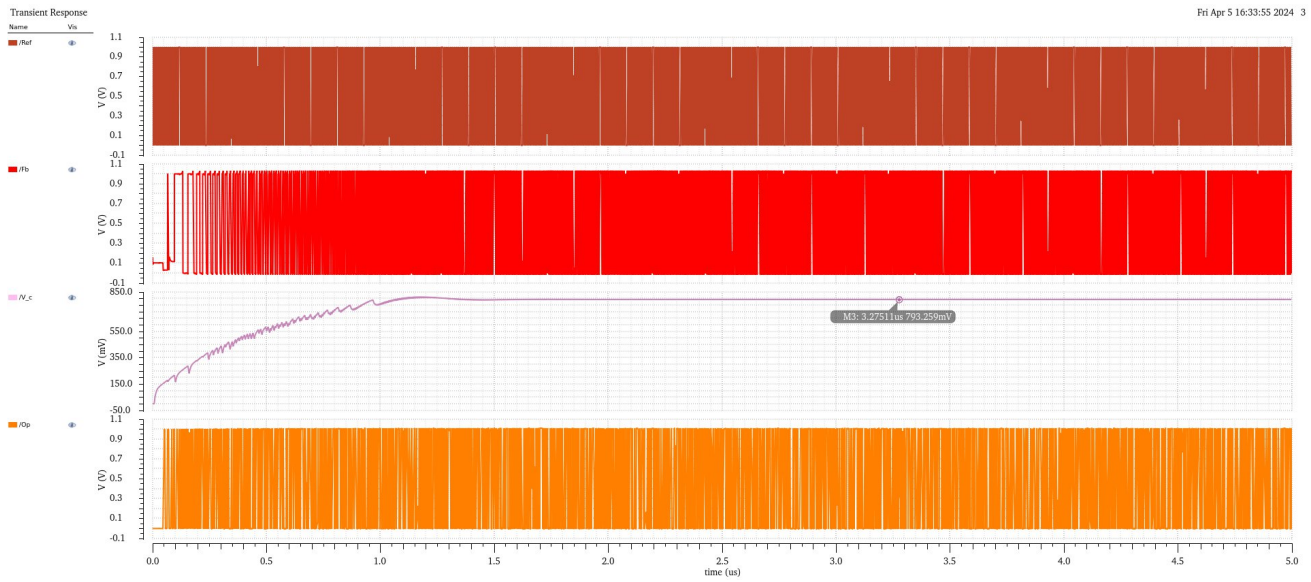

Figure 20: Input Waveform, Output Waveform and Control Voltage

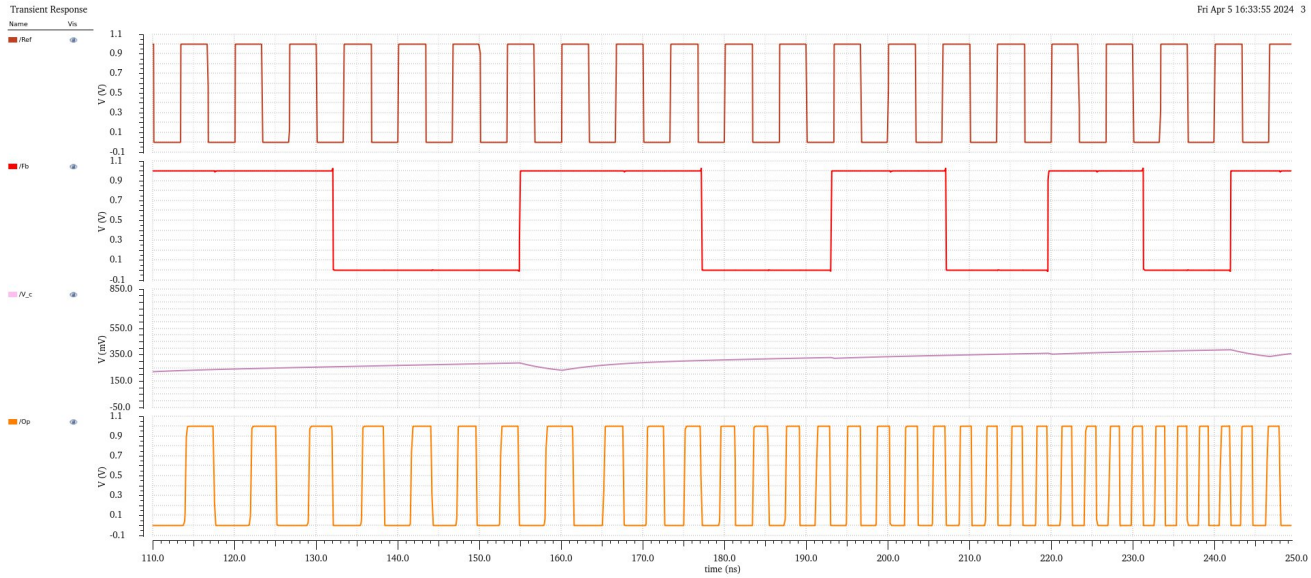

Figure 21: Input Waveform, Output Waveform and Control Voltage (zoomed-in)

Table 1: Results from simulation

Parameters	**Values**
VDD	1 V
Output Locking Frequency	1.1999×10^9 Hz
Frequency Divider Output	149.899 Mhz
Frequency Divider	8
Charge Pump Current	13.24 μA
Total Power Consumption	111.3 μW
Total Capacitance	6.98 pF
C_1	3.701 pF
C_2	286.98 fF
R	21580 Ω

10 Conclusion

The phase-locked loop locks at a frequency of 1.9999 GHz which is observed in figure 18. The output of the frequency divider after locking is observed from figure 19 at 149.899Mhz. Thus, the output frequency specification has been approximately met. The output voltage of the charge pump settles at 793 mV.

References

[1] Pavan Kumar Hanumolu, Merrick Brownlee, Kartikeya Mayaram, and Un-Ku Moon. Analysis of charge-pump phase-locked loops. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 51(9):1665–1674, 2004.

[2] Hamid R Rategh, Hirad Samavati, and Thomas H Lee. A cmos frequency synthesizer with an injection-locked frequency divider for a 5-ghz wireless lan receiver. *IEEE Journal of Solid-State Circuits*, 35(5):780–787, 2000.

[3] Behzad Razavi. *Design of CMOS phase-locked loops: from circuit level to architecture level*. Cambridge University Press, 2020.