Indirect Feedback Compensation Technique with Split Length Current Mirror in two stage OpAmp

A seminar report (Course code: EE539) submitted in partial fulfillment of the requirements for the degree of

Master of Technology

by

Ayanmani Das
(Entry No. 2023EEM1017)

Under the guidance of
Dr. Mahendra Sakare

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROPAR

2023

Declaration

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

Ayanmani Das
Entry No. 2023EEM1017

Date: 11TH December, 2023

Abstract

Indirect feedback compensation technique using split length current mirror load is studied and analysed in great depth and a comparison is drawn with direct compensation technique, popularly known as Miller Compensation. A brief introduction is given on two stage opamps and requirement of frequency compensation is emphasized for the stable operation of opamps. The main drawbacks of Miller compensation is highlighted and solutions proposed to overcome them is studied and implemented with the help of simulation, with an emphasis on indirect compensation technique's advantages.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

CMOS Operational Amplifiers , commonly known as CMOS OpAmps are one of the most important components of integrated circuit systems. The Two-stage OpAmps have been one of the most widely used analog circuit architectures. They are popularly used due to their high gain, along with simplicity in frequency compensation and relaxation in stability criteria. One of the most popular methods of compensation technique is the Miller compensation, which as also called direct compensation technique. It makes use of the pole splitting concept which is achieved by Miller capacitance multiplication effect. This tends to make the system behave like a single-pole system as because of the dominant pole effect.

One of the major drawbacks of thus technique is that a right-half-plane(RHP) zero is introduced by the Miller capacitance which reduces the phase margin of the system and lowers the unity gain bandwidth of the OpAmps. In order to tackle this, Vishal *at el.* [1] proposed a compensation technique which is known as indirect compensation technique where the feedback current which passes through the C_C from the output node to the output of the first stage is now indirectly feedback by using split -length currrent mirror load. The main aim of this report is to highlight the affects, advantages and disadvantages of the compensation technique used with respect to Miller compensation technique.

Chapter 2

Literature Survey

The Two-Stage OpAmp is a popular circuit configuration. Compensation technique is used to improve the OpAmp's stability which can be implemented by many ways. Direct compensation which is also known as Milller compensation [2] is the widely used technique which leads to a stable configuration. But it introduces as right-half-plane which degenerates the phase margin and unity gain bandwidth . Vishal *et al.* [3] [1] had done extensive work in this regard, and proposed solutions in overcoming this draawback. In [3] [1] [4] the proposed architectures were based on canceling the compensation current from the output node to the output of the first stage, which was leading cause of the existence of RHP zrero. With the blocking of the compensation current, the rhp zero was nullified which lead to better , stable systems with higher phase margin and lead to a reduction in layout size. The proposed architectures were Split-length-current mirror load and split-length-differential pair.

Chapter 3

Indirect Compensation Technique

Two-stage OpAmps are the widely used amplifier topologies in analog circuit design because of their simple frequency compensation and stability criteria. Conventionally, they have been compensated using Miller compensation or the Direct Compensation technique. The two-stage opamp consists of two stages as shown in 3.1, mainly the differential pair which gives high gain followed by the single-stage amplifier which gives gain and allows high output swing. The output buffer is used when there arises a requirement to drive a large capacitive or resistive load.

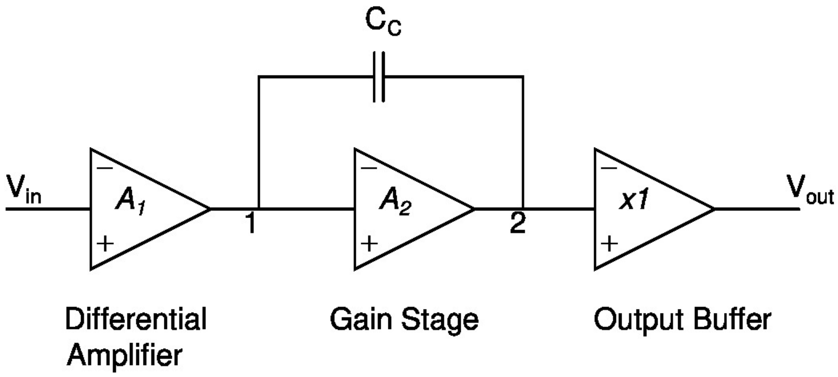

Figure 3.1: Block diagram of two-stage Opamp

3.0.1 Miller Compensation

Miller compensation is a frequency compensation technique where the compensation is achieved by pole splitting of the two poles which were close to each other when the OpAmp was uncompensated. In the uncompensated OpAmp, the poles were at $p_1 = \frac{1}{R_1C_1}$ and $p_2 = \frac{1}{R_2C_2}$ where R and C denoted the resistances and capacitances at node 1 and 2. In Miller Compsensation technique, the pole splitting is achieved by connecting a compensating capacitor between the

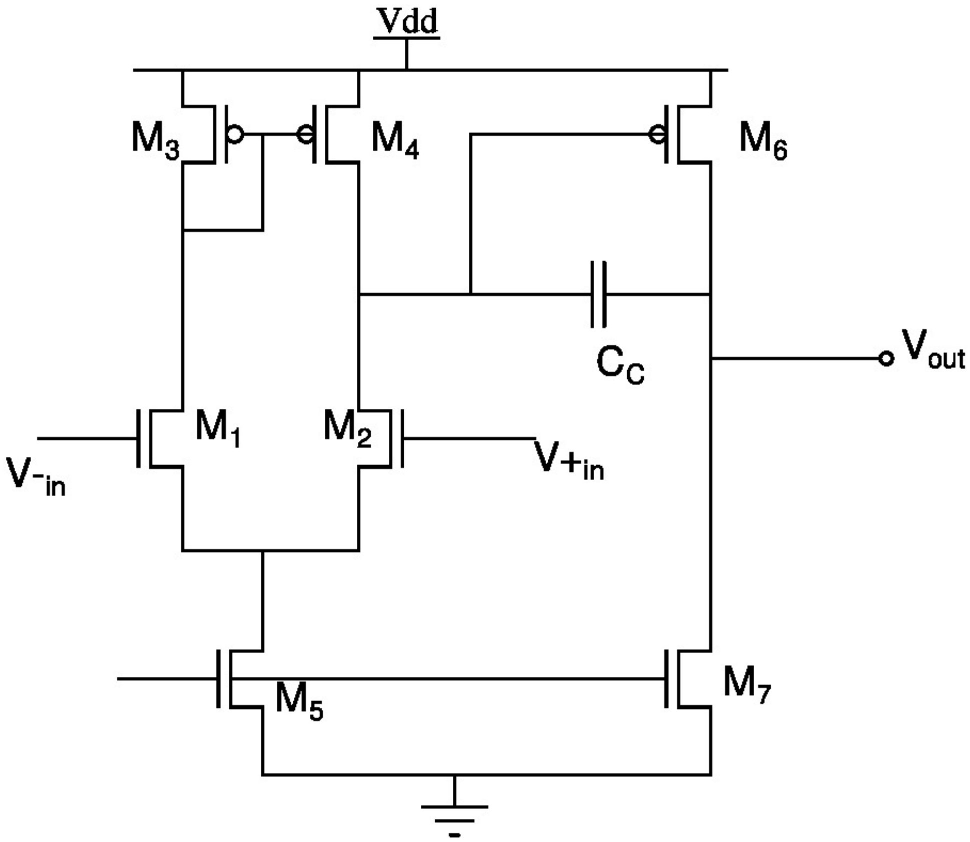

Figure 3.2: Two-stage Miller Compensated Opamp

output of the two stages. This capacitor helps to actively split the two poles which leads to one closer to the origin being the dominant pole and other being the non-dominant pole. But due to the capacitor, this generates a RHP zero which arises due to the feed-forward current from the output of the first stage to the output of the OpAmp. The transfer function of the Miller compensated two stage Opamp is

$$\frac{v_{out}}{v_{in}} = A_o \frac{(1 - \frac{s}{z})}{(1 - \frac{s}{p_1})(1 - \frac{s}{p_2})} \tag{3.1}$$

The dominant pole is located at

$$p_1 = -\frac{1}{g_{m2} R_2 R_1 C_c} \tag{3.2}$$

The non dominant pole is located at

$$p_2 = -\frac{g_{m2}}{C_1 + C_2} \tag{3.3}$$

The zero is

$$z_1 = -\frac{g_m 2}{C_c} \tag{3.4}$$

The open loop gain is $A_v = g_{m1} R_1 g_{m2} R_2$ and unity gain frequency is $f_{ugb} = \frac{g_m 1}{2\pi C_c}$. The pole splitting is shown by figure 3.3 . The RHP zero degrades the phase margin of the OpAmp and reduces the stability when the second pole moves closer to the unity gain frequency. This makes the stabilisation of the OpAMp difficult. The compensation current has twp constituents, the first being the feedforward current ($i_{fforward} = sC_c v_1$) while the second is feedback current which is ($i_{fback} = sC_c v_{out}$). When both the currents are equal and opposite to each other, then total current becomes zero which leads to 0 current flowing through the capacitor, which inturn generates a zero in the transfer function. This zero can be eliminated by blocking the feedforward current by some technique while allowing the feedback component of the compensation current in order to achieve pole splitting.

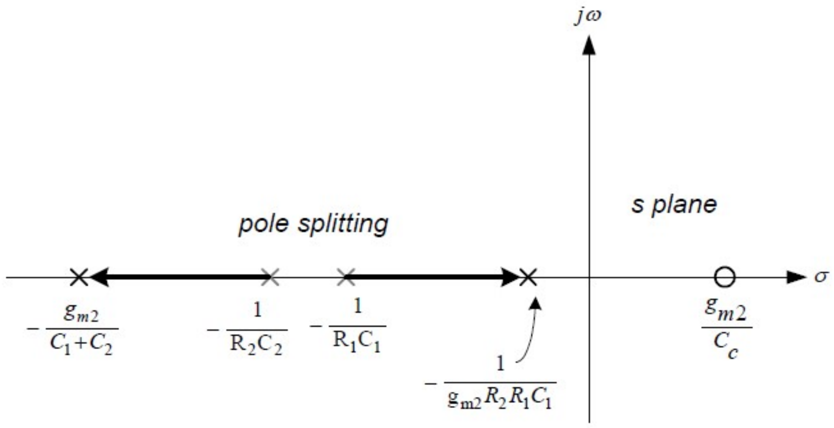

Figure 3.3: Pole splitting due to compensation technique [1]

3.0.2 Indirect Compensation

In order to cancel the RHP zero observed in Miller Compensation, the feedback current or the compensation current is fed back from the output of the OpAmp to the first stage through an internal low-impedance node in the first stage amplifier which in turn, indirectly acts like feedback mechanism which is why this class of compensation is called indirect compensation. There are many topologies which use the indirect compensation technique such as voltage buffer, split length current mirror load, split length differential pair to name a few.

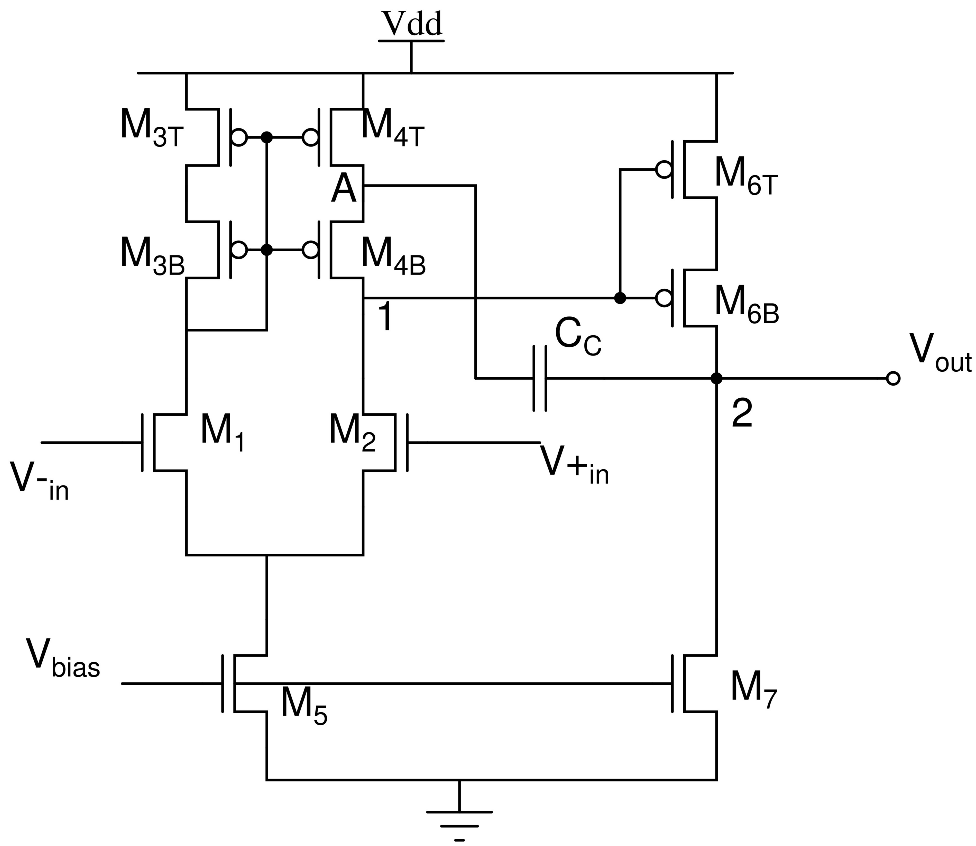

Figure 3.4: Two-stage Indirect Compensated Split Length Current Mirror Load Opamp

3.0.3 Split Length Current Mirror Load

The figure 3.4 describes the circuit architecture employing the split length current mirror load. This is a class of indirect compensation technique where, in order to obtain a low impedance node, the current mirror load transistors have been split using the split length concept a shown in figure 3.5.

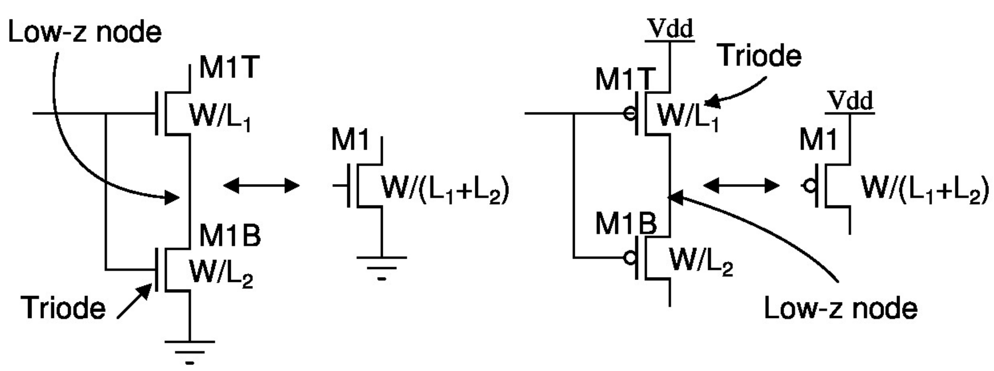

Figure 3.5: Split length NMOS and PMOS device and formation of low impedance node

For the small signal model of the opamp,the following assumptions have been made. The

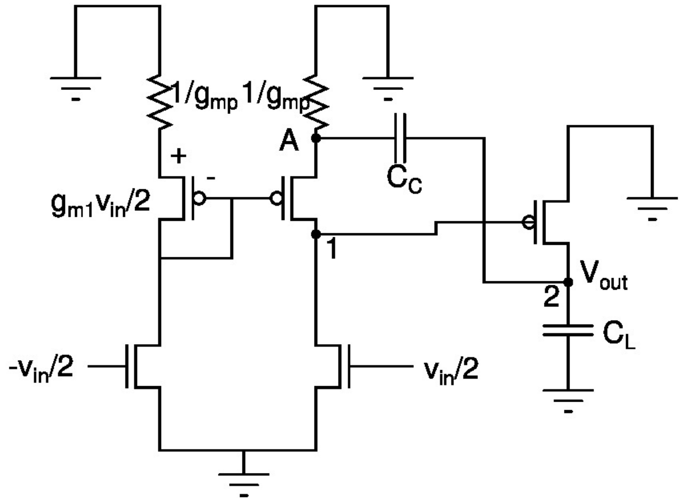

Figure 3.6: Small signal equivalent circuit with split length current mirror load (a)

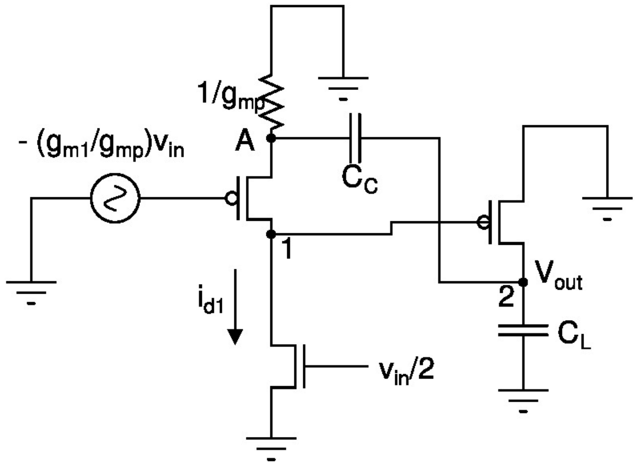

Figure 3.7: Small signal equivalent circuit with split length current mirror load (b)

transconductance of each split PMOS device is labelled as g_{mp} and the resistances and capacitances at nodes A and 1 are combined together and connected between the respective ground and nodes as shown in figure 3.6 3.7. The resistance R_A is approximately $\frac{1}{g_{mp}}$ for values of V_{SD} which are small. If the current mirror load has a transconductance same as that of the differential pair, then g_{mp} = $\sqrt{2}g_{m1}$ where g_{m1} is the transconductance of the first stage.

By applying the nodal analysis on the small signal model 3.8, and solving for the voltage and current equations at nodes 1, A and 2, the small signal transfer function is obtained which is

$$\frac{v_{out}}{v_{in}} = -A_v \frac{b_0 + b_1 s + b_2 s^2}{a_0 + a_1 s + a_2 s^2 + a_3 s^3} \tag{3.5}$$

With the assumptions that $g_{mi}R_i >> 1$, $C_2 \approx C_L$, $C_c and C_2 >> C_1 and C_A$, the following

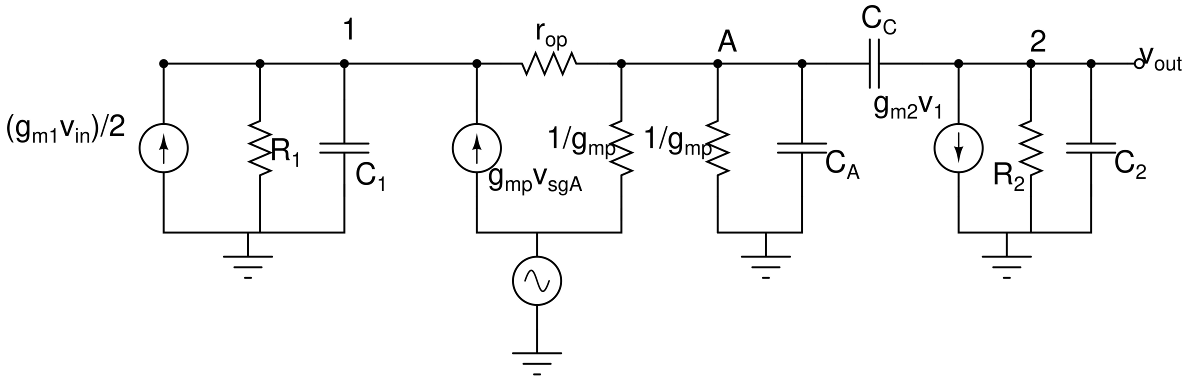

Figure 3.8: Small signal model of the circuit

transfer function coefficients are obtained

$$A_v = g_{m1}R_1g_{m2}R_2 \tag{3.6}$$

$$b_0 \approx 4g_{mp}r_{op} \tag{3.7}$$

$$b_1 \approx 3r_o(C_A + C_C) \tag{3.8}$$

$$b_2 \approx (2r_{op}C_1C_C)/g_{m2} \tag{3.9}$$

$$a_0 \approx 4g_{mp}r_{op} \tag{3.10}$$

$$a_1 \approx 2g_{m2}R_2R_2g_{mp}r_{op}C_C \tag{3.11}$$

$$a_2 \approx 4R_2C_1R_1g_{mp}r_{op}(C_2 + C_C) + 2R_2C_2[r_{op}(C_C + C_A) + R_1(C_C + C_A + C_1)] \tag{3.12}$$

$$a_3 \approx 2R_1C_1R_2r_{op}(C_2C_A + C_2C_C + C_CC_A) \tag{3.13}$$

The unity-gain frequency is at

$$f_{un} = \frac{g_{m1}}{2\pi 2C_C} \tag{3.14}$$

The first LHP zero is located at

$$z_1 \approx -\frac{b_0}{b_1} = -\frac{4g_{mp}}{3(C_A + C_C} \approx \frac{8\sqrt{2}\omega_{un}}{3} \tag{3.15}$$

This implies that the zero is 3.77 times away from unity gain frequency.

The second LHP zero is located at

$$z_2 \approx -\frac{b_1}{b_2} = \frac{-3g_{m2}}{2C_1} \tag{3.16}$$

This zero can be ignored at frequencies of interest as it is located at a high frequency.

The dominant pole is located at

$$p_1 \approx -\frac{a_0}{a_1} = \frac{1}{2g_{m2}R_2R_2C_C} \tag{3.17}$$

Assuming that the $g_{mp} >> \frac{g_{m2}C_C(C_2||(C_C+C_A)}{C_1(C_2+C_C)}$,

$$p_2 \approx -\frac{a_1}{a_2} \approx \frac{-g_{m2}C_C}{2C_1C_L} \tag{3.18}$$

$$p_3 \approx -\frac{a_2}{a_3} \approx -2[\frac{2g_{mp}}{C_2||C_C} + \frac{1}{(R_1||r_{op})}C_1] \tag{3.19}$$

Chapter 4

Results

The Miller compensated two-stage Opamp and indirect compensation technique using split length current mirror load was simulated on Cadence Virtuoso using the 65nm TSMC Process Design Kit and a comparison was done between both the simulations.

The Miller Circuit was first simulated and the open loop gain of the amplifier as well as the phase margin was observed. Similarly, the same parameters were observed for split length current mirror load.

Parameters	Miller Compensated	Indirect SLCM
Open-loop gain	49.33dB	49.72dB
Phase Margin	69°	0°
Unity-gain frequency	13.54 MHz	257.417MHz

Table 4.1: Comparison Table

From the comparison table and figures obtained from simulation, it is observed that in the frequency response of the split length current mirror load , gain peaking can be seen which indicates the presence of a LHP zero along with a pole. This had degraded the phase margin of the Opamp . It can also seen that this configuration has lead to higher unity gain frequency , indicating that a less value of compensating capacitor can be used which in-turn, reduces the area requirement of the transistor.

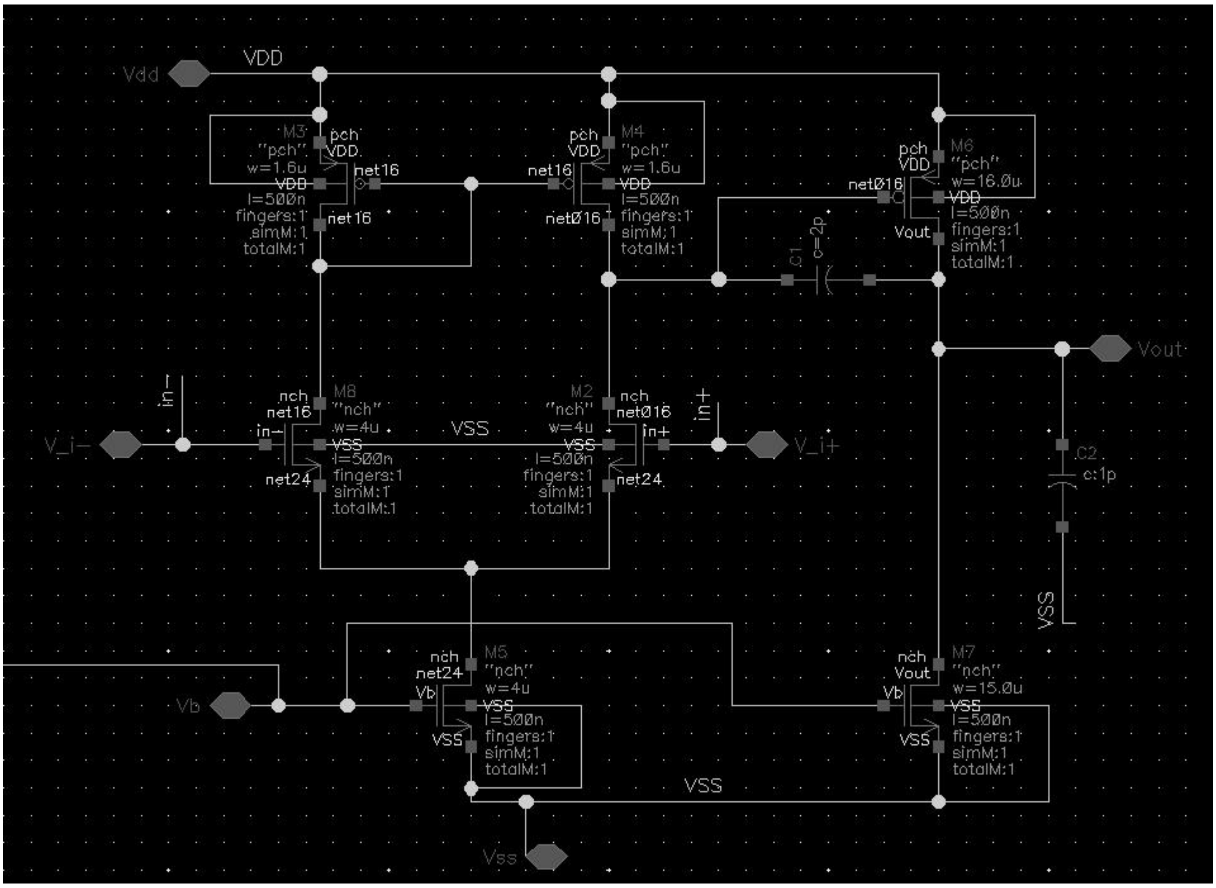

Figure 4.1: Schematic of Miller Compensated Opamp

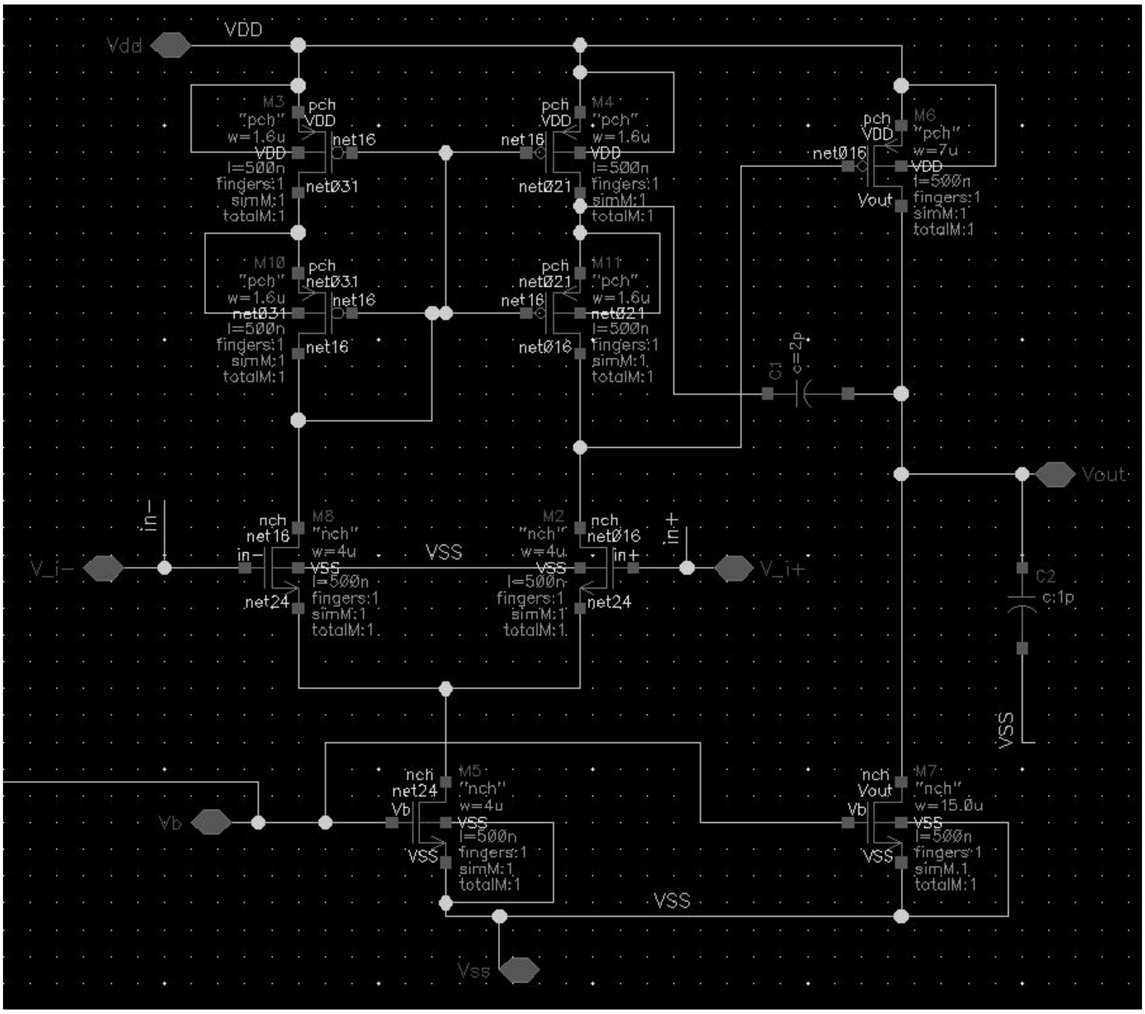

Figure 4.2: Schematic of Indirect Split Length Current Mirror Load Compensated Opamp

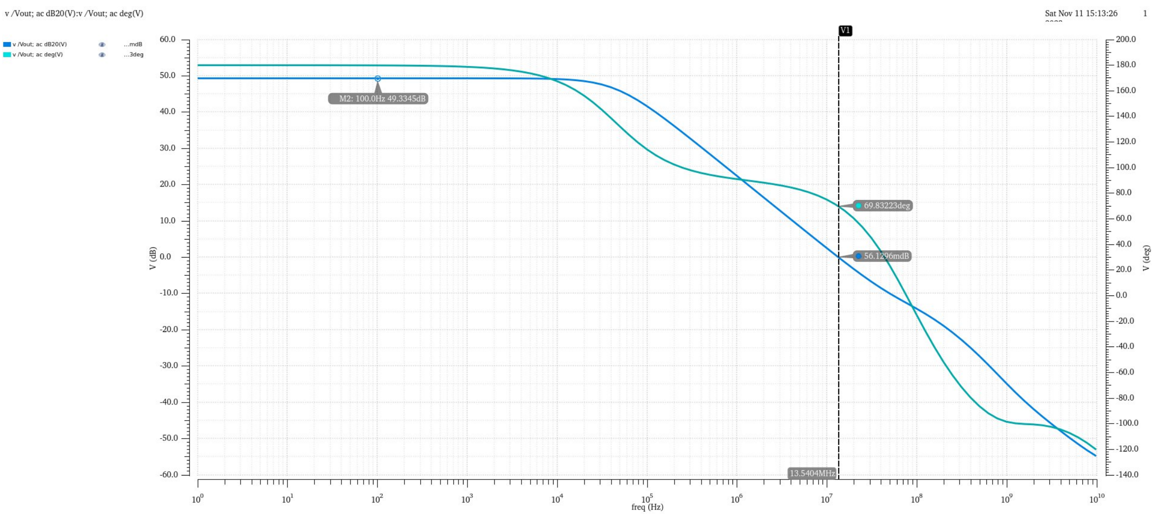

Figure 4.3: Phase Margin and Open-loop gain of Miller Compensated Opamp

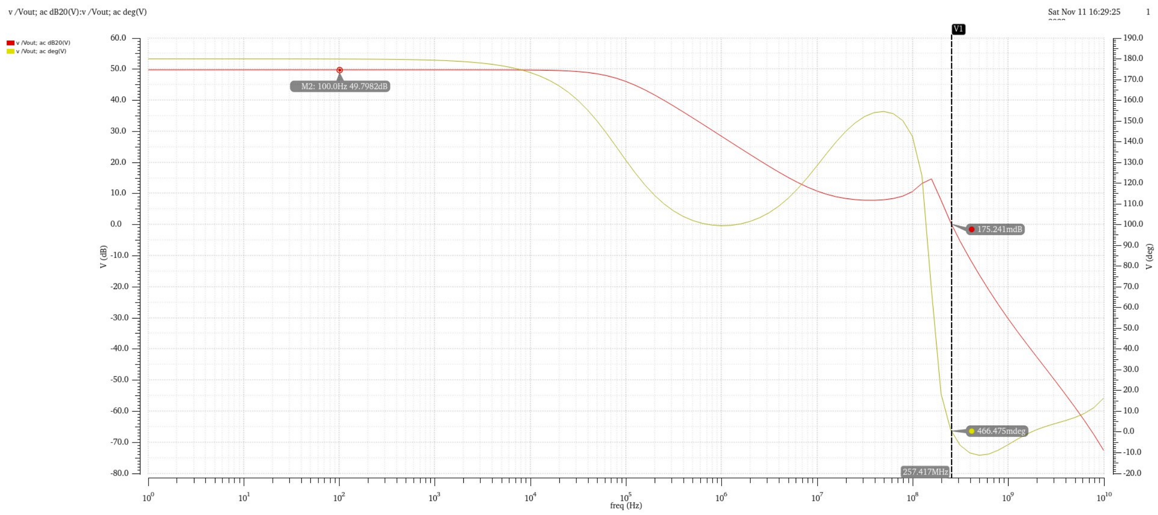

Figure 4.4: Phase Margin and Open-loop gain of Indirect Split Length Current Mirror Load Compensated Opamp

Chapter 5

Conclusion

Indirect compensation method aimed at blocking the feedforward current by providing an alternate path for the feedback of compensating current through a low impedance node. This architecture, proposed by [1] , highlighted the advantages of using this compensation technique over Miller compensation. The split length current mirror load topology had provided higher phase margin and unity gain bandwidth,along with removal of the RHP zero which was introduced by Miller Compensation. An attempt was made to reconstruct similar findings through simulation of both topologies and it was observed that the split length current mirror topology provided higher unity-gain frequency than its counterpart. One major drawback observed was the degradation of phase margin in split length current mirror topology due to gain peaking . Such shortcomings can be further investigated and rectified.

References

[1] V. Saxena, "Indirect feedback compensation technique for multi-stage operational amplifiers," 2007.

[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*. USA: McGraw-Hill, Inc., 2000.

[3] V. Saxena and R. Baker, "Indirect feedback compensation of cmos op-amps," in *2006 IEEE Workshop on Microelectronics and Electron Devices, 2006. WMED '06.*, 2006, pp. 2 pp.–4.

[4] V. Saxena and R. J. Baker, "Compensation of cmos op-amps using split-length transistors," in *2008 51st Midwest Symposium on Circuits and Systems*, 2008, pp. 109–112.