PhD Qualifier Examination
Department of Computer Science and Engineering

Date: 23-Oct-2013 **Maximum Marks:** 100

[*Answer any* five *questions from Group A, and any* five *questions from Groups B and C.*]

Group A

A.1 (a) Let $f(n), g(n)$ be two positive real-valued functions of positive (or non-negative) integers. If $f(n) = \Theta(g(n))$, prove that $g(n) = \Theta(f(n))$. **(4)**

(b) You are given an array A of size n, that may contain duplicate entries. Your task is to produce an array B with $\leqslant n$ elements that contains all the entries of A but with all the duplicates removed. If an entry occurs multiple times in A, only one occurrence of it will go to B. Apart from this constraint, the elements of B can be any permutation of the mutually distinct elements of A. Supply an $O(n \log n)$-time algorithm to solve the problem. **(6)**

A.2 Suppose that a programming language supports range checking on arrays. This means that whenever an element outside the allocation space of an array is tried to be accessed, only a warning message is generated and the program continues to run. You are given an array A of an unknown size n. How can you obtain the exact value of n in $O(\log n)$ time? You should use the warning messages appropriately. **(10)**

A.3 (a) You are given a library implementing the max-priority queue functions *init*, *insert*, *getmax* and *deletemax*. Assume that the key values for heap ordering are integers. How can you implement a stack (more precisely, the *push* and *pop* operations) using this implementation of the priority queue? Assume that the number of times the push operation is performed fits in an integer variable. **(7)**

(b) Propose a constant-time algorithm to find the second maximum value stored in a max-heap. **(3)**

A.4 (a) Define a directed acyclic graph (DAG). **(2)**

(b) How do you check whether a given directed graph is acyclic? **(3)**

G (c) Let $G = (V, E)$ be a DAG with $|V| = n$. A *Hamiltonian path* in G is a path in G of length $n-1$ (that is, a path on which all vertices of G appear). Propose an $O(|V| + |E|)$-time algorithm to determine whether G contains a Hamiltonian path. (**Hint:** Use topological sorting.) **(5)**

A.5 (a) Suppose that some edge costs in a directed graph G are negative. Make all edge costs positive by adding a fixed positive bias to each cost. Then, run Dijkstra's algorithm on this updated graph. Give an example to demonstrate that this algorithm may fail to give the shortest paths in the original graph. **(5)**

G (b) Let $G = (V, E)$ be a connected undirected graph with each edge carrying a positive cost. A *maximum spanning tree* of G is a spanning tree T of G such that the sum of the costs of the edges in T is as large as possible. Propose an efficient algorithm to compute the maximum spanning tree of G. **(5)**

A.6 Write a C function that, upon the input of a string S, prints a substring of S which is a palindrome and of length as large as possible. **(10)**

A.7 (a) Propose a C data type for representing binary trees. Assume that each node of the tree contains an integer key value and two child pointers only. **(3)**

(b) Write a C function that, upon the input of a binary tree represented as in Part (a), returns the number of leaves in the tree. **(7)**

A.8 (a) Propose a C data type for storing an undirected graph in the adjacency-list representation. **(3)**

G (b) Let G be a simple undirected graph. An *Eulerian tour* in G is a closed walk on the graph on which every edge of G appears exactly once. It is known that a simple connected undirected graph G contains an Eulerian tour if and only if each vertex of G has even degree. Write a C function that, upon the input of a simple connected undirected graph G in the representation of Part (a), returns the decision whether G contains an Eulerian tour. **(7)**

Group B

B.1 Solve the recurrence relation $S(k) - 4S(k-1) + 3S(k-2) = 3^k$ with the initial conditions $S(0) = 1$ and $S(1) = 2$. **(10)**

B.2 Show that if any five distinct integers from 1 to 8 are chosen, then two of them will have a sum of 9. **(10)**

B.3 A box contains 7 red and 13 blue balls. Two balls are selected at random and are discarded without their colors being seen. If a third ball is drawn randomly and observed to be red, what is the probability that both of the discarded balls were blue? **(10)**

B.4 (a) Given two languages L_1 and L_2, the right quotient L_1/L_2 of L_1 with respect to L_2 is defined as $L_1/L_2 = \{x \mid \exists y \in L_2, xy \in L_1\}$. Prove that if both L_1 and L_2 are regular, then L_1/L_2 is regular. **(5)**

(b) Let $L = \{0^i x \mid i \geqslant 0 \wedge x \in \{0,1\}^* \wedge |x| \leq i\}$. Prove that L is not regular. **(5)**

B.5 Consider the language, $L = \{x \in \{0,1,2\}^* \mid x$ does not contain the substring $01\}$.

(a) Construct a DFA (deterministic finite automaton) which recognizes L. **(3)**

(b) For all $i \geqslant 0$, let $T(i)$ denote the number of strings of length i in L. Construct a recurrence relation over $T(i)$ along with initial conditions $T(0)$ and $T(1)$. **(5)**

(c) Prove that $T(i) = F_{2i+1}$ (the $(2i+1)$-st Fibonacci number). **(2)**

(**Hint:** You may use the sets $S(q,i)$ of strings of length i for which the state q is reachable starting from any initial state.)

B.6 (a) Provide a context-free grammar which is equivalent to the language corresponding to the regular expression $(011+1)^*(01)^*$. **(5)**

(b) A *counter automaton* is a PDA (pushdown automaton) with just two stack symbols, A and Z_0, for which the string on the stack is always of the form $A^n Z_0$ for some $n \geqslant 0$. In other words, the only possible change in the stack contents is a change in the number of A's in the stack. Construct a counter automaton which accepts the language $L = \{x \in \{0,1\}^* \mid n_0(x) = n_1(x)\}$, where $n_0(x)$ and $n_1(x)$ denote the number of 0's and 1's in the string x respectively. **(5)**

Group C

C.1 (a) Realize the following switching function using an 8:1 MUX — assume that the MUX has no enable/disable inputs. $f(w,x,y,z) = \Sigma(1,5,7,8,11,13,15)$. **(4)**

(b) A communication system is designed to transmit just two codewords: $A = 0010$ and $B = 1101$. However, owing to noise in the system, the received word may have as many as two errors. Design a combinational circuit, which upon the input of the received 4-bit codeword, can correct one error and can detect the presence of two errors. The circuit has the interface as shown in Fig. 1. Output A is 1 if the received codeword is inferred to be A; output B is 1 if the received codeword is inferred to be B, and output C is 1 if there are two errors in the received codeword. Find the minimized logic expressions for A, B and C (no need to draw the logic diagrams). **(6)**

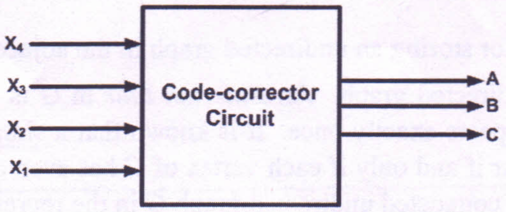

Figure 1: Code-corrector circuit.

C.2 It is required to design a sequential circuit with one input line and one output line such that the circuit produces an output 1 whenever the pattern 10 occurs after two 01 patterns with some intervening 0s and 1s among them. Overlapping input subsequence satisfying the above property should also produce output 1. Initially, you can assume that the output is 0. A sample stream of input and another of output are shown below:

```
i/p :  1 0 0 1 0 0 0 1 1 1 0 1 0 1 0 0 0 0 ...
o/p :  0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 ...
```

(a) Give a state transition diagram designating the initial state, and ensuring minimum number of states. **(5)**

(b) Assuming JK flip-flops as the state elements, derive the Boolean logic expressions (no circuit diagram needed) for the J- and K-inputs of any one of the FFs, and the output. Show the relevant K-maps. **(5)**

C.3 (a) State three distinguishing features of a RISC architecture. **(2)**

(b) Consider a memory system with two levels of cache (L1 and L2), with the following parameters:

Access time of main memory: 150 nsec
Access time of L2 cache: 50 nsec
Access time of L1 cache: 20 nsec

The hit ratios for the L1 and L2 caches are 99% and 75% respectively, where the L2 hit ratio is calculated with respect to the residual memory accesses which result in L1 miss. Calculate the overall access time of the memory hierarchy. **(4)**

(c) It is required to construct a 64 Mbytes memory system by connecting four memory modules of size 16 Mbytes each. Draw a schematic diagram clearly showing how the memory modules will be connected to the address and data buses of the processor. **(4)**

C.4 (a) In a floating-point number representation, what is the basic purpose of: **(2)**

i) Biasing of the exponent
ii) Normalization of the mantissa

(b) A processor has a single interrupt line through which any external device can send an interrupt request. It is required to connect 8 external devices to the interrupt line. Draw a schematic diagram for a possible solution to this problem, clearly stating how the respective interrupt handlers will get invoked. **(5)**

(c) "Modern processors implement a combination of hardwired control and microprogramming." Justify or contradict this statement. **(3)**

C.5 (a) A system using demand-paged memory takes 250 ns to satisfy a memory request if the page is in memory. If the page is not in memory, the request takes on an average 5 ms if a free frame is available or the page to be swapped out has not been modified or 12 ms if the page to be swapped out has been modified. What is the effective access time if the page fault rate is 2% and 40% of the time the page to be replaced has been modified? **(5)**

(b) Explain thrashing and its impact on the system performance. **(2)**

(c) Suppose that a machine's instruction set includes an instruction named swap that operates as follows (as an indivisible instruction):

```
Swap(Boolean a, Boolean b)
{
    Boolean t;
    t := a;
    a := b;
    b := t;
}
```

Show how swap can be used to implement mutual exclusion. **(3)**

C.6 (a) Consider the set of the process given in the following table and the following scheduling algorithms:

i) First-Come First-Served
ii) Round Robin (quantum = 2)
iii) Round Robin (quantum = 1)

Process	Arrival Time	Burst time
A	0	4
B	2	7
C	3	3
D	3.5	3
E	4	5

If there is tie within the processes, the tie is broken in the favor of the oldest process.

i) Draw the Gantt chart and find the average waiting time and response time for the algorithms. Comment on your result which one is better and why?

ii) If the scheduler takes 0.2 unit of CPU time in context switching for the completed job and 0.1 unit of additional CPU time for incomplete jobs for saving their context, calculate the percentage of CPU time wasted in each case. (7)

(b) Consider the two-dimensional array A:

```
int A[][] = new int[100][100];
```

where A[0][0] is at location 200, in a paged system with pages of size 200. A small process is in page 0 (locations 0 to 199) for manipulating the matrix; thus, every instruction fetch will be from page 0. For three page frames, how many page faults are generated by the following array initialization loops, using LRU replacement, and assuming page frame 1 has the process in it, and the other two are initially empty: (3)

```
I. for (int j = 0; j < 100; j++)
       for (int i = 0; i < 100; i++)
           A[i][j] = 0;

II. for (int i = 0; i < 100; i++)
       for (int j = 0; j < 100; j++)
           A[i][j] = 0;
```