DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

PhD Comprehensive Examination, Paper II

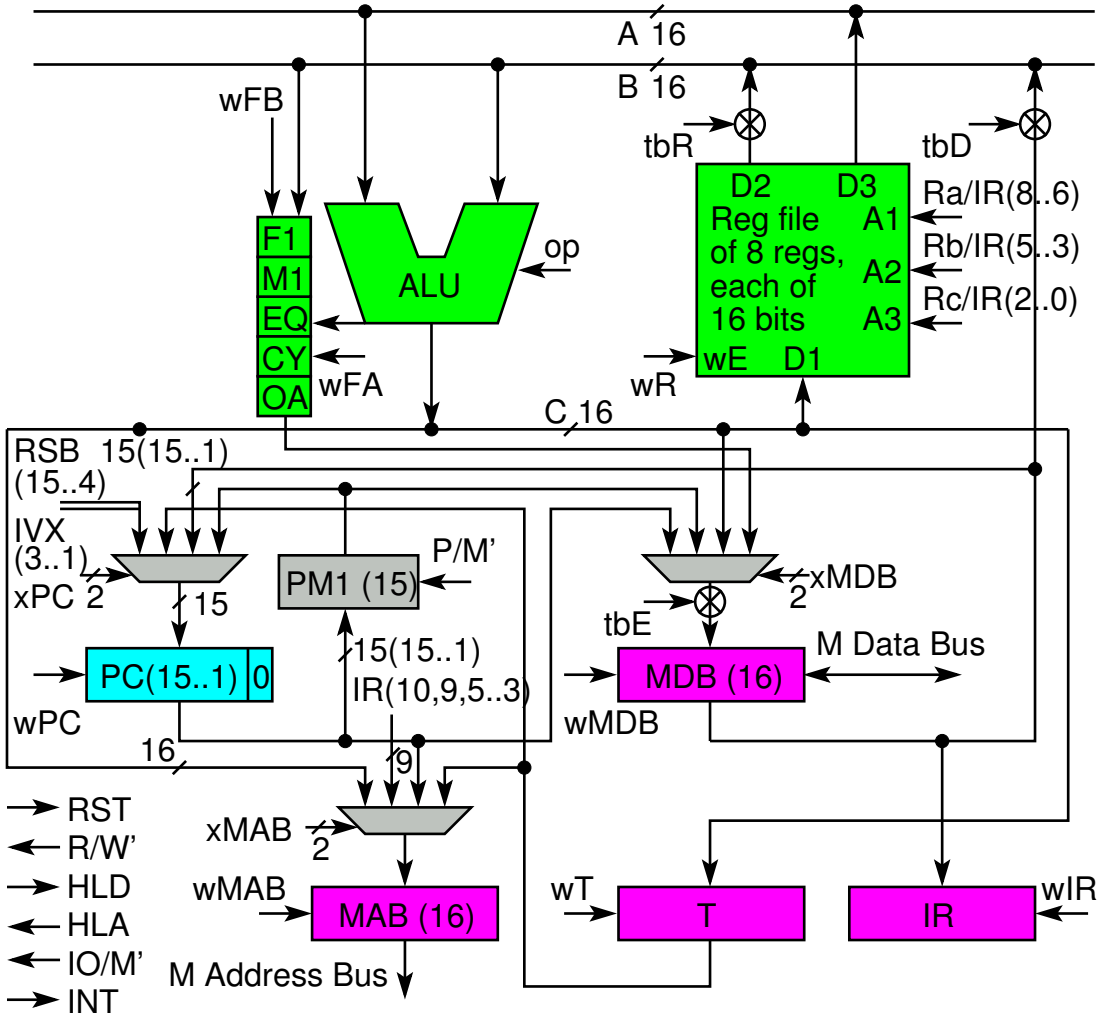
Total time: 3 Hours **October 07, 2010** **Maximum Marks: 120**

Answer from ALL the three parts

Part A: Computer Organisation and Architecture

Answer FOUR questions in this part

A.1 Consider the CPU in the given figure.



tbX: tristate output of X to bus (eg. tbD); wX: write/latch to X (eg. wIR, wMDB)
MemR/W'=1:Data from Mem to bus; MemR/W'=0: Data from bus to Mem
xMUX: select input of MUX; IV: interrupt vector; VBA: vector base address
xFA: set flags from ALU; wFB: set flags from bus; R/W': memory read/write'
F1, M1, EQ, CY,OA: various flags set depending on ALU operation and output

The `LDX R Rx M` instruction for loading register **R** (indicated as **rrr**) with the contents of the memory location **M** at an offset equal to the contents of **Rx** (indicated as **xxx**) consists of the main instruction as `11110--rrrxxx-----` followed by the 16-bit memory address **M**.

Ignoring details in the data path not relevant to this instruction, list the micro-operations, wrt the given data path, to carry out this, beyond fetching the first instruction word. 10

A.2 List out the steps for performing $15 \div 14$ using restoring or non-restoring division using registers A, Q and M so that the dividend is loaded in the Q register as: 01111, the divisor is loaded in the M register as: 01110 and the accumulator A is intially zeroed as: 00000. 10

A.3 A CPU uses memory addresses of 32 bits. Its main memory is made up of several memory modules. Each main memory module can store 2 Mi bytes (1Mi = 2^{20}) and has a chip select (CS) pin (module enabled if CS=1, memory data port tristated if CS=0). Main memory word size is of 2 bytes (data port has 16 bits). Each line of the cache is divided into 4 slots of 4 bytes each. Describe with the help of a labelled diagram, the interleaved organisation of the main memory (using the main memory modules) so that transfer between the main memory and the cache happens in the unit of a complete cache line. 10

A.4 i) What are the typical stages involved in the pipelined execution of instructions (state them in order)? Briefly explain the operation of each stage. 3

ii) What are data hazards and how are those handled in a pipelined CPU? 4

iii) What are control hazards and how are those handled in a pipelined CPU? 3

A.5 A DMA based disk controller wants to transfer 4096 bytes of data from its local buffer to an address in the main memory by cycle stealing DMA. Explain how the DMA controller will achieve this, indicating in particular the following:

i) The overall conduction of the transfer. 3

ii) What are the bus signals used by the CPU and the DMA controller for this job? 3

iii) How the contention of the bus between the CPU and the DMA controller for transferring data to the memory is resolved. 2

iv) How the transfer is properly completed. 2

Part B: Operating Systems

Answer ALL questions in this part

B.1 A program contains a loop that executes 50 times. The loop contains a computation that lasts 50 milliseconds followed by an I/O operation that consumes 200 milliseconds. This program is executed in a round robin time-sharing system with 9 other identical processes. All processes start their execution at the same time. The scheduling overhead of the OS is 3 milliseconds. Compute the total waiting time for a process if the time slice is 50 milliseconds. 10

B.2 A process makes r page references during its execution. The page reference sequence (string) of the process contains d distinct page numbers in it ($d \leq r$). The process is allocated f page frames all through its execution.

i) What is the least number of page faults that can occur during its execution?

ii) What is the maximum number of page faults that can occur during its execution?

Justify your answer. 10

B.3 A barbershop consists of a waiting room with n chairs, and a barber room with one barber chair. If there are no customers to be served, the barber goes to sleep. If a customer enters the barbershop and all chairs are occupied, then the customer leaves the shop. If the barber is busy, but chairs are available, then the customer sits in one of the free chairs. If the barber is asleep, the customer wakes up the barber. Suggest a solution to coordinate the barber and the customers using semaphores. 10

B.4 In a multiprocessor system, there are several processors which access a common shared memory module M. Only one processor can access a memory location in M at a time. Suggest an implementation of semaphore in such a scenario. 10

Part C: Programming

Answer ALL questions in this part

C.1 Consider rectangles with sides parallel to x and y-axis. Suppose that such a rectangle is specified by its top left corner and bottom right corner.

i) Define a C data type **`POINT`** to represent a point in 2-d space. 4

ii) Define a C data type **`RECTANGLE`** to represent a rectangle with sides parallel to x and y axis. 4

iii) Write a C function **`int FindArea(RECTANGLE R1, RECTANGLE R2)`** that takes as parameters two rectangles **`R1`** and **`R2`**, and returns the area of their intersection. If the rectangles do not intersect each other, then the area of intersection is 0. If the sides of the rectangles touch each other, it is not considered as an intersection. 12

C.2 Each term of a polynomial in a single variable x can be represented by its coefficient and degree of x. A polynomial is represented as a singly linked list of terms of the polynomial, in decreasing order of degree of x. If a degree of x is missing, no terms are present for it.

i) Define a C data type **`TERM`** to represent a single term of a polynomial in x. 4

ii) Define a C data type **`POLY`** to represent a polynomial as above. 4

iii) Write a C function **`POLY AddPoly(POLY P1, POLY P2)`** that takes as parameters two polynomials **`P1`** and **`P2`**, and returns a new polynomial which is the addition of the two. The polynomials **`P1`** and **`P2`** should remain unchanged. 12