

Verilog Netlist Enhancer

By:

Aya Farag 900160580

Noha 900163073

Problem

The Problem to be solved is that when provided with a netlist, a maximum fanout, and delay , sometimes the netlist violates both the fanout and the delay therefore to solve this problem we provided 3 ways to solve it:

- 1) Sizing up cells that have a large fanout
- 2) Clone high fan-out cells
- 3) Add buffers to high-fanout cells and distribute the load between the,

Algorithm: Sizing up cells that have a large fanout

- We first of all created a dictionary called cell-delay that has each cell and its delay. We calculated the load capacitance of each cell that a certain cell drives, and then we summed the capacitances. We then looked for the load in the capacitance table (index_2) in the liberty file and we chose the delay that corresponds to it and the middle transition time from (index_1). If the load capacitance is not found in the index table, we then either interpolate or extrapolate.
- To size up the cells that have a large fanout I first parsed the netlist and created a dictionary that contains the cell from the netlist and its area corresponding to the liberty file provided by the user. Then we checked if the cell-delay status is violated we find a bigger size of that cell and size up the cell, and replace it in the original verilog netlist, making sure that now it is not violated

Algorithm: Clone High fan-out cells

- We checked the cells that violated the maximum fanout, these cells are all in a list called Fanout with the fanout of each cell and its status (whether or not it's violating).
- The cells that had a violating status were then cloned and the output wire of the cells was renamed. The output wire is then assigned as an input to a number of the fanout cells of the cell we cloned (the number of cells we assigned is equal to the maximum fanout).
- After cloning, we recheck the netlist to see if the cloning process produced any more violations and we fix them by cloning as well.

Algorithm: Add buffers to high-fanout cells

- We looped over the cells and we checked if the output of a cell is an input to any other cell, then we saved that number along with the cell in a list named Fanout.
- We first got the maximum fanout from the user input and then we had to calculate the number of buffers needed now to not violate the maximum fanout per cell, so we created a variable called numbuf where we divide the number of fanouts per cell by the maximum fanout and then we ceil it. After that we check if the status of that cell is violating we then check that numbuf is smaller than maxfanout and we continue adding buffers until numbuf = 0. If numbuf is not less than maxfanout which means that their will be multilevels of buffers connect to each other , for the first layer we make sure the outputs of the cells are inputted into the buffer , and then to add more layers we had to make sure that the output of the buffer in the layer before layer+1 is the input of layer+1 and it does not exceed the maximum fan out per cell.

How to use?

- 1) There will be a user input where you enter the delay and then the max fanout
- 2) Another user input will ask you to pick one of the three ways to enhance the netlist
- 3) The output will be a text file with the name of the option.txt in Run file
- 4) For the Bonus the outputs will be in a file called Bonus in text files

Test Case 1

The First Test case tests large fanout wires, by adding buffers to reduce the delay. The output is as following of before and after:

```
[Fanout(cell='BUFX2_1', fanout=3, status='Violating'),
Fanout(cell='BUFX2_2', fanout=1, status='Not Violating'),
Fanout(cell='BUFX2_3', fanout=1, status='Not Violating'),
Fanout(cell='BUFX2_4', fanout=1, status='Not Violating'),
Fanout(cell='AND2X1_1', fanout=1, status='Not Violating'),
Fanout(cell='NAND2X1_1', fanout=0, status='Not Violating'),
Fanout(cell='NAND2X1_2', fanout=1, status='Not Violating'),
Fanout(cell='AND2X1_2', fanout=3, status='Violating'),
Fanout(cell='INVX1_1', fanout=0, status='Not Violating'),
Fanout(cell='INVX1_2', fanout=0, status='Not Violating'),
Fanout(cell='OAI21X1_3', fanout=0, status='Not Violating')]
```

functions ->"Before"

```
['BUFX2 BUFX2_1 ( .A(s[0]), .Y(c1) );\n',
'BUFX2 BUFX2_2 ( .A(s[1]), .Y(c2) );\n',
'BUFX2 BUFX2_3 ( .A(s[2]), .Y(c3) );\n',
'BUFX2 BUFX2_4 ( .A(s[3]), .Y(c4) );\n',
'AND2X1 AND2X1_1 ( .A(c3), .B(s[3]), .Y(L1) );\n',
'NAND2X1 NAND2X1_1 ( .A(c1), .B(s[3]), .Y(L2) );\n',
'NAND2X1 NAND2X1_2 ( .A(c1), .B(s[2]), .Y(L3) );\n',
'AND2X1 AND2X1_2 ( .A(c1), .B(s[3]), .Y(L4) );\n',
'INVX1 INVX1_1 ( .A(L4), .Y(Y5) );\n',
'INVX1 INVX1_2 ( .A(L4), .Y(L6) );\n',
'OAI21X1 OAI21X1_3 ( .A(c2), .B(r[3]), .C(r[2]), .Y(T) );\n',
'OR2X1 OR2X1_1 ( .A(L3), .B(L1), .Y(n));\n',
'OR2X1 OR2X1_2 ( .A(n), .B(r[0]), .Y(T));\n',
'OR2X1 OR2X1_3 ( .A(L4), .B(c4), .Y(f));\n']
```

functions

```
['BUFX4 BUFX4_1 ( .A(s[0]), .Y(c1) );\n',
'BUFX4 BUFX4_2 ( .A(s[1]), .Y(c2) );\n',
'BUFX4 BUFX4_3 ( .A(s[2]), .Y(c3) );\n',
'BUFX4 BUFX4_4 ( .A(s[3]), .Y(c4) );\n',
'AND2X2 AND2X2_1 ( .A(c3), .B(s[3]), .Y(L1) );\n',
'NAND2X2 NAND2X2_1 ( .A(c1), .B(s[3]), .Y(L2) );\n',
'NAND2X2 NAND2X2_2 ( .A(c1), .B(s[2]), .Y(L3) );\n',
'AND2X2 AND2X2_2 ( .A(c1), .B(s[3]), .Y(L4) );\n',
'INVX8 INVX8_1 ( .A(L4), .Y(Y5) );\n',
'INVX8 INVX8_2 ( .A(L4), .Y(L6) );\n',
'OAI21X1 OAI21X1_3 ( .A(c2), .B(r[3]), .C(r[2]), .Y(T) );\n',
'OR2X1 OR2X1_1 ( .A(L3), .B(L1), .Y(n));\n',
'OR2X1 OR2X1_2 ( .A(n), .B(r[0]), .Y(T));\n',
'OR2X1 OR2X1_3 ( .A(L4), .B(c4), .Y(f));\n']
```

Test Case 2

The Second Test case tests large fanout wires, by adding buffers we reduce the delay. In this test case Fanouts are not violating but the delay is violating therefore we size up the gates.

Fanout

```
[Fanout(cell='AND2X1_1', fanout=2, status='Not Violating'),
Fanout(cell='OAI21X1_1', fanout=0, status='Not Violating'),
Fanout(cell='AND2X1_2', fanout=1, status='Not Violating'),
Fanout(cell='INVX1_1', fanout=1, status='Not Violating'),
Fanout(cell='AND2X1_3', fanout=0, status='Not Violating'),
Fanout(cell='AND2X1_4', fanout=0, status='Not Violating'),
Fanout(cell='AND2X1_5', fanout=1, status='Not Violating'),
Fanout(cell='NOR2X1_1', fanout=0, status='Not Violating'),
Fanout(cell='AND2X1_6', fanout=2, status='Not Violating'),
Fanout(cell='AND2X1_7', fanout=1, status='Not Violating'),
Fanout(cell='AND2X1_8', fanout=1, status='Not Violating'),
Fanout(cell='OR2X1_1', fanout=0, status='Not Violating')]
```

```
[replaceit(origcell='AND2X1_1', origgate='AND2X', num='1', newcell='AND2X2', newarea=128.0, library='AND2X1'),
replaceit(origcell='OAI21X1_1', origgate='OAI21X', num='1', newcell='none', newarea=0, library='OAI21X1'),
replaceit(origcell='AND2X1_2', origgate='AND2X', num='1', newcell='AND2X2', newarea=128.0, library='AND2X1'),
replaceit(origcell='INVX1_1', origgate='INVX', num='1', newcell='none', newarea=0, library='INVX1'),
replaceit(origcell='AND2X1_3', origgate='AND2X', num='1', newcell='AND2X2', newarea=128.0, library='AND2X1'),
replaceit(origcell='AND2X1_4', origgate='AND2X', num='1', newcell='AND2X2', newarea=128.0, library='AND2X1'),
replaceit(origcell='AND2X1_5', origgate='AND2X', num='1', newcell='AND2X2', newarea=128.0, library='AND2X1'),
replaceit(origcell='NOR2X1_1', origgate='NOR2X', num='1', newcell='none', newarea=0, library='NOR2X1'),
replaceit(origcell='AND2X1_6', origgate='AND2X', num='1', newcell='AND2X2', newarea=128.0, library='AND2X1'),
replaceit(origcell='AND2X1_7', origgate='AND2X', num='1', newcell='AND2X2', newarea=128.0, library='AND2X1'),
replaceit(origcell='AND2X1_8', origgate='AND2X', num='1', newcell='AND2X2', newarea=128.0, library='AND2X1'),
replaceit(origcell='OR2X1_1', origgate='OR2X', num='1', newcell='OR2X2', newarea=128.0, library='OR2X1')]
```

cell_delay

```
[cell_delay_things(cell='AND2X1_1', delay=array(0.23412165), status='Violating', library='none'),
cell_delay_things(cell='OAI21X1_1', delay=0.276575, status='Violating', library='none'),
cell_delay_things(cell='AND2X1_2', delay=array(0.23225509), status='Violating', library='none'),
cell_delay_things(cell='INVX1_1', delay=array(0.17577644), status='Not Violating', library='none'),
cell_delay_things(cell='AND2X1_3', delay=0.32774, status='Violating', library='none'),
cell_delay_things(cell='AND2X1_4', delay=0.32774, status='Violating', library='none'),
cell_delay_things(cell='AND2X1_5', delay=array(0.23301385), status='Violating', library='none'),
cell_delay_things(cell='NOR2X1_1', delay=0.304627, status='Violating', library='none'),
cell_delay_things(cell='AND2X1_6', delay=array(0.23410375), status='Violating', library='none'),
cell_delay_things(cell='AND2X1_7', delay=array(0.23265586), status='Violating', library='none'),
cell_delay_things(cell='AND2X1_8', delay=array(0.23306148), status='Violating', library='none'),
cell_delay_things(cell='OR2X1_1', delay=0.300365, status='Violating', library='none')]
```

Test Case 3

Test case 3 is a Ripple Carry Adder, the cells that exceed the specified Timing delay are shown on the side. To reduce the timing delay We sized up.

```
[Fanout(cell='BUFX2_1', fanout=0, status='Not Violating'),
Fanout(cell='BUFX2_2', fanout=0, status='Not Violating'),
Fanout(cell='BUFX2_3', fanout=0, status='Not Violating'),
Fanout(cell='BUFX2_4', fanout=0, status='Not Violating'),
Fanout(cell='BUFX2_5', fanout=0, status='Not Violating'),
Fanout(cell='INVX1_1', fanout=2, status='Not Violating'),
Fanout(cell='OR2X2_1', fanout=1, status='Not Violating'),
Fanout(cell='NAND2X1_1', fanout=2, status='Not Violating'),
Fanout(cell='NAND3X1_1', fanout=1, status='Not Violating'),
Fanout(cell='NOR2X1_1', fanout=2, status='Not Violating'),
Fanout(cell='AND2X2_1', fanout=1, status='Not Violating'),
Fanout(cell='OAI21X1_1', fanout=1, status='Not Violating'),
Fanout(cell='NAND2X1_2', fanout=1, status='Not Violating'),
Fanout(cell='OAI21X1_2', fanout=4, status='Violating'),
Fanout(cell='INVX1_2', fanout=2, status='Not Violating'),
Fanout(cell='OR2X2_2', fanout=1, status='Not Violating'),
Fanout(cell='NAND2X1_3', fanout=2, status='Not Violating'),
Fanout(cell='NAND3X1_2', fanout=1, status='Not Violating'),
Fanout(cell='NOR2X1_2', fanout=2, status='Not Violating'),
Fanout(cell='AND2X2_2', fanout=1, status='Not Violating'),
Fanout(cell='OAI21X1_3', fanout=1, status='Not Violating'),
Fanout(cell='NAND2X1_4', fanout=1, status='Not Violating'),
Fanout(cell='OAI21X1_4', fanout=4, status='Violating'),
Fanout(cell='INVX1_3', fanout=2, status='Not Violating'),
Fanout(cell='OR2X2_3', fanout=1, status='Not Violating'),
Fanout(cell='NAND2X1_5', fanout=2, status='Not Violating'),
Fanout(cell='NAND3X1_3', fanout=1, status='Not Violating'),
Fanout(cell='NOR2X1_3', fanout=2, status='Not Violating'),
Fanout(cell='AND2X2_3', fanout=1, status='Not Violating'),
Fanout(cell='OAI21X1_5', fanout=1, status='Not Violating'),
Fanout(cell='NAND2X1_6', fanout=1, status='Not Violating'),
Fanout(cell='OAI21X1_6', fanout=4, status='Violating'),
Fanout(cell='INVX1_4', fanout=2, status='Not Violating'),
Fanout(cell='OR2X2_4', fanout=1, status='Not Violating'),
Fanout(cell='NAND2X1_7', fanout=2, status='Not Violating'),
Fanout(cell='NAND3X1_4', fanout=1, status='Not Violating'),
Fanout(cell='NOR2X1_4', fanout=2, status='Not Violating'),
Fanout(cell='AND2X2_4', fanout=1, status='Not Violating'),
Fanout(cell='OAI21X1_7', fanout=1, status='Not Violating'),
Fanout(cell='NAND2X1_8', fanout=1, status='Not Violating'),
Fanout(cell='OAI21X1_8', fanout=1, status='Not Violating')]
```

Continuation of Test Case 3:

Test case 3 also has fanout violations so we added buffers to minimize the fanout.

```
[Bufferadded(BufferType='BUFX4 ', Buffername='BUFX4_0_added ', inputt='c1', output='0'),  
 Bufferadded(BufferType='BUFX4 ', Buffername='BUFX4_1_added ', inputt='c1', output='1'),  
 Bufferadded(BufferType='BUFX4 ', Buffername='BUFX4_2_added ', inputt='c2', output='2'),  
 Bufferadded(BufferType='BUFX4 ', Buffername='BUFX4_3_added ', inputt='c2', output='3'),  
 Bufferadded(BufferType='BUFX4 ', Buffername='BUFX4_4_added ', inputt='c3', output='4'),  
 Bufferadded(BufferType='BUFX4 ', Buffername='BUFX4_5_added ', inputt='c3', output='5')]
```

Test Case 4

Test Case 4 is uses the Ripple Carry Adder module with a slight modification to drives out of it many fanouts to test sizing up and adding buffers.

Size up

```
In [325]: cell delay
```

```
Out[325]: [cell_delay_things(cell='BUF2X_1', delay=0.359906, status='Violating', library='BUF2X'),
cell_delay_things(cell='BUF2X_2', delay=0.359906, status='Violating', library='BUF2X'),
cell_delay_things(cell='BUF2X_3', delay=0.359906, status='Violating', library='BUF2X'),
cell_delay_things(cell='BUF2X_4', delay=0.359906, status='Violating', library='BUF2X'),
cell_delay_things(cell='BUF2X_5', delay=0.359906, status='Violating', library='BUF2X'),
cell_delay_things(cell='INVX1_1', delay=array(0.18296699), status='Not Violating', library='INVX1'),
cell_delay_things(cell='OR2X2_1', delay=array(0.27092712), status='Violating', library='OR2X2'),
cell_delay_things(cell='NAND2X1_1', delay=array(0.20469434), status='Not Violating', library='NAND2X1'),
cell_delay_things(cell='NAND3X1_1', delay=array(0.24266393), status='Violating', library='NAND3X1'),
cell_delay_things(cell='NOR2X1_1', delay=array(0.20644544), status='Not Violating', library='NOR2X1'),
cell_delay_things(cell='AND2X2_1', delay=array(0.26809826), status='Violating', library='AND2X2'),
cell_delay_things(cell='OA121X1_1', delay=array(0.21210386), status='Not Violating', library='OA121X1'),
cell_delay_things(cell='NAND2X1_2', delay=array(0.19737745), status='Not Violating', library='NAND2X1'),
cell_delay_things(cell='OA121X1_2', delay=array(0.22808014), status='Not Violating', library='OA121X1'),
cell_delay_things(cell='INVX1_2', delay=array(0.17680094), status='Not Violating', library='INVX1'),
cell_delay_things(cell='OR2X2_2', delay=array(0.27092712), status='Violating', library='OR2X2'),
cell_delay_things(cell='NAND2X1_3', delay=array(0.20469434), status='Not Violating', library='NAND2X1'),
cell_delay_things(cell='NAND3X1_2', delay=array(0.24266393), status='Violating', library='NAND3X1'),
cell_delay_things(cell='NAND2X1_2', delay=array(0.20644544), status='Not Violating', library='NOR2X1'),
cell_delay_things(cell='NAND2X1_3', delay=array(0.26809826), status='Violating', library='AND2X2'),
cell_delay_things(cell='NAND2X1_4', delay=array(0.276757), status='Violating', library='OA121X1'),
cell_delay_things(cell='NAND2X1_5', delay=array(0.19737745), status='Not Violating', library='NAND2X1'),
cell_delay_things(cell='OA121X1_4', delay=array(0.22185229), status='Not Violating', library='OA121X1'),
cell_delay_things(cell='INVX1_3', delay=array(0.17564073), status='Not Violating', library='INVX1'),
cell_delay_things(cell='OR2X2_3', delay=array(0.27092712), status='Violating', library='OR2X2'),
cell_delay_things(cell='NAND2X1_5', delay=array(0.20469434), status='Not Violating', library='NAND2X1'),
cell_delay_things(cell='NAND3X1_3', delay=array(0.24266393), status='Violating', library='NAND3X1'),
cell_delay_things(cell='NOR2X1_3', delay=array(0.20644544), status='Not Violating', library='NOR2X1'),
cell_delay_things(cell='AND2X2_3', delay=array(0.26809826), status='Violating', library='AND2X2'),
cell_delay_things(cell='OA121X1_5', delay=array(0.21210386), status='Not Violating', library='OA121X1'),
cell_delay_things(cell='NAND2X1_6', delay=array(0.19737745), status='Not Violating', library='NAND2X1'),
cell_delay_things(cell='OA121X1_6', delay=array(0.23700889), status='Violating', library='OA121X1'),
cell_delay_things(cell='INVX1_4', delay=0.298417, status='Violating', library='INVX1'),
cell_delay_things(cell='OR2X2_4', delay=array(0.27092712), status='Violating', library='OR2X2'),
cell_delay_things(cell='NAND2X1_7', delay=array(0.20469434), status='Not Violating', library='NAND2X1'),
cell_delay_things(cell='NAND3X1_4', delay=array(0.24266393), status='Violating', library='NAND3X1'),
cell_delay_things(cell='NOR2X1_4', delay=array(0.20071722), status='Not Violating', library='NOR2X1'),
cell_delay_things(cell='AND2X2_4', delay=array(0.26809826), status='Violating', library='AND2X2'),
cell_delay_things(cell='OA121X1_7', delay=0.276757, status='Violating', library='OA121X1'),
cell_delay_things(cell='NAND2X1_8', delay=array(0.19737745), status='Not Violating', library='NAND2X1'),
cell_delay_things(cell='OA121X1_8', delay=array(0.21144237), status='Not Violating', library='OA121X1')]
```

Test Case 5

- We tested Cloning one the netlist on the left, and produced the netlist on the right. (all the files are attached with the submission). The maximum fanout was two, and the violating cell was INVX1_1, cloning that cell caused the violation of BUFX2_4, so it was cloned as well.

```
module rca4 (a, b, ci, s, co);

input ci;
output co;
input [3:0] a;
input [3:0] b;
output [3:0] s;

wire vdd = 1'b1;
wire gnd = 1'b0;

BUFX2 BUFX2_1 ( .A(fa0_s), .Y(s[0]) );
BUFX2 BUFX2_2 ( .A(fa1_s), .Y(s[1]) );
BUFX2 BUFX2_3 ( .A(fa2_s), .Y(s[2]) );
BUFX2 BUFX2_4 ( .A(fa3_s), .Y(0_1) );
INVX1 INVX1_1 ( .A(0_1), .Y(_4_) );
OR2X2 OR2X2_1 ( .A(_4_), .B(0_1), .Y(_5_) );
NAND2X1 NAND2X1_1 ( .A(_4_), .B(a[0]), .Y(_6_) );
NAND3X1 NAND3X1_1 ( .A(_4_), .B(_6_), .C(_5_), .Y(_7_) );
endmodule
```

```
BUFX2 BUFX2_1 ( .A(fa0_s), .Y(s[0]) );
BUFX2 BUFX2_2 ( .A(fa1_s), .Y(s[1]) );
BUFX2 BUFX2_3 ( .A(fa2_s), .Y(s[2]) );
BUFX2 BUFX2_4 ( .A(fa3_s), .Y(0_1) );
INVX1 INVX1_1 ( .A(0_11), .Y(_4_) );
OR2X2 OR2X2_1 ( .A(_4_), .B(0_11), .Y(_5_) );
NAND2X1 NAND2X1_1 ( .A(_4_), .B(a[0]), .Y(_6_) );
NAND3X1 NAND3X1_1 ( .A(_4_), .B(_6_), .C(_5_), .Y(_7_) );
INVX1 INVX1_1_cloned4 (.A(0_1),.Y(_4__));
BUFX2 BUFX2_4_cloned3 (.A(fa3_s),.Y(0_11))
```

Test Case 6

- Also Cloning, we tested the rca netlist that was provided on slack (original Netlist on the left and modified netlist on the right), the files are provided with the submission:

```
BUFX2 BUFX2_X_1 ( .A(fa0_s) , .Y(s[0]) );
BUFX2 BUFX2_X_2 ( .A(fa1_s) , .Y(s[1]) );
BUFX2 BUFX2_X_3 ( .A(fa2_s) , .Y(s[2]) );
BUFX2 BUFX2_X_4 ( .A(fa3_s) , .Y(s[3]) );
BUFX2 BUFX2_X_5 ( .A(_0) , .Y(c0) );
INVX1 INVX1_1 ( .A(b[0]) , .Y(_4_) );
OR2X2 OR2X2_1 ( .A(c1) , .B(a[8]) , .Y(_5_) );
NAND2X1 NAND2X1_1 ( .A(c1) , .B(s[0]) , .Y(_6_) );
NAND3X1 NAND3X1_1 ( .A(_4_) , .B(_6_) , .C(_5_) ) , .Y(_7_) );
NOR2X1 NOR2X1_1 ( .A(c1) , .B(s[0]) , .Y(_1_) );
AND2X2 AND2X2_1 ( .A(c1) , .B(a[0]) , .Y(_2_) );
OAI2X1 OAI2X1_1 ( .A(_1_) , .B(_2_) , .C(b[0]) ) , .Y(_3_) );
NAND2X1 NAND2X1_2 ( .A(_3_) , .B(_7_) , .Y(fa0_s) );
OAI2X1 OAI2X1_2 ( .A(_4_) , .B(_1_) , .C(_6_) , .Y(c1) );
INVX1 INVX1_2 ( .A(b[1]) , .Y(_11_) );
OR2X2 OR2X2_2 ( .A(c1) , .B(a[1]) , .Y(_12_) );
NAND2X1 NAND2X1_3 ( .A(c1) , .B(s[1]) , .Y(_13_) );
NAND3X1 NAND3X1_2 ( .A(_11_) , .B(c12) , .C(_12_) ) , .Y(_14_) );
NOR2X1 NOR2X1_2 ( .A(c1) , .B(s[1]) , .Y(_9_) );
AND2X2 AND2X2_2 ( .A(c1) , .B(a[1]) , .Y(_9_) );
OAI2X1 OAI2X1_3 ( .A(_8_) , .B(_9_) , .C(b[1]) ) , .Y(_10_) );
NAND2X1 NAND2X1_4 ( .A(_10_) , .B(fa1_s) );
OAI2X1 OAI2X1_4 ( .A(_11_) , .B(_9_) , .C(_13_) ) , .Y(c2) );
INVX1 INVX1_3 ( .A(b[2]) , .Y(_18_) );
OR2X2 OR2X2_3 ( .A(c2) , .B(a[2]) , .Y(_19_) );
NAND2X1 NAND2X1_5 ( .A(c2) , .B(s[2]) , .Y(_20_) );
NAND3X1 NAND3X1_3 ( .A(_18_) , .B(c20) , .C(_19_) ) , .Y(_21_) );
NOR2X1 NOR2X1_3 ( .A(c2) , .B(s[2]) , .Y(_15_) );
AND2X2 AND2X2_3 ( .A(c2) , .B(a[2]) , .Y(_16_) );
OAI2X1 OAI2X1_5 ( .A(c2) , .B(a[2]) , .C(b[2]) ) , .Y(_17_) );
NAND2X1 NAND2X1_6 ( .A(_17_) , .B(_21_) , .Y(fa2_s) );
OAI2X1 OAI2X1_6 ( .A(_18_) , .B(_15_) , .C(_20_) ) , .Y(c3) );
INVX1 INVX1_4 ( .A(b[3]) , .Y(_25_) );
OR2X2 OR2X2_4 ( .A(c3) , .B(a[3]) , .Y(_26_) );
NAND2X1 NAND2X1_7 ( .A(c3) , .B(s[3]) , .Y(_27_) );
NAND3X1 NAND3X1_4 ( .A(_25_) , .B(c26) , .C(_26_) ) , .Y(_28_) );
NOR2X1 NOR2X1_4 ( .A(c3) , .B(s[3]) , .Y(_22_) );
AND2X2 AND2X2_4 ( .A(c3) , .B(a[3]) , .Y(_23_) );
OAI2X1 OAI2X1_7 ( .A(_22_) , .B(_23_) , .C(b[3]) ) , .Y(_24_) );
NAND2X1 NAND2X1_8 ( .A(_24_) , .B(_28_) , .Y(fa3_s) );
OAI2X1 OAI2X1_8 ( .A(_25_) , .B(_22_) , .C(_27_) ) , .Y(_0_) );

```

```
INVX1 INVX1_2 ( .A(b[1]) , .Y(_11_) );
OR2X2 OR2X2_2 ( .A(c11) , .B(a[1]) , .Y(_12_) );
NAND2X1 NAND2X1_3 ( .A(c11) , .B(a[1]) , .C(_13_) );
NAND3X1 NAND3X1_2 ( .A(_11_) , .B(_13_) , .C(_12_) ) , .Y(_14_) );
NOR2X1 NOR2X1_2 ( .A(c11) , .B(a[1]) , .Y(_8_) );
AND2X2 AND2X2_2 ( .A(c1) , .B(a[1]) , .Y(_9_) );
OAI2X1 OAI2X1_3 ( .A(_8_) , .B(_9_) , .C(b[1]) ) , .Y(_10_) );
NAND2X1 NAND2X1_4 ( .A(_10_) , .B(_14_) ) , .Y(fa1_s) );
OAI2X1 OAI2X1_4 ( .A(_11_) , .B(_8_) , .C(_13_) ) , .Y(c2) );
INVX1 INVX1_3 ( .A(b[2]) , .Y(_18_) );
OR2X2 OR2X2_3 ( .A(c22) , .B(a[2]) , .Y(_19_) );
NAND2X1 NAND2X1_5 ( .A(c22) , .B(s[2]) , .Y(_20_) );
NAND3X1 NAND3X1_3 ( .A(_18_) , .B(c20) , .C(_19_) ) , .Y(_21_) );
NOR2X1 NOR2X1_3 ( .A(c22) , .B(a[2]) , .Y(_15_) );
AND2X2 AND2X2_3 ( .A(c2) , .B(a[2]) , .Y(_16_) );
OAI2X1 OAI2X1_5 ( .A(_15_) , .B(_16_) , .C(b[2]) ) , .Y(_17_) );
NAND2X1 NAND2X1_6 ( .A(_17_) , .B(_21_) ) , .Y(fa2_s) );
OAI2X1 OAI2X1_6 ( .A(_18_) , .B(_15_) , .C(_20_) ) , .Y(c3) );
INVX1 INVX1_4 ( .A(b[3]) , .Y(_25_) );
OR2X2 OR2X2_4 ( .A(c33) , .B(a[3]) , .Y(_26_) );
NAND2X1 NAND2X1_7 ( .A(c33) , .B(a[3]) , .Y(_27_) );
NAND3X1 NAND3X1_4 ( .A(_25_) , .B(c26) , .C(_26_) ) , .Y(_28_) );
NOR2X1 NOR2X1_4 ( .A(c33) , .B(a[3]) , .Y(_22_) );
AND2X2 AND2X2_4 ( .A(c3) , .B(a[3]) , .Y(_23_) );
OAI2X1 OAI2X1_7 ( .A(_22_) , .B(_23_) , .C(b[3]) ) , .Y(_24_) );
NAND2X1 NAND2X1_8 ( .A(_24_) , .B(_28_) ) , .Y(fa3_s) );
OAI2X1 OAI2X1_8 ( .A(_25_) , .B(_22_) , .C(_27_) ) , .Y(_0_) );
OAI2X1 OAI2X1_2_cloned13 (.A(_4_),.B(_1_),.C(_6_),.Y(c11))
OAI2X1 OAI2X1_4_cloned22 (.A(_11_),.B(_8_),.C(_13_),.Y(c22))
OAI2X1 OAI2X1_6_cloned31 (.A(_18_),.B(_15_),.C(_20_),.Y(c33))
```

Test Case 7

- Also Cloning,

```
BUFX2 BUFX2_1 ( .A(fa0_s), .Y(s[0]) );
BUFX2 BUFX2_2 ( .A(fa1_s), .Y(s[1]) );
BUFX2 BUFX2_3 ( .A(fa2_s), .Y(s[2]) );
BUFX2 BUFX2_4 ( .A(_4_), .Y(s[3]) );
BUFX2 BUFX2_5 ( .A(_0_), .Y(co) );
INVX1 INVX1_1 ( .A(e), .Y(_4_) );
OR2X2 OR2X2_1 ( .A(ci), .B(a[0]), .Y(_5_) );
NAND2X1 NAND2X1_1 ( .A(ci), .B(a[0]), .Y(_6_) );
NAND3X1 NAND3X1_1 ( .A(_4_), .B(_6_), .C(_5_), .Y(_7_) );
NOR2X1 NOR2X1_1 ( .A(ci), .B(a[0]), .Y(_1_) );
AND2X2 AND2X2_1 ( .A(ci), .B(a[0]), .Y(_2_) );
OAI21X1 OAI21X1_1 ( .A(_1_), .B(_2_), .C(b[0]), .Y(_3_) );
NAND2X1 NAND2X1_2 ( .A(_3_), .B(_7_), .Y(fa0_s) );
OAI21X1 OAI21X1_2 ( .A(_4_), .B(_1_), .C(_6_), .Y(c1) );
INVX1 INVX1_2 ( .A(_4_), .Y(k) );
```

```
BUFX2 BUFX2_1 ( .A(fa0_s), .Y(s[0]) );
BUFX2 BUFX2_2 ( .A(fa1_s), .Y(s[1]) );
BUFX2 BUFX2_3 ( .A(fa2_s), .Y(s[2]) );
BUFX2 BUFX2_4 ( .A(_4_), .Y(s[3]) );
BUFX2 BUFX2_5 ( .A(_0_), .Y(co) );
INVX1 INVX1_1 ( .A(e), .Y(_4_) );
OR2X2 OR2X2_1 ( .A(ci), .B(a[0]), .Y(_5_) );
NAND2X1 NAND2X1_1 ( .A(ci), .B(a[0]), .Y(_6_) );
NAND3X1 NAND3X1_1 ( .A(_4_), .B(_6_), .C(_5_), .Y(_7_) );
NOR2X1 NOR2X1_1 ( .A(ci), .B(a[0]), .Y(_1_) );
AND2X2 AND2X2_1 ( .A(ci), .B(a[0]), .Y(_2_) );
OAI21X1 OAI21X1_1 ( .A(_1_), .B(_2_), .C(b[0]), .Y(_3_) );
NAND2X1 NAND2X1_2 ( .A(_3_), .B(_7_), .Y(fa0_s) );
OAI21X1 OAI21X1_2 ( .A(_4_), .B(_1_), .C(_6_), .Y(c1) );
INVX1 INVX1_2 ( .A(_4_), .Y(k) );
INVX1 INVX1_1_cloned5 (.A(e),.Y(_4__))
```

Test Case 8

- Sizing Up, (original Netlist on the left and modified netlist on the right).

```
module rca4 (a, b, ci, s, co);

input ci;
output co;
input [3:0] a;
input [3:0] b;
output [3:0] s;

wire vdd = 1'b1;
wire gnd = 1'b0;

BUFX2 BUFX2_1 ( .A(fa0_s), .Y(s[0]) );
BUFX2 BUFX2_2 ( .A(fa1_s), .Y(s[1]) );
BUFX2 BUFX2_3 ( .A(fa2_s), .Y(s[2]) );
BUFX2 BUFX2_4 ( .A(fa3_s), .Y(0_1) );
INVX1 INVX1_1 ( .A(0_1), .Y(_4_) );
OR2X2 OR2X2_1 ( .A(_4_), .B(0_1), .Y(_5_) );
NAND2X1 NAND2X1_1 ( .A(_4_), .B(a[0]), .Y(_6_) );
NAND3X1 NAND3X1_1 ( .A(_4_), .B(_6_), .C(_5_), .Y(_7_) );
endmodule
```

```
BUFX4 BUFX4_1 ( .A(fa0_s), .Y(s[0]) );
BUFX4 BUFX4_2 ( .A(fa1_s), .Y(s[1]) );
BUFX4 BUFX4_3 ( .A(fa2_s), .Y(s[2]) );
BUFX4 BUFX4_4 ( .A(fa3_s), .Y(0_1) );
INVX1 INVX1_1 ( .A(0_1), .Y(_4_) );
OR2X2 OR2X2_1 ( .A(_4_), .B(0_1), .Y(_5_) );
NAND2X1 NAND2X1_1 ( .A(_4_), .B(a[0]), .Y(_6_) );
NAND3X1 NAND3X1_1 ( .A(_4_), .B(_6_), .C(_5_), .Y(_7_) );
```

Bonus

- Each one of the three methods is run by choosing it as a user input. When running any method the delays and number of cells of each type before enhancement are printed in a file in the bonus folder.
- After the user chooses a method and it runs, the delays and number of cells of each type after enhancement are printed in files in the Bonus folder.
- GitHub Repository : <https://github.com/ayashaker98/MiniProject.git>

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