

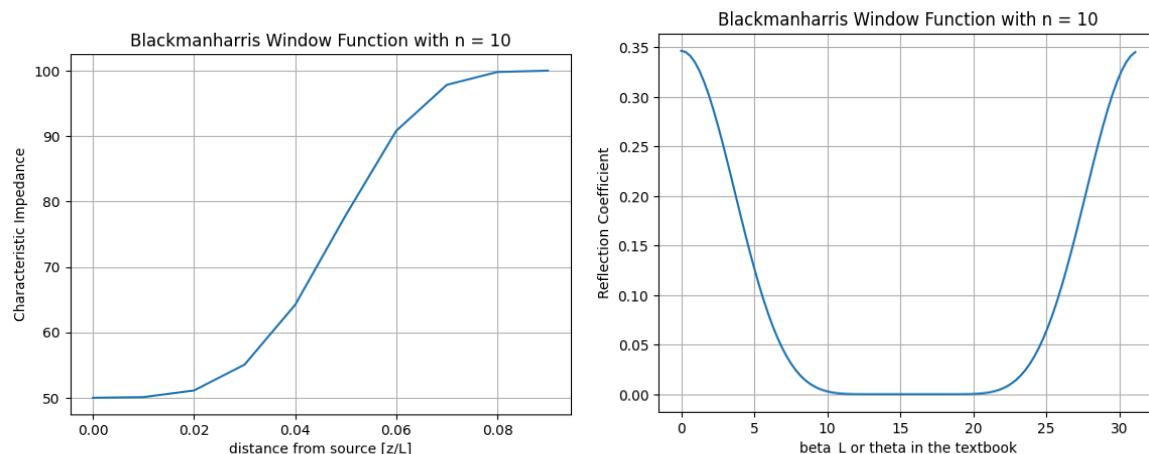
Microwave Project Methodology

Step 1: Tapered line selection

Choosing Blackman-Harris because it offers excellent side lobe suppression, which significantly reduces spectral leakage.

Step 2: Simulation

In this step we use Python, on Google Colab, to visualize the taper line behavior through characteristic Impedance versus distance from source [z/L] from 50Ω to 100Ω plot and the Reflection Coefficient in decibel versus βL plot. We also use Python to compute the impedance of each section in this step, we number of sections equal 10. The plots are shown below:



The computed impedance for each section is saved as table, as shown below:

	0
0	50
1	50.1062102
2	51.11348314
3	55.0701908
4	64.19909417
5	77.88271882
6	90.79322092
7	97.82154714
8	99.78802987
9	100

Ratchaphon Sudjaiboon 6610550867
Sakolhat Meesomboon 6610553726

Then we import it to Google Sheet and modify it to be ready for Sonnet file format:

TLIN	1	2	Z=	50	E=	36.00	F=	4.00	TLIN 1 2 Z=50.0 E=36.0 F=4.0
TLIN	2	3	Z=	50.1062102	E=	36.00	F=	4.00	TLIN 2 3 Z=50.1 E=36.0 F=4.0
TLIN	3	4	Z=	51.11348314	E=	36.00	F=	4.00	TLIN 3 4 Z=51.1 E=36.0 F=4.0
TLIN	4	5	Z=	55.0701908	E=	36.00	F=	4.00	TLIN 4 5 Z=55.1 E=36.0 F=4.0
TLIN	5	6	Z=	64.19909417	E=	36.00	F=	4.00	TLIN 5 6 Z=64.2 E=36.0 F=4.0
TLIN	6	7	Z=	77.88271882	E=	36.00	F=	4.00	TLIN 6 7 Z=77.9 E=36.0 F=4.0
TLIN	7	8	Z=	90.79322092	E=	36.00	F=	4.00	TLIN 7 8 Z=90.8 E=36.0 F=4.0
TLIN	8	9	Z=	97.82154714	E=	36.00	F=	4.00	TLIN 8 9 Z=97.8 E=36.0 F=4.0
TLIN	9	10	Z=	99.78802987	E=	36.00	F=	4.00	TLIN 9 10 Z=99.8 E=36.0 F=4.0

Step 3: netlist simulation inside sonnet

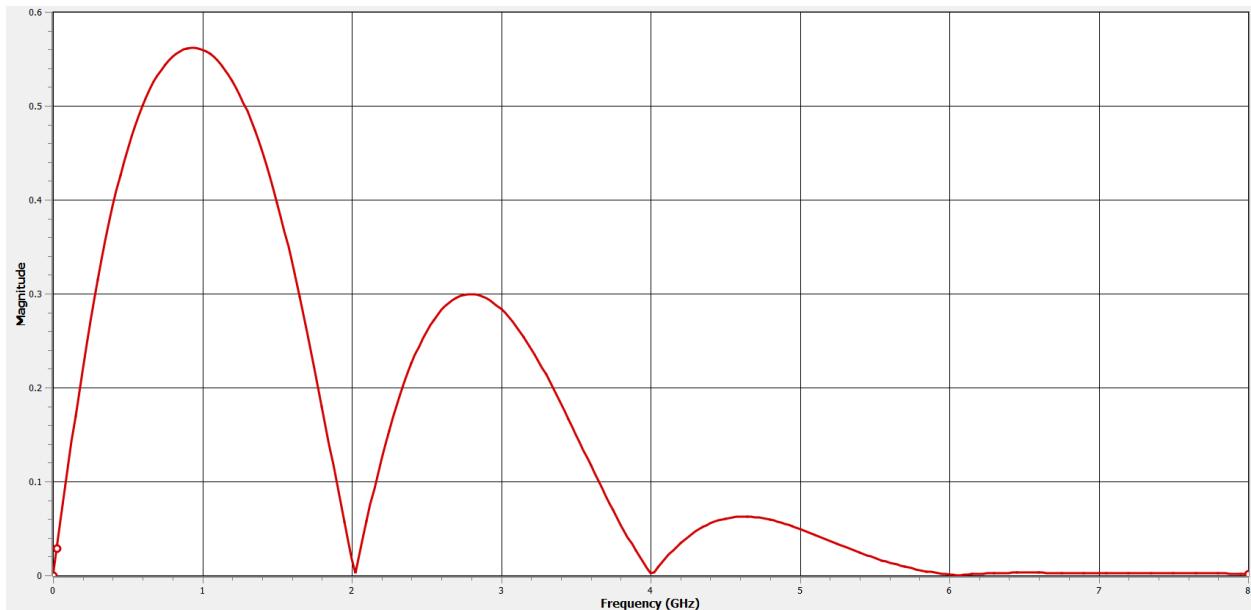
Since both sides of the tapered line are symmetry we simply extend the table as shown below before using the rightmost column for modifying the Sonnet netlist file.

TLIN	1	2	Z=	50	E=	36.00	F=	4.00	TLIN 1 2 Z=50.0 E=36.0 F=4.0
TLIN	2	3	Z=	50.1062102	E=	36.00	F=	4.00	TLIN 2 3 Z=50.1 E=36.0 F=4.0
TLIN	3	4	Z=	51.11348314	E=	36.00	F=	4.00	TLIN 3 4 Z=51.1 E=36.0 F=4.0
TLIN	4	5	Z=	55.0701908	E=	36.00	F=	4.00	TLIN 4 5 Z=55.1 E=36.0 F=4.0
TLIN	5	6	Z=	64.19909417	E=	36.00	F=	4.00	TLIN 5 6 Z=64.2 E=36.0 F=4.0
TLIN	6	7	Z=	77.88271882	E=	36.00	F=	4.00	TLIN 6 7 Z=77.9 E=36.0 F=4.0
TLIN	7	8	Z=	90.79322092	E=	36.00	F=	4.00	TLIN 7 8 Z=90.8 E=36.0 F=4.0
TLIN	8	9	Z=	97.82154714	E=	36.00	F=	4.00	TLIN 8 9 Z=97.8 E=36.0 F=4.0
TLIN	9	10	Z=	99.78802987	E=	36.00	F=	4.00	TLIN 9 10 Z=99.8 E=36.0 F=4.0
TLIN	10	11	Z=	100	E=	36.00	F=	4.00	TLIN 10 11 Z=100.0 E=36.0 F=4.0
TLIN	11	12	Z=	100	E=	36.00	F=	4.00	TLIN 11 12 Z=100.0 E=36.0 F=4.0
TLIN	12	13	Z=	99.78802987	E=	36.00	F=	4.00	TLIN 12 13 Z=99.8 E=36.0 F=4.0
TLIN	13	14	Z=	97.82154714	E=	36.00	F=	4.00	TLIN 13 14 Z=97.8 E=36.0 F=4.0
TLIN	14	15	Z=	90.79322092	E=	36.00	F=	4.00	TLIN 14 15 Z=90.8 E=36.0 F=4.0
TLIN	15	16	Z=	77.88271882	E=	36.00	F=	4.00	TLIN 15 16 Z=77.9 E=36.0 F=4.0
TLIN	16	17	Z=	64.19909417	E=	36.00	F=	4.00	TLIN 16 17 Z=64.2 E=36.0 F=4.0
TLIN	17	18	Z=	55.0701908	E=	36.00	F=	4.00	TLIN 17 18 Z=55.1 E=36.0 F=4.0
TLIN	18	19	Z=	51.11348314	E=	36.00	F=	4.00	TLIN 18 19 Z=51.1 E=36.0 F=4.0
TLIN	19	20	Z=	50.1062102	E=	36.00	F=	4.00	TLIN 19 20 Z=50.1 E=36.0 F=4.0
TLIN	20	21	Z=	50	E=	36.00	F=	4.00	TLIN 20 21 Z=50.0 E=36.0 F=4.0

Now, we have the netlist file. The units are left as default, our netlist has 2 ports, and both ports have 50 Ohms resistance. Then we sweep from 0 to 8 GHz frequency. Here is the netlist:

Element	Nodes	Description
Net	1 21	Main Network
TLIN	1 2	Z=50.0 E=36.0 F=4.0
TLIN	2 3	Z=50.1 E=36.0 F=4.0
TLIN	3 4	Z=51.1 E=36.0 F=4.0
TLIN	4 5	Z=55.1 E=36.0 F=4.0
TLIN	5 6	Z=64.2 E=36.0 F=4.0
TLIN	6 7	Z=77.9 E=36.0 F=4.0
TLIN	7 8	Z=90.8 E=36.0 F=4.0
TLIN	8 9	Z=97.8 E=36.0 F=4.0
TLIN	9 10	Z=99.8 E=36.0 F=4.0
TLIN	10 11	Z=100.0 E=36.0 F=4.0
TLIN	11 12	Z=100.0 E=36.0 F=4.0
TLIN	12 13	Z=99.8 E=36.0 F=4.0
TLIN	13 14	Z=97.8 E=36.0 F=4.0
TLIN	14 15	Z=90.8 E=36.0 F=4.0
TLIN	15 16	Z=77.9 E=36.0 F=4.0
TLIN	16 17	Z=64.2 E=36.0 F=4.0
TLIN	17 18	Z=55.1 E=36.0 F=4.0
TLIN	18 19	Z=51.1 E=36.0 F=4.0
TLIN	19 20	Z=50.1 E=36.0 F=4.0
TLIN	20 21	Z=50.0 E=36.0 F=4.0

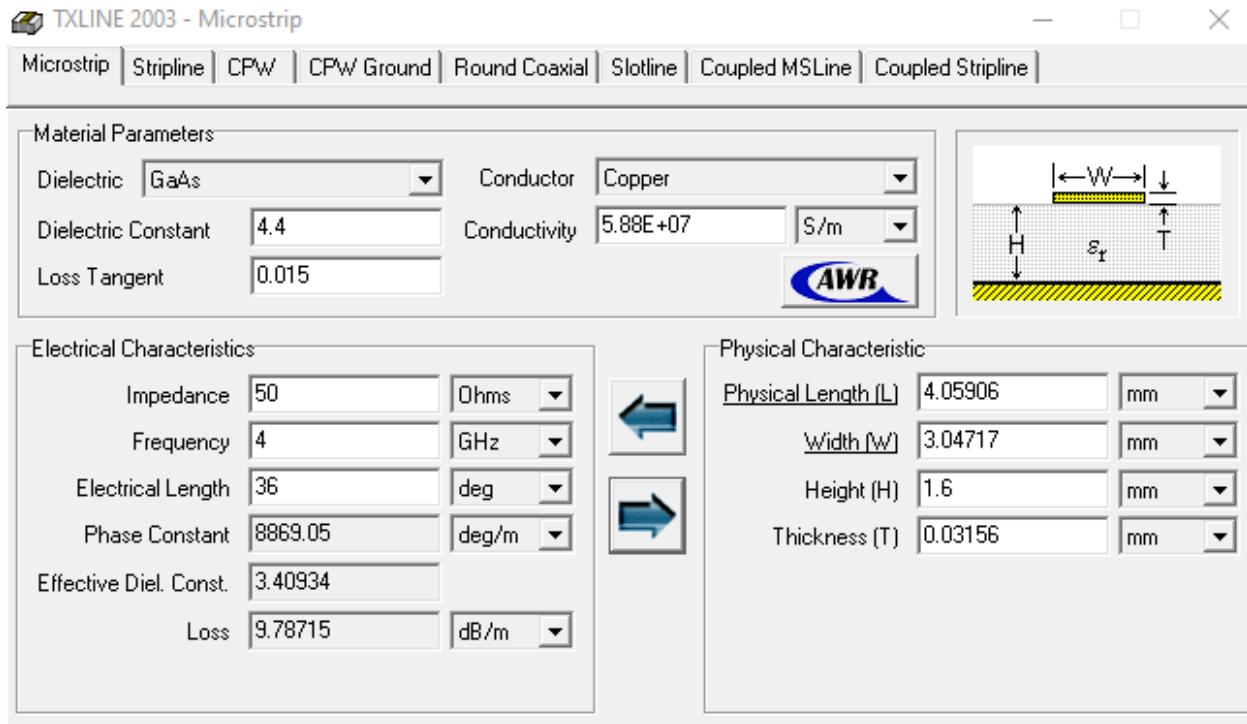
Sweeps from 0 to 8 GHz:



Step 4: geometry simulation inside sonnet

After confirming the expected result from netlist, we now use TXLINE 2003 to convert impedance, frequency and electrical length to Length and Width of the copper piece on the PCB.

Example of using TXLINE 2003 to convert the first tapered line section in netlist to length and width:

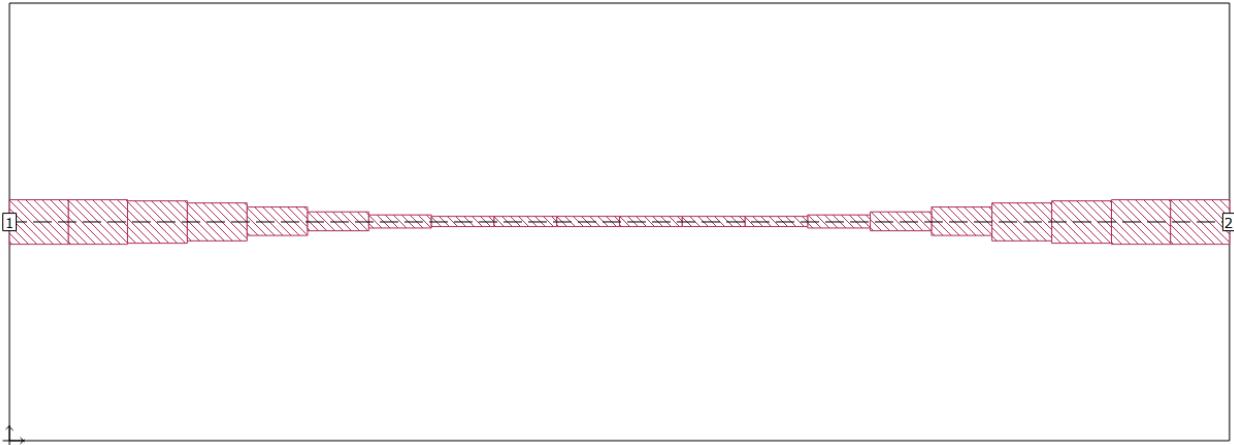


After converting every tapered line section in netlist to length and width, we need to reduce floating points of the dimensions to match Sonnet's resolution.

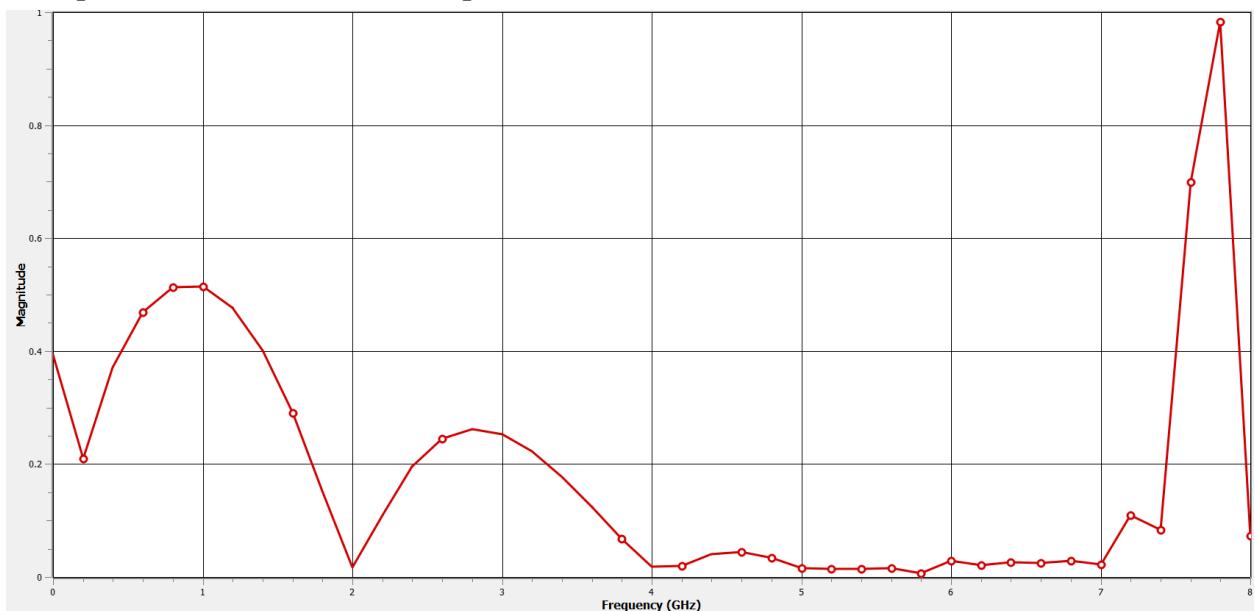
Then we get this as dimensions for each copper piece which represent each section of the tapered line:

section	Length, X	width Y,	unit mm
1	4.06	3.05	
2	4.06	3.04	
3	4.07	2.94	
4	4.09	2.58	
5	4.15	1.93	
6	4.22	1.28	
7	4.27	0.88	
8	4.30	0.72	
9	4.31	0.68	
10	4.31	0.67	
11	4.31	0.67	
12	4.31	0.68	
13	4.30	0.72	
14	4.27	0.88	
15	4.22	1.28	
16	4.15	1.93	
17	4.09	2.58	
18	4.07	2.94	
19	4.06	3.04	
20	4.06	3.05	

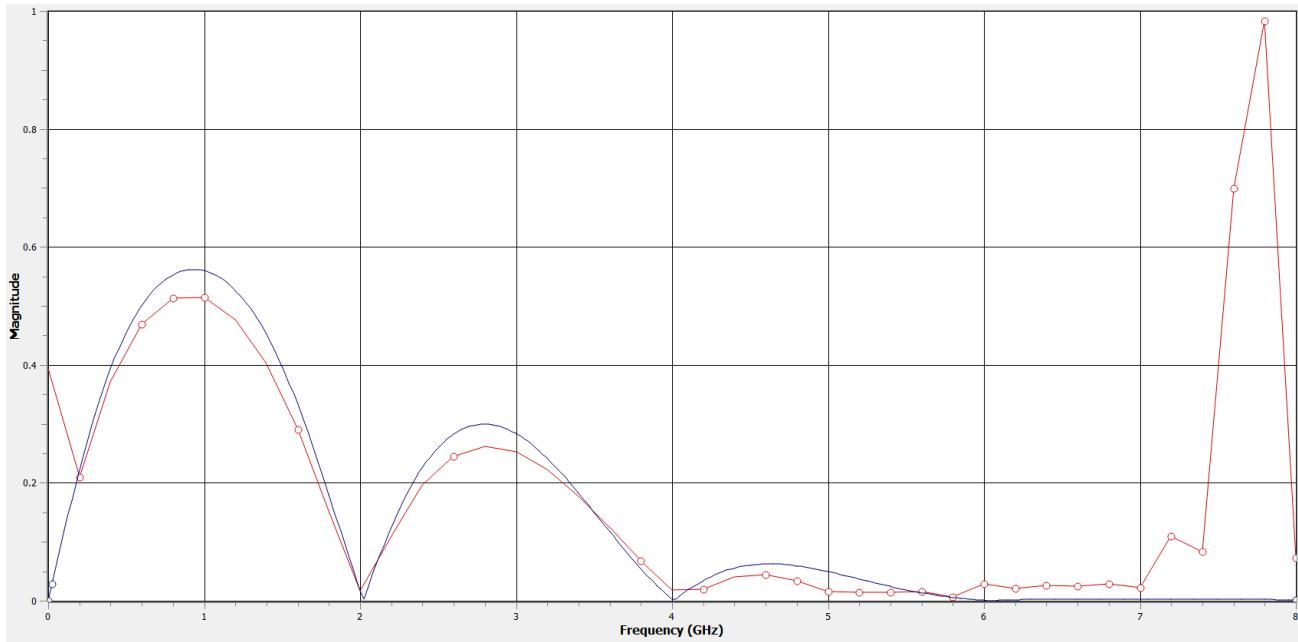
Now we can draw the taper line in the Sonnet geometry file. After we carefully drew the first half (10 sections) of the tapered line, we can copy and flip them, then connect 2 halves together to form the complete tapered line, and lastly we attach 1 port on each side.



Sweeps from 0 to 8 GHz with step size 0.2 GHz:



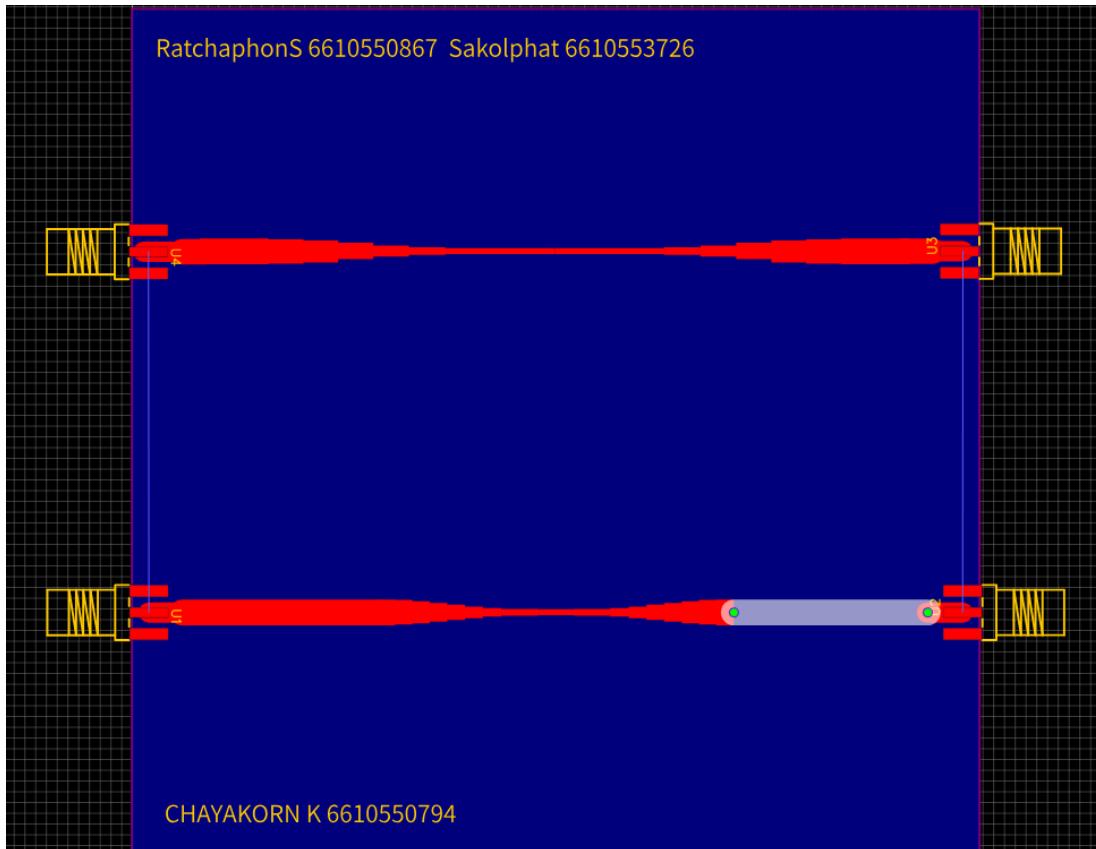
We can see how the geometry sweep (red line) and netlist sweep (blue line) closely resemble each other at 0 to 7 GHz frequency, which is acceptable.



Step 6: Fabrication

After getting acceptable results, we can export geometry file as .DXF file format, we can then import it to EasyEDA, we import .DXF file to the top layer and fill the shape, then erase the perimeter, connect the ports with the same specifications as the actual one, then we trace the copper from the first and last section to the connector.

After we confirmed the work is ready, we combine our work with Chayakorn to create the PCB with 2 tapered lines for the efficient fabrication and costing.



After this, we simply export it to be fabricated by JLCPCB.

Step 7: Testing

After receiving the fabricated PCB, we connect to ports, i.e. solder the connectors onto them, and test for actual performance.

The actual performance is plotted in orange, even though it is far from ideal result, it does show some resemblance at lower frequency.

