CS303 Logic and Digital System Design Lab 4

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We start from IDLE which is the initial step. It waits for an entered input and when in Read Phase or any other phase if reset input is given code comes back to the IDLE. When enter is pressed we move to the Writing Phase where we make the given matrix index , 1 , and there is a counter that counts the number of inputs while it is smaller than 5 it continues to take input but when it is equal to 5 we move to the Read Phase, I showed it in 2 parts because when we read we do not directly output the Z there is a delay in there so in Read Phase 1 X and Y is taken and read_phase_2 is initialized to 1 and if statement is finished so we move to the next clock stage this procedure helps us the maintain the Z=0 until enter is pressed because as you can see from my code X and Y is taken and also read_phase_2 is initialized to 1 this takes us to the next phase Read Phase 2 in the next clock phase. “posedge clk” part in always helps me to make sure that I sample the input signal at the positive clock edge. Second part of always is ”posedge rst” checks if rst operation is inputted or not if it is inputted it is directly initialized in the first if statement. In the second if statement enter input is checked and writing phase starts it makes the X and Y inputted index 1 and there is readding phase after that one when counter equal to 5. As I explained above at the end of the clock phase X and Y equated to X Y while Z is zero before these we made sure that enter is pressed but as these happens clock phase is done and output is X Y and Z as zero in the next clock phase as read_phase_2 became 1 Z is outputted with X and Y as it has to be.