CS-303

Lab 4: Matrix Input/Output

Fall 2024

Due: 09/12/2024, 23:59 AM (No late submission)

In this lab you are required to design a Verilog module that realizes input and output operations from a four by four matrix.

Y\X	00	01	10	11
00				
01				
10				
11				

Your top module will have the following ports. You are required to use this template. Each change in module name, port names or definitions will reduce your grade by five points.

```
module matrixops (
  input            clk  ,
  input            rst  ,
  input            enter,
  input      [1:0] X    ,
  input      [1:0] Y    ,
  output reg       Z
);
```

Your module will be a sequential design. You will realize the module according to the following requirements.

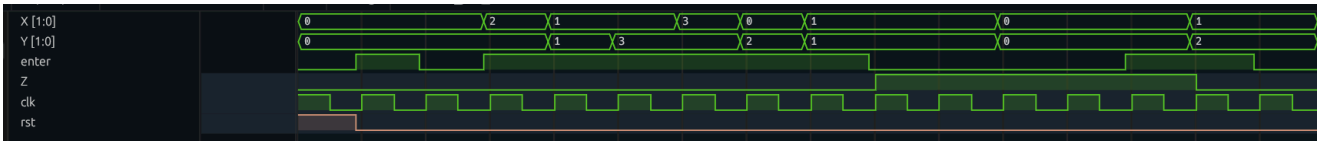
- The module needs to sample the inputs signals at the positive (rising) clock edge.
- The module needs to reset and initialize all of its outputs and internal variables to defaults when `rst` is set to high.
- It will wait until the `enter` signal has been set to high and will not change any internal variables while waiting. The first `enter` signal acts like a start signal. It will not write to the matrix or sample the `X`, `Y` inputs at the first occurrence of the `enter` signal being high at the positive clock edge.
- Once the initial `enter` signal arrives it will expect five input sets from the user. The inputs are as follows.
  - `X` coordinate: a 2-bit value of the cell's X coordinate
  - `Y` coordinate: a 2-bit value of the cell's Y coordinate

    - `enter` signal: a 1-bit signal signifying the submission of final values for `X`, and `Y`. Contents of the cells can be zero (empty) or one (full). When you select a coordinate and press `enter` you fill that cell.
- You will only get inputs when the `enter` is pressed. Otherwise, the module should wait for the next input.
- After getting the five input sets, it will expect coordinates to be supplied by the user to display its contents. Initially , `Z` will stay as zero until it gets the first coordinate and the user presses `enter`. `Z` will keep its previous value until we supply a new coordinate and press `enter`.
    - `Z` signal: contents of a cell, given the user supplied the `X`, `Y` coordinates and pressed `enter` (set `enter` to high)

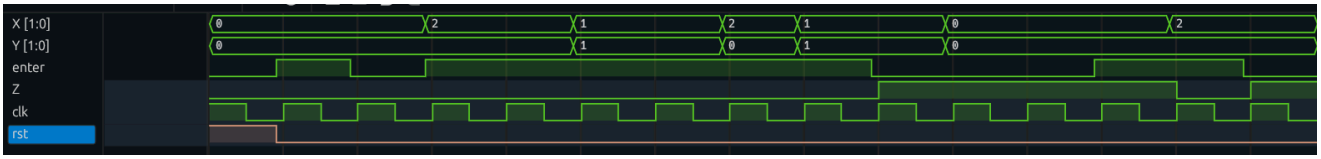
Here are some example waveforms for you to take as reference while designing.

> **Questions?**
>
> If you have any questions or think there is an edge case not represented here, send an e-mail to selim.kirbiyik@sabanciuniv.edu

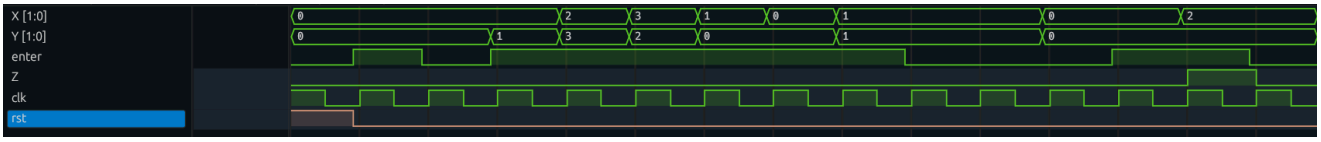
Test Case 0



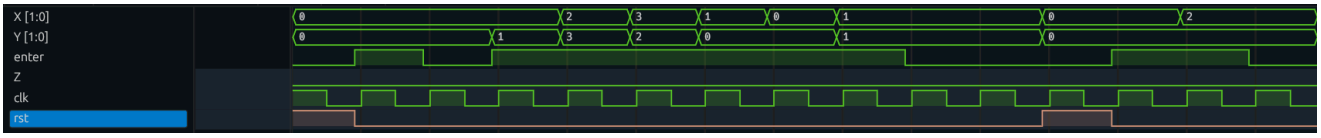
Test Case 1



Test Case 2



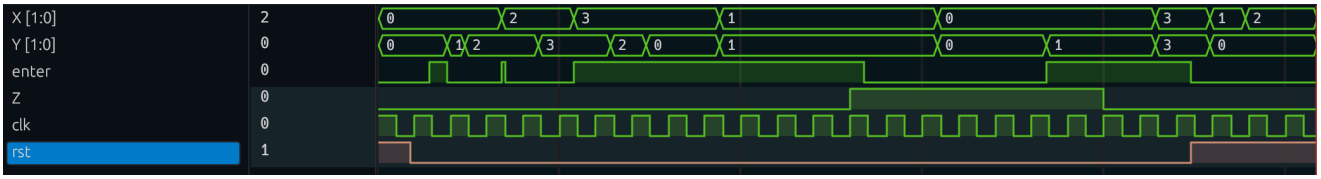
Test Case 3



Test Case 4

Test Case 5

Test Case 6



The following summarizes what you should do before and during the lab session.

Before the lab:

1. Design your circuits using Verilog.
2. Test your circuits according to the expected behavior.
3. Write a report of your design explaining your design.
    1. Draw your state machines.
    2. Explain how you handle the inputs. How do you ensure that you sample the input signals at the positive clock edge?
    3. Explain how you handle outputs. How do you make sure that `Z` stays at zero until user presses `enter` and requests the content of a given coordinate?
4. Submit your work, as much as you've done, through SUCourse as a zip file. Name of the zip file must be "`{SUID}_lab3.zip`" (e.g. If your SUID is 26797, your zip file must be "`26797_lab3.zip`").
    1. Include your Verilog files (all modules, testbench).
    2. Include your simulation waveform.
    3. Include your report in either PDF or Word format.

At the lab:

1. Demonstrate your report to the assistant.
2. Answer questions regarding your work.

Notes:

- You will work individually. No group work allowed.
- You will be required to demonstrate your work to the lab assistant as (s)he instructs.
- No late submissions.

- **Do not change the module, input and output signal names.** Each (signal name, module name) change reduces your grade by five points.
- **Do not use any verilog features that you did not see in the lectures.** This will be seen as a source of plagiarism.