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Lab 9 Post Lab Report

Introduction:

In this lab, we executed a Mealy state machine. We used a clock in order to implement the Mealy machine and included a pause and resume button. The counter was on the seven segment display and we were able to visually test the circuit to see if the functions were correct and worked properly.

Procedure:

We created several Verilog files to control different operations, then by replacing the lab9.v file with the different Verilog files, we were able to have the board operate as wanted.

Answering the Questions:
- Yes, the state diagrams and state tables from our prelab were correct.
- This change is a problem because it completely eliminates the check for PR'. This causes both the truth table and Verilog to be changed. If not adjusted for, then values will be incorrect when inputting combinations such as PR'.
- If the PR button was pressed for a long time then the time at which the button was pressed and the time which the button was released will be different. This could cause the button to act weirdly and possibly give a value which the user did not want. A way to resolve this would be to implement a Mealy state machine that calculates the output during the input.

Conclusion:

We felt that this was a good final lab as it culminated all the concepts into 1 lab. The lab also had a good flow and we did not encounter any weird issues like we did in previous labs.

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lab9.v   UpCounter_6bit.v   bin_7seg.v   BCD_enco

Table of Contents

Flow Summary

<<Filter>>

Flow Status

Quartus Prime Version

Revision Name

Top-level Entity Name

Family

Device

Timing Models

Total logic elements

Total registers

Total pins

Total virtual pins

Total memory bits

Embedded Multiplier 9-bit elements

Total PLLs

20

40

40

0

0 / 3

0 / 5

0 / 4

Compilation

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programm

Timing Analysis

EDA Netlist Writer

Edit Settings

<<Filter>>   Find...   Find Next

```
ID    Message
      **************************************************************
      Running Quartus Prime EDA Netlist Writer
      Command: quartus_eda --read_settings_files=on --write_settings_files=off lab9 -c lab9
18236 Number of processors has not been specified which may cause overloading on shared machine
199027 Can't generate output files. Specify command-line options to generate output files, or up
      Quartus Prime EDA Netlist Writer was successful. 0 errors, 2 warnings
```

ystem (1)   Processing (6)

Type here to search

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Flow Summary

🔍 <<Filter>>

Programmer - Z:/ELEN_21L/lab9/lab9 - lab9 - [lab9.cdf]

File   Edit   View   Processing   Tools   Window   Help

Search Intel FPGA

🔧 Hardware Setup... | USB-Blaster [USB-0] | Mode: | JTAG ▼ | Progress: | 100% (Successful) |

☐ Enable real-time ISP to allow background programming when available

	File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine
▶ Start	lab9.sof	EP4CE115F29	00580463	00580463	☑	☐	☐	☐
⏸ Stop								
🔍 Auto Detect								
✖ Delete								
📄 Add File...								
📄 Change File...								
💾 Save File								
📄 Add Device...								
⬆ Up								
⬇ Down								

TDI →

(intel)

EP4CE115F29

TDO ←

```
*************************
s=on --write_settings_files=off lab9 -c lab9
ed which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QS
and-line options to generate output files, or update EDA tool settings using GUI or Tcl script.
essful. 0 errors, 2 warnings
```