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Lab 4 Report

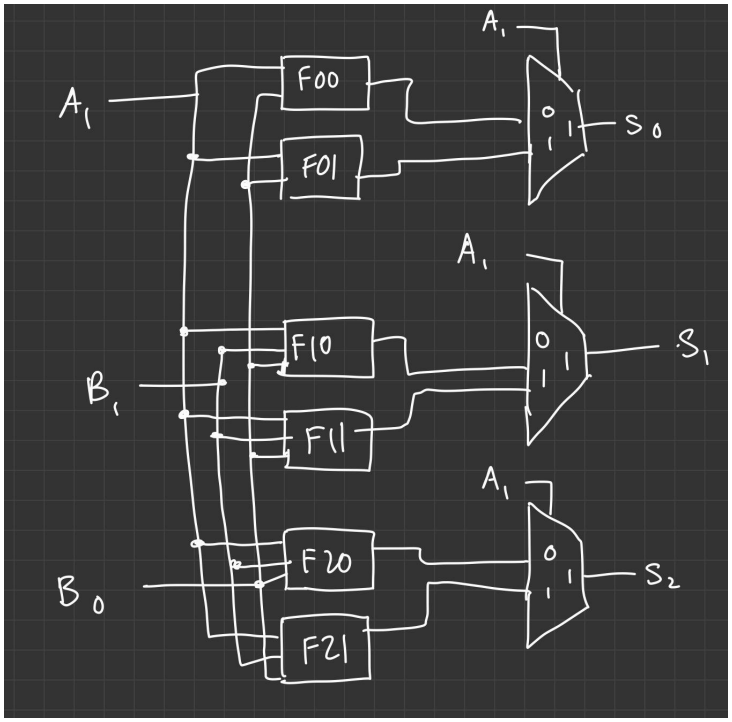
Introduction

In this lab we created a circuit which included 3, 2-1 MUX which allows S0, S1, and S2 to pass through depending on the conditions of F00, F01, F10, and F11. The tree inputs were A1, B1, and B0 which connected to F00, F01, F10, and F11 respectively. We found the relationships between these functions by creating a truth table (pictured below) and simplified the outputs using k-maps. Our logic functions ended up being:

S0F0=A0⊕B0,
S0F1=A0⊕B0,
S1F0=!A0B1+B1!B0+A0!B1B0,
S1F1=!A0!B1+!B1!B0+A0B1B0,
S2F0=A0B1B0,
S2F1=B1+A0B0.

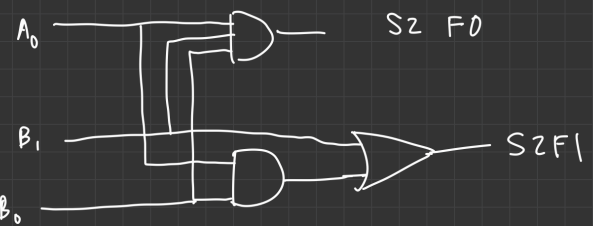
Conclusion

We had very few problems with this lab, however, the challenges for this lab included learning to use Verilog and seeing how the code interacts with the circuit. Also, creating multiplexers in Quartus and corresponding that with the code was difficult because the system did not recognize the file names correctly and we continued to get errors that were difficult to fix. For example, the compiler kept telling us that we did not have a file called “Lab 4” which we supposedly addressed in our code. We never addressed a file called “Lab 4” in our code, so identifying what exactly that meant and how to solve the problem was difficult and not intuitive. We ended up having to reset by creating a new project and transferring the Verilog code into separate files. Overall, building the circuit and code was fairly simple, however, implementing it in Quartus was challenging.



ECEN 21 Prelab Lab 3
Seana Comers

A1	A0	B1	B0	S2	S1	S0	Sum 10
0	0	0	0	0	0	0	0+0 = 0
0	0	0	1	0	0	1	0+1 = 1
0	0	1	0	0	1	0	0+2 = 2
0	0	1	1	0	1	1	0+3 = 3
0	1	0	0	0	0	1	1+0 = 1
0	1	0	1	0	1	0	1+1 = 2
0	1	1	0	0	1	1	1+2 = 3
0	1	1	1	1	0	0	1+3 = 4
1	0	0	0	0	1	0	2+0 = 2
1	0	0	1	0	1	1	2+1 = 3
1	0	1	0	1	0	0	2+2 = 4
1	0	1	1	1	0	1	2+3 = 5
1	1	0	0	0	1	1	3+0 = 3
1	1	0	1	1	0	0	3+1 = 4
1	1	1	0	1	0	1	3+2 = 5
1	1	1	1	1	1	0	3+3 = 6



S0F0 = A0⊕B0
S0F1 = A0⊕B0
S1F0 = !A0B1 + B1!B0 + A0!B1B0
S1F1 = !A0!B1 + !B1!B0 + A0B1B0
S2F0 = A0B1B0
S2F1 = B1 + A0B0

S1 Verilog ②

```
module S1F0(A0, B1, B0, S1 F0);
    input A0, B1, B0;
    output S1 F1;

    and(z1, ~A0, B1);
    and(z2, ~B1, B0);
    and(z3, ~A0, B1, B0);
    or(S1F0, z1, z2, z3);
endmodule
```

S1 Verilog ①

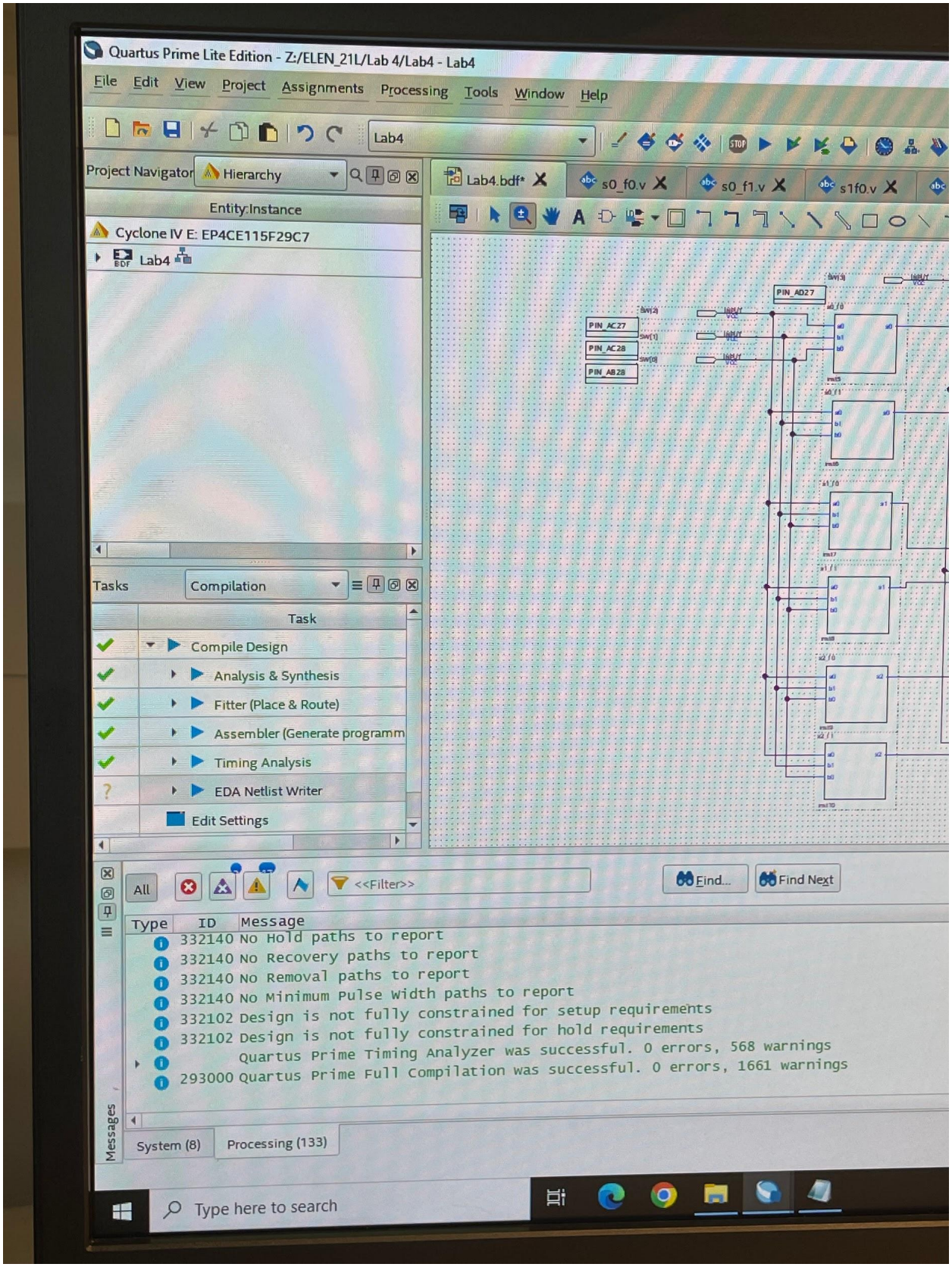
```
module S1F1(A0, B1, B0, S1F1)
    input A0, B1, B0;
    output S1F1;

    and (z1, ~A0, ~B1);
    and (z2, ~B1, ~B0);
    and (z3, A0, B1, B0);
    or (S1F1, z1, z2, z3);
end module
```

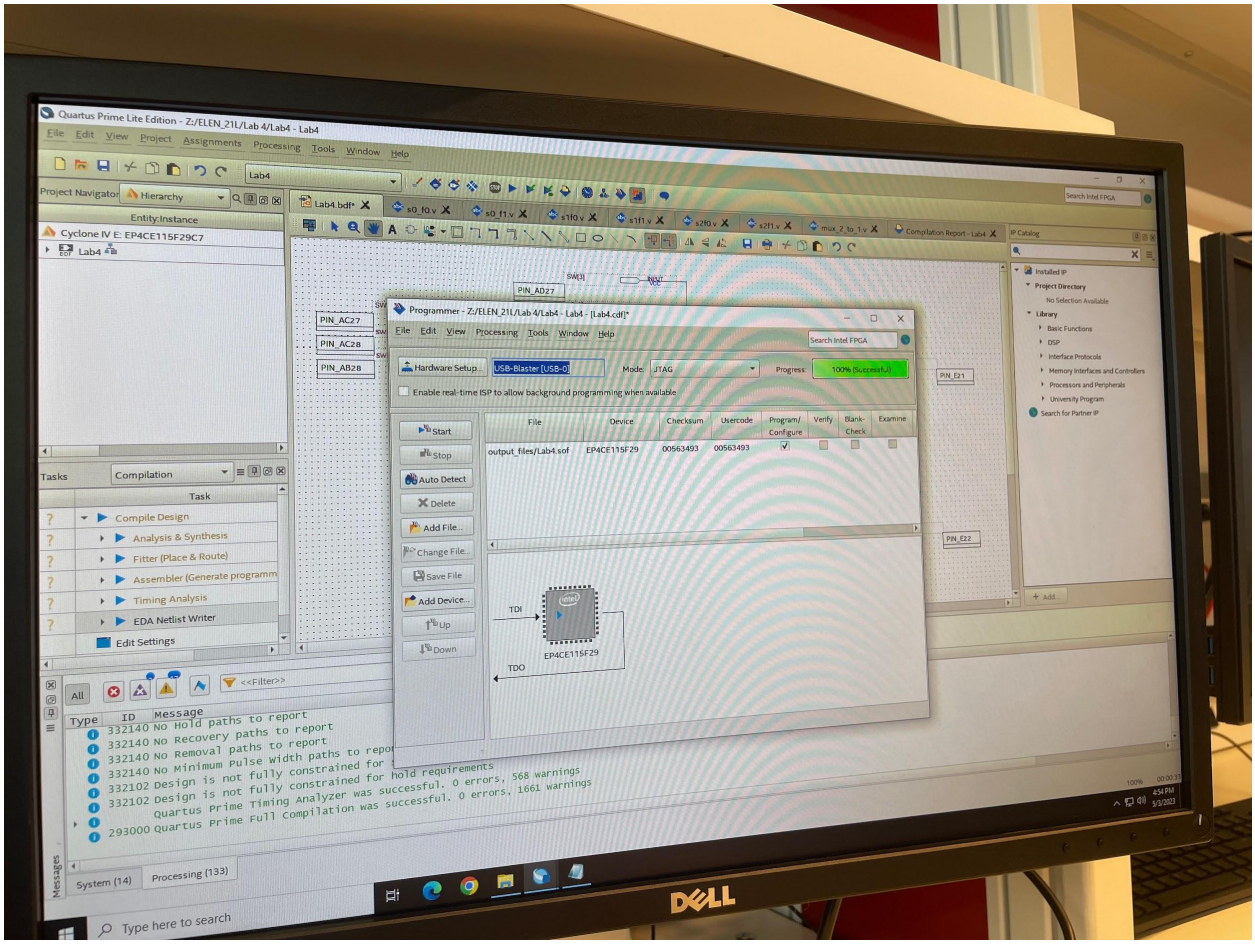
SOF0 Verilog

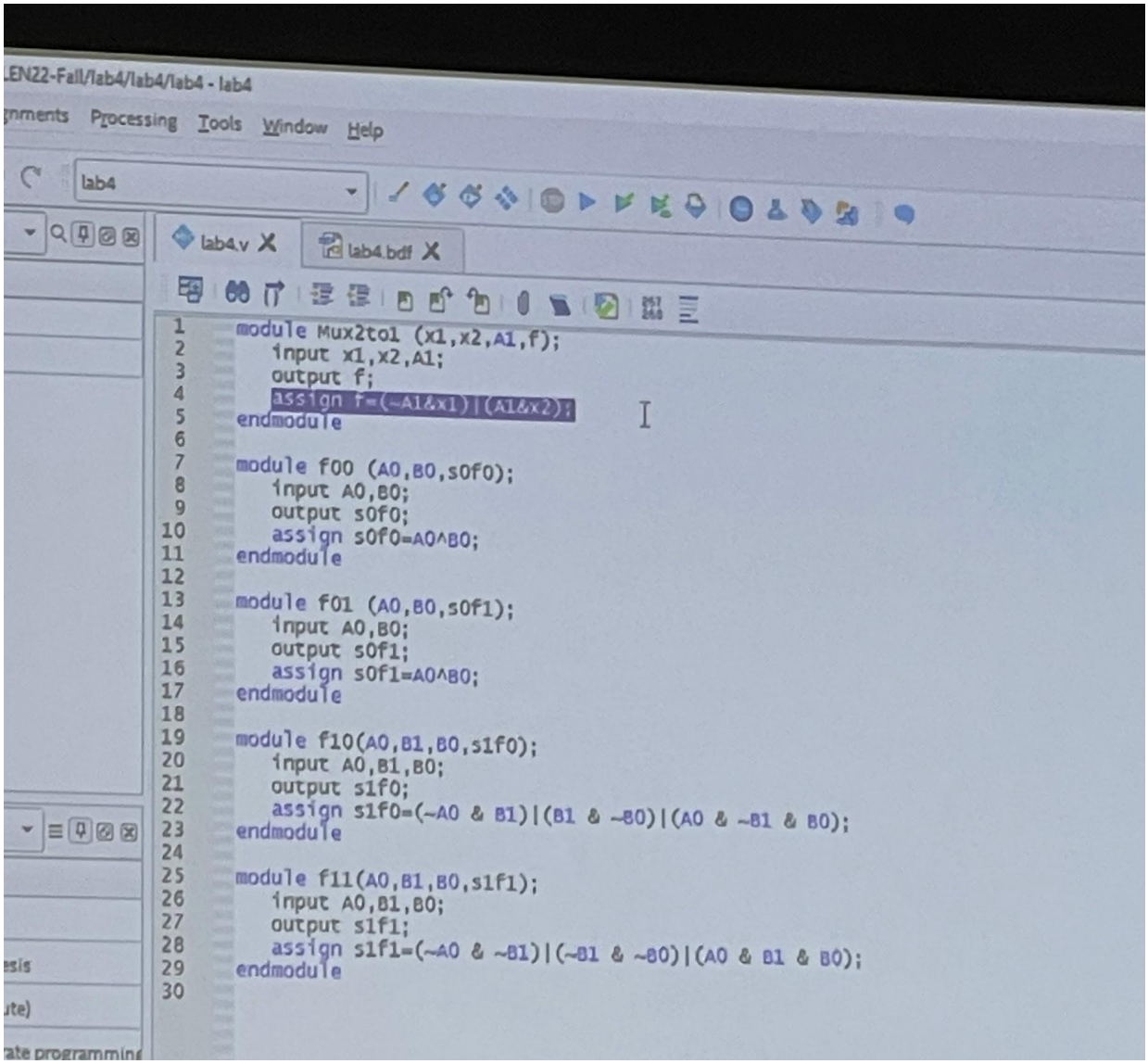
```
module SOF0(A0, B0, SOF0);
    input A0, B0;
    output SOF0;

    assign SOF0 = A0 ^ B0;
endmodule
```

SOF1 Verilog

```
module SOF1(A0, B0, SOF1);
    input A0, B0;
    output SOF1;

    assign SOF1 = A0 ^ B0;
endmodule
```


Quartus Prime Lite Edition - Z:/ELEN_21L/Lab 4/Lab4 - Lab4
File Edit View Project Assignments Processing Tools Window Help
Lab4
Project Navigator Hierarchy
Entity:Instance
Cyclone IV E: EP4CE115F29C7
Lab4
Lab4.bdf*
s0_f0.v
s0_f1.v
s1f0.v
PIN_AD27
PIN_AC27
PIN_AC28
PIN_AB28
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
Edit Settings
All
<<Filter>>
Find...
Find Next
Type ID Message
332140 No Hold paths to report
332140 No Recovery paths to report
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to report
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 568 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 1661 warnings
Messages
System (8)
Processing (133)
Type here to search


Quartus Prime Lite Edition - Z:/ELEN_211/Lab 4/Lab4 - Lab4
Programmer - Z:/ELEN_211/Lab 4/Lab4 - Lab4 - [Lab4.cdf]*
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
100% (Success)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
output_files/Lab4.sof
EP4CE115F29
00563493
00563493
TDI
TDO
EP4CE115F29
Cyclone IV E: EP4CE115F29C7
Tasks
Compilation
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
Edit Settings
Type
ID
Message
332140 No Hold paths to report
332140 No Recovery paths to report
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to repo
332102 Design is not fully constrained for hold requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 568 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 1661 warnings
System (14)
Processing (133)
Type here to search
DELL


EN22-Fall/lab4/lab4/lab4 - lab4
Processing
Tools
Window
Help
lab4
lab4.v
lab4.bdf
1 module Mux2to1 (x1,x2,A1,f);
2 input x1,x2,A1;
3 output f;
4 assign f=(~A1&x1)|(A1&x2);
5 endmodule
6
7 module f00 (A0,B0,s0f0);
8 input A0,B0;
9 output s0f0;
10 assign s0f0=A0^B0;
11 endmodule
12
13 module f01 (A0,B0,s0f1);
14 input A0,B0;
15 output s0f1;
16 assign s0f1=A0^B0;
17 endmodule
18
19 module f10(A0,B1,B0,s1f0);
20 input A0,B1,B0;
21 output s1f0;
22 assign s1f0=(~A0 & B1)|(B1 & ~B0)|(A0 & ~B1 & B0);
23 endmodule
24
25 module f11(A0,B1,B0,s1f1);
26 input A0,B1,B0;
27 output s1f1;
28 assign s1f1=(~A0 & ~B1)|(~B1 & ~B0)|(A0 & B1 & B0);
29 endmodule
30