COURSE INFORMATION

Instructor:

Associate Professor Senol Mutlu
Room: KB206D, inside BETA Lab., Tel: (212) 359-7442
e-mail address: senol.mutlu@boun.edu.tr

Lectures:

Wednesday 1-3 p.m. Class:To be determined.

Office Hours:

Monday 1-3 p.m. at my office at KB206D.

Laboratories:

There will be four laboratory sessions. Tuesday 1-3 p.m., Friday 10 a.m.-12 p.m., Friday 1-3 p.m. and Friday 3-5 p.m. at Network & Electrical Measurement Laboratory. You will have 7 Labs and 1 Hardware Project as a final exam.

Credits: 3

Teaching Assistants: Ozan Ertop (ozan.ertop@boun.edu.tr), Hikmet Çeliker (hikmet.celiker@boun.edu.tr, Bayram C. Akdeniz (bayramakdeniz89@gmail.com), Reza Ashrafi (reza.ashrafi@boun.edu.tr).

Course Description:

EE 240 is the laboratory class complementary to EE142, an introductory course of digital design. Implementations of combinational and sequential digital circuits using discrete integrated circuits (IC) and field programmable gate arrays (FPGAs) are taught. A hardware description language (VHDL) is introduced.

There are 7 labs and 1 hardware lab project. These labs introduce you to digital circuits and Computer Aided Design (CAD) tools. You use advanced computer integrated virtual instrumentation hardware and software from National Instruments and advanced field-programmable logic chips and boards along with the associated PC-based design software from the Xilinx and Digilent corporations. The labs and projects are prepared to give you the ability to use CAD tools to design, simulate and implement digital circuits.

Memory, sequential circuits such as counters, state machines and control units and other digital system examples are studied in the lectures. An in-class midterm is given.

Website:
https://moodle.boun.edu.tr/login/index.php
You can reach this website through the registration website. Login to the registration website (http://registration.boun.edu.tr/). Choose "Go to **BOUN-Moodle**" option.
Lecture slides, laboratory manuals and other additional course materials and your grades will be published on this website.

Required Textbook:
Digital Design by Morris Mano 4th Edition.

Reference Texts:

Nexys 3 Board Reference Manual, Digilent Inc.
(http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,897&Prod=NEXYS3)
Xilinx ISE Webpack Manual
http://www.xilinx.com/products/design-tools/ise-design-suite/ise-webpack.html
http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/ise_tutorial_ug695.pdf

Laboratories:

1. Lab 1 – Introduction to SC-2075 & LABVIEW and using them in the implementation of digital logic with IC gates
2. Lab 2 – Hardware lab for combinational circuits using IC gates
3. Lab 3 – Introduction to XILINX FPGA & Project Navigator and using them in the implementation of sequential circuits
4. Lab 4 – Implementation of Counters using IC gates and FPGAs
5. Lab 5 – Conversion of 6-bit Floating Point Numbers into Sign-Magnitude Representation and its FPGA Implementation.
6. Lab 6 – Up/Down BCD Counting of the Number of Pushes on Buttons and its FPGA Implementation
7. Lab7 – Simple VGA Driver to Display All Possible Colors

Lab groups and which lab sessions to attend will be announced by the TAs. They will have a sign-up sheet at the BETA lab. Please sign up only one of the lab sessions. If you have a schedule conflict, please contact the TAs or me as soon as possible. Get in touch with your labmate as soon as possible. Each group will be provided with a box of electronic components and materials at the beginning of each lab. Please make sure that you observe the following:

· In order to pass the course, all labs must be completed. Just attending a lab and showing an effort on it may result in a low lab grade but it would mean you have completed that lab. In a semester, you can have only one make-up lab. In order to have the make-up lab, you should have a valid excuse.

You should finish your lab during your lab session. Otherwise, if you complete your lab by the next lab session after yours, you will have a penalty of 15% cut. For example if yours is on Wednesday and you show your finished work on the Friday sessions, 15% of your grade will be cut. If you finish on the second lab session after yours, there will be a 30% cut (Yours is on Wednesday, and you show on the next Wednesday). Showing on the third lab session after yours will result in a 50% cut (Yours is on Wednesday, and you show on the next Friday). After this, your lab grade will be finalized and cannot change. If it is a two-week lab (check the schedule), you can finish it by your lab session on the second week. If it is a two-week lab and you finish your work on the first week, you do not have to attend the lab on the second week. You must attend the first week.

· It is each group's responsibility to take good care of the materials throughout the semester.

· Each group is responsible for turning in their components at the end of the lab –where all the components are complete and functional.

Lab Manuals are available online on the website of the class. You can also make its hardcopy using the copy room of the department.

Please note that most of the labs will require you using ISE Xilinx Webpack. ISE Xilinx is available in zipped format and you can get a copy of it on CD or DVD from the lab manager (Yalçın Turgay) of the Network and Electrical Measurement Laboratory.

Before you come to a lab session…
Make sure that you read and understand the experiments.
Make sure that you have all the required datasheets for the IC's that you will be using and prepare the wiring and connections of the design.
Your lab grading for the labs will be based on your preparedness and your performance during the lab.

Hardware Lab Project
The purpose of "hardware lab project" is to make you design and implement your own digital circuits in hardware. You may work in groups of two at max. You may choose your group member for the hardware project as you will.

In this project, you will design and implement a digital circuit of your own choosing. There is no restriction on the design except that it should be more sophisticated than the regular labs you did during the semester.

You will be responsible for getting the required components from Selanik Pasaji or Kadikoy, so your circuit should not contain expensive components. Also your circuit should not be too simple or too complex (so that it does not function!).

You are free to look at books, web or other sources for possible circuits. If you decide to build such a circuit, make sure you give full reference. Also, in that case, you should also introduce a change to the circuit that makes it function slightly different. You should explain this fully in your report. You should hand in a 1-page proposal by the date given on the schedule. In this proposal, you should include a project title, the group members and a short description of your project. The description should specify the inputs, outputs and functionality of your circuit

You should then arrange time with your group to go into the lab and implement your circuit on the board. If you can, do a Xilinx ISE design first to make sure that your circuit works as it should. You will make a demo to the TAs during the final period of the term. You should hand in a project report (in the form of final project lab report form) including your problem, the drawing of your circuit and a very SHORT description of how it works as well as all the references by the end of that week.

Guidelines for Writing Final Project Report
Please refer to Report Writing Guidelines for a detailed discussion regarding how to prepare the report. A report template (in pdf or in doc) is also available. The report should contain a short and clear description of your design – including a short description of your problem (inputs and the required outputs), the steps you took in finalizing your implementation and results from sample inputs if asked to do so. You may look at a sample project report from former years. Please make sure that you use only your own sentences. If you need to use sentences or information (anything such as knowledge,

circuit drawings, pictures, graphics) from external source, make sure that you refer to them by using the following conventions:
Place where you use somebody else's work [XXX] where XXX specifies the number of your reference.
"…….. sentence of somebody else ….." [YYY] where YYY specifies the number of your reference. At the end of your report, you then add a section named **References** and list all the references, given full information such as who said, where, when, what pages, what html etc. as follows:
References
[XXX] ……Mano, M. Digital Design, pp: 140-142, Addison-Wesley, 1999.
[YYY] http://www.ee.boun.edu.tr
(These are examples to give you the idea!)

Project Demos: You will make a demonstration of your final project during the last week of the final exam period of the semester.

Midterm: There is only one midterm. Its date is indicated in the course outline.

Grading Policy:
Course grades will be assigned according to the following grading formula. *Please note that this formula is tentative*; students will be informed of any major changes.

Labs..... 50%
(Lab1 5%, Lab2 5%, Lab3 6%, Lab4 7%, Lab5 8%, Lab6 9%, Lab7 10%)
Project 25%
Midterm..... 25%

In most cases students will be made aware of the basic statistics (mean, median, and standard deviation) for each assignment.

Course Outline (Tentative)

Mo.	*Date*	*Material Covered*	*Assign.*	*Comments*
Feb.	**9**	Introduction, FPGAs		
	16	Inverter, switch, electrical current values in digital IC, LED, resistor, delay Review of Sequential Circuits		
	23	Review of Sequential Circuits	***Lab#1***	
Mar.	1	Review of Sequential Circuits	***Lab#2***	
	8	State Machines	***Lab#3***	
	15	Introduction to VHDL, Structural description of hardware in VHDL	***Lab#3***	
	22	Dataflow description of hardware in VHDL	***Lab#4***	
	29	Dataflow and Behavioral description of hardware in VHDL	***Lab#4***	
Apr.	**5**	Behavioral description of hardware in VHDL	***Lab#5***	
	12	State Machine Examples, Counters	***Lab#6***	
Apr.	**19**	**Apr 18-Apr 22 Spring Break**		
	26	Memory, Hamming Code	***Lab#6***	
May	**3**	Programmable Logic Devices and FPGAs	***Lab#7***	
	10	**Midterm**	***Lab#7***	
May	**13**	**Project proposals are due, Projects start**		
May 13th, Friday, Last Day of Classes				
May 17th-May 31th Final Period, **Hardware Project Demos and Reports**				

According to the Ethics Code of the EE Department, you have to perform all graded work individually. All assignments are to be completed independently by all students, except as specified. Although no interaction is permitted during tests, students are encouraged to discuss homework problems **at a conceptual level** with others taking the same course. Copying the homework solutions from any source, be it another student, an assignment from a preceding term, etc., defeats the educational intent of the effort, and will be subject to disciplinary action.