EE333 FALL 2017 ASSIGNMENT#3

1. Answer the following with 40 ***words*** or less for each (you get +1 bonus if the answer is shorter than 21 ***words*** and is still sensible – full sentences are not a necessity, but be clear.). **(6% each)**

a) Identify two diodes (pn junctions) in a standard MOSFET structure. Can you identify a parasitic BJT as well?

b) How should these diodes be biased (forward/reverse)? Based on your answer, comment on MOSFET biasing requirements for NMOS and PMOS.

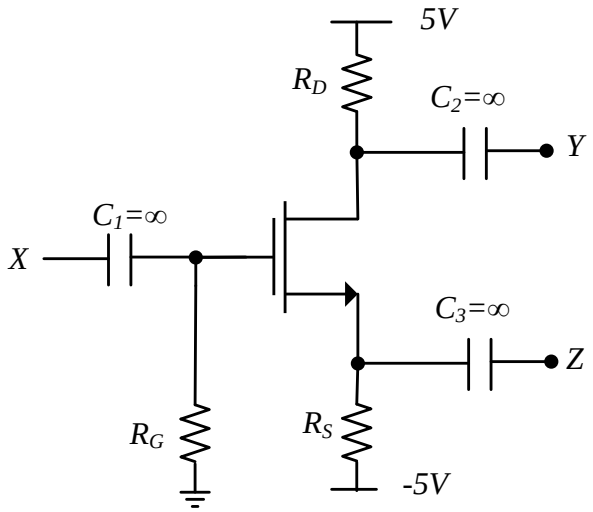
c) What are the different operation regions in a MOS? Compare r_{DS} for these regions, based on the presence and shape of the channel between the drain and source terminals.

d) Describe what channel length modulation is, and how it is affected by the design parameter L.

e) An NMOS device is fabricated on a p-type bulk. Denote the initial acceptor concentration of the bulk as N_A and assume $V_{SB}=V_{GS}=0$ initially. When one starts applying positive gate voltage V_{GS}, electrons start accumulating in what will become the channel region. Denote the electron concentration in channel region as an increasing function of gate voltage as $N_e(V_{GS})$ @ $V_{GS}\geq 0$. Let us define a threshold voltage quantity V_t so that when $N_e(V_{GS}=V_t) = N_A$. Knowing this [and keeping in mind that $N_e(V_{GS}=0)$ is nonzero because some electrons exist in the channel as minority carriers of the p-type semiconductor] comment on how V_t would change for:

- Increased acceptor concentration in bulk N_A,
- Increased temperature,
- Increased V_{SB}.

2. For the MOSFET below, $k'_nW/L=800\mu A/V2$, $V_t=1V$ and $VA=40V$, and all capacitor values are $330\mu F$. Use a signal source with 10mV amplitude, 1kHz frequency and 10kΩ resistance.



a) Find the values of RS, RD and RG so that $I_D=100\mu A$, the largest possible value for RD is used while a maximum signal swing at the drain of ±1V is possible, and the input resistance at the gate is 100kΩ. **(20%)**

b) Use the following model to verify the desired DC operation in spice by observing the operation points (.op simulation). **(10%)**

.model mynmos nmos (kn=0.8m , vto=1, lambda=0.025)

c) If the terminal Z is grounded, terminal X is connected to the signal, and the terminal Y is connected to a load resistance of 40kΩ, find A_{vo}, A_v, and G_v. Verify with simulations. What is the maximum peak voltage allowable for the signal source? Change the signal source amplitude to the double of this value and observe the output. **(20%)**

d) If the terminal X is grounded, terminal Z is connected to a current source delivering a signal current of 10μA and having a resistance of 100kΩ, find the voltage that at Y. Verify with simulations. **(20%)**

You can write your hand calculations on a paper and add it to the rest of the homework. Provide the relevant plots as well as the circuit schematics. Make sure the numbers are visible and the figures can easily be referred to.

Do not waste ink, paper and material. **(bonus: 5% pts)**