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**ID: 1191408 Section:5**

**Q1 IN HDL HOMEWORK**

**FIRST SEMESTER 2021\2020**

**DIGITAL SYSETMS ENCS2340**

**Mux4\*1:**

**In this question we have 2 Mux4\*1**

**Code:**

module Maree(OUT,w,x,y,z,s0,s1);

input w,x,y,z,s0,s1;

output OUT;

wire S0bAR ,S1bAR,t1,t2,t3,t4;

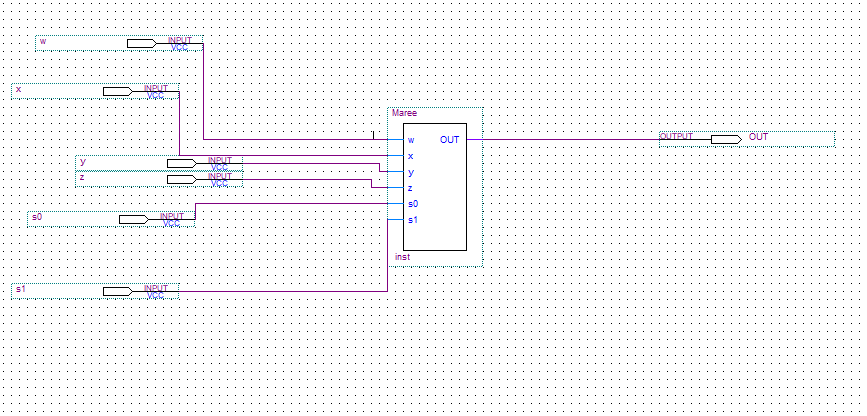
not (S0bAR,s0),(S1bAR,s1);

and (t1,w,S0bAR,S1bAR),(t2,x,S0bAR,s1),(t3,y,s0,S1bAR),(t4,z,s0,s1);

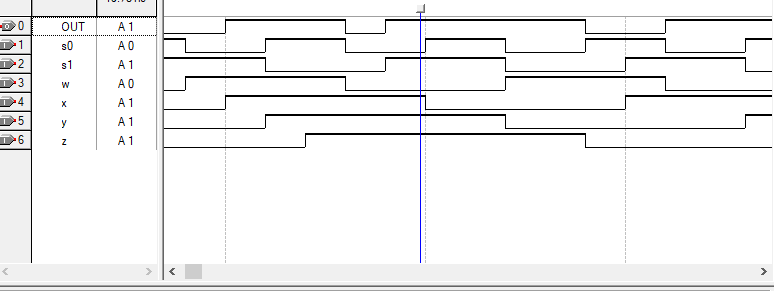
or(OUT,t1,t2,t3,t4);

endmodule

**Block Diagram:**

****

**Simulation:**

****

**Mux2\*1:**

**In this question we have one Mux2\*1**

**CODE:**

module Ayham(Y,w,x,S);

output Y;

input w,x,S;

wire t1,t2,SbAR;

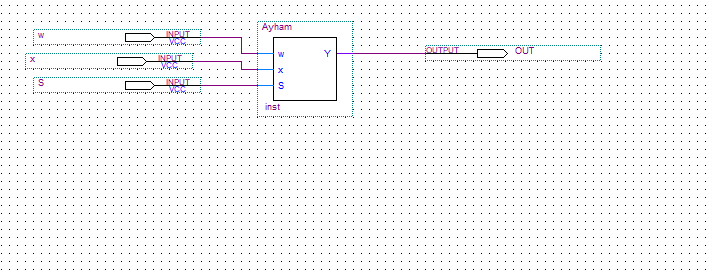
and (t1,w,S),(t2,x,SbAR);

not (SbAR,S);

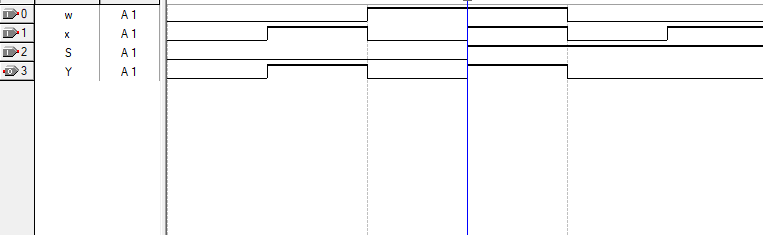
or(Y,t1,t2);

endmodule

**Block Diagram:**



**Simulation:**

****

**The Whole System:**

**CODE:**

module id1191408(I,S,OUT);

input[0:7]I;

input[0:2]S;

output OUT;

wire w1,w2;

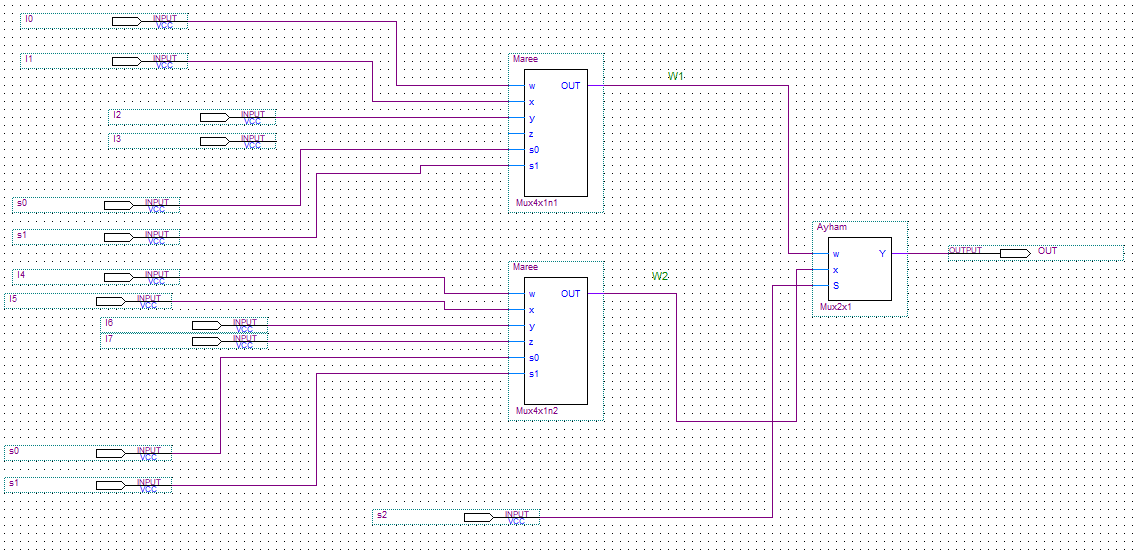
Maree X1(I[0],I[1],I[2],I[3],S[1],S[0],w1);

Maree X2(I[4],I[5],I[6],I[7],S[1],S[0],w2);

Ayham X3(w1,w2,S[2],OUT);

endmodule

Block Diagram:



Simulation:

