

Figure 1

Please note that the only contiguous samples in figure 1 are the data values 128, 0, and 5 of Data[7..0]. The data samples 10 and 15 are from a later samples.

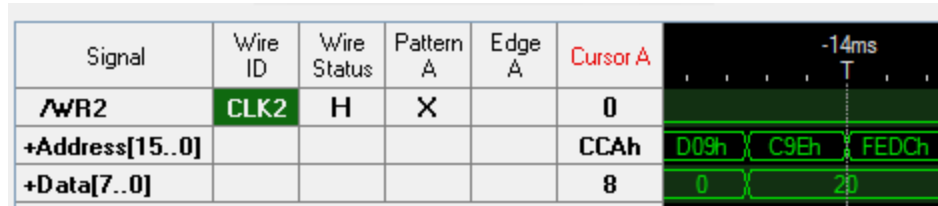


Figure 2

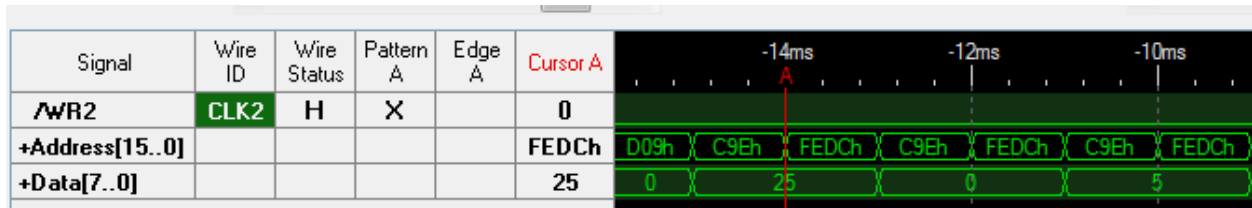


Figure 3

Figures 1, 2, and 3 show the output of the logic analyzer when utilizing the macro routine in the heap report required element of the lab. The macro is called before and after each function call in main. At each debug macro instance, there is to be a write to memory location 0xFEDC. The values written are values 0 to 25 in increments of 5. Figure 1, 2 and 3 show the writes in memory and the correct values that should be written after each function call in main. In addition, to capture these values the logic analyzer was set to sample on the 8051 /WR signal and triggered off the debug memory write location 0xFEDC.