Supplemental Timing Calculations

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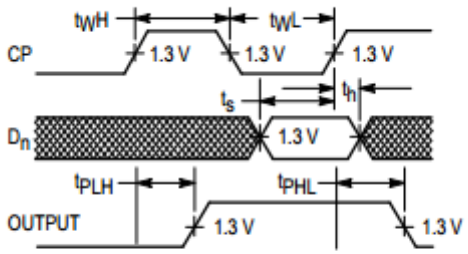


Figure 5

The figure above describes the setup and hold times for the 374' latch. The setup time is when the data is valid and the clock pulse goes high. The hold time is when the clock pulse goes high to when the data is not valid anymore. The timing diagram for the 374' latch gives an indication of what to look for in the C501 datasheet for the setup and holding times for the data being sent out of the 8051. By comparing figure 5 above and figure 15 below, the setup and hold time for the 8051 can be identified. The CP in figure 5 is mostly the /WR in Figure 15 and D_n in figure 5 is the Port 0 signal in Figure 15. Therefore, the setup time is when Data OUT is valid to when /WR goes high and the hold time is when /WR goes high to when Data OUT is not valid anymore. There are propagation delays that are introduced by the SPLD and 374', which will be discussed later.

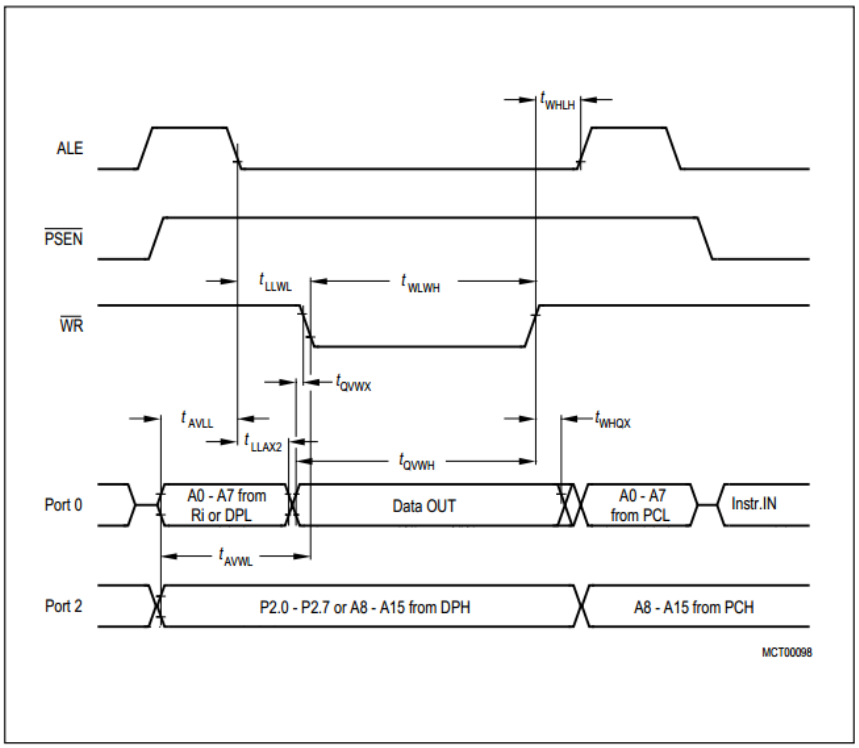


Figure 15
Data Memory Write Cycle

More specifically, figure 15 above describes the timing for a memory write cycle. A memory write cycle is used to trigger the 374' latch to store a count value indicating where the program is in its routine. The program writes a count value to memory and this value is captured by the latch. In order to do this, the latch is trigged on the /WR signal. The SPLD was programmed to drive the 374' latch with a CLOCK signal. The CLOCK signal is comprised of /WR & !A15. This ensures that when the /WR goes high (in the appropriate address range), the 374' will latch the Data OUT that resides on Port 0. To ensure the 8051 meets timing requirements, we need to compare the setup time of data for the 8051 (t_{QVWH}) and propagation delays introduced by SPLD (t_{pd}) and 374' latch (t_{plh}) with the setup time requirements for the 374' latch. Likewise, the hold time of data for the 8051 (t_{WHQX}) and propagation delays introduced by the SPLD (t_{pd}) and 374' latch must be compared to the hold time requirements for the 374' latch.

8051 Timing Constraints

$$t_{clcl} = \frac{1}{11{,}059{,}200} = 90.4224\ ns$$

$$8051\ setup\ time = t_{QVWH} = 7 * t_{clcl} - 50 = 7 * 90.4224 - 50 = 582.96\ ns$$

$$8051\ hold\ time = \ t_{WHQX} = t_{clcl} - 20 = 70.4224\ ns$$

SPLD Propagation Delay

$$t_{pd} = 7.5\ ns$$

Latch 374' Propagation Delay

$$t_{plh} = 28\ ns$$

374' Timing Requirements

$$setup\ time = 20\ ns$$

$$hold\ time = 1\ ns$$

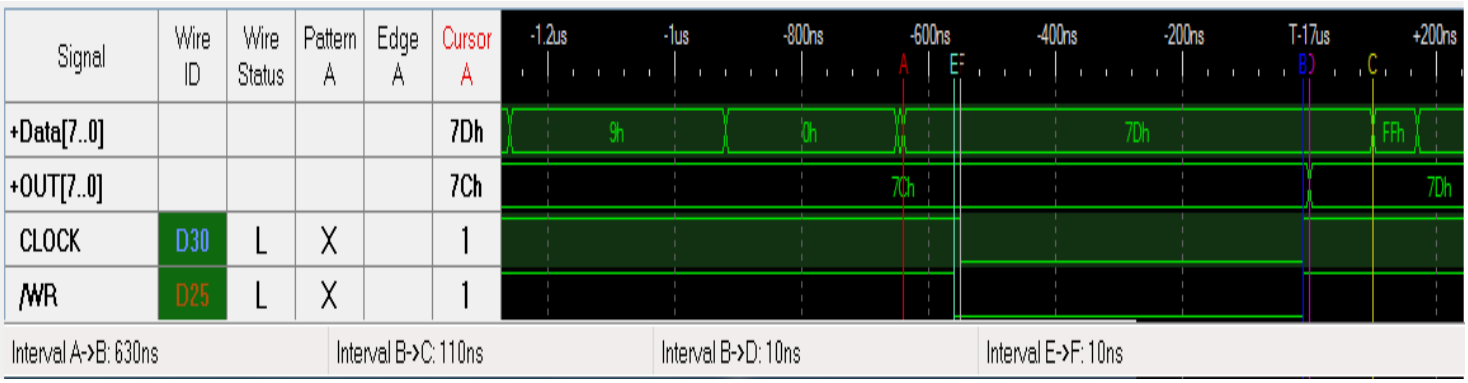
Measured Setup and Hold Up Times

$$8051\ setup\ time = 630\ ns$$

$$8051\ hold\ time = 110\ ns$$

$$SPLD\ propagation\ delay = 10\ ns$$

$$374'propagation\ delay = 10\ ns$$



Based on the measurements, the 8051 meets timing constraints. The logic analysis above shows the measured setup and hold times for the 8051. Note that the clock pulse coming out of the SPLD to clock the 374' latch, functions on the logic Clock = WR & !A15. A15 is included to ensure no latching in address space 8000h and above. The time from data is valid (cursor A) to when the clock pulse is high (cursor B) is the setup time. The time from when the clock pulse (cursor B) is high to when the data is no longer valid (cursor C) is the hold time.

As discussed earlier, there is propagation delay that changes the phase of the 8051 outputs. This propagation delay can be seen in the SPLD and the 374' latch. The SPLD is driving the 374' latch with the CLOCK signal. /WR goes into the SPLD and CLOCK comes out of the SPLD. When /WR does its first transition from LOW to HIGH, the CLOCK should follow the same pattern, however, there is a slight delay. From the /WR transition (cursor E) to the CLOCK transition (cursor F), the delay is 10 ns. Notice though that the CLOCK signal is only relevant on a rising edge and you will notice that there is no delay at that point. Likewise, the propagation delay in the 374' is identified as the time between when the 374' sees a rising edge (cursor B) to when the data is actually latched (cursor D), which is 10 ns. This suggests that the propagation delay changes the phase of the 8051 setup and hold time by 10 ns. All in all, the measured setup and hold up times for the 8051 are much larger than what is required by the 374' and are even larger than what the data sheet reflected.