You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by **Friday, September 26, 2014 (Required Elements) and Wednesday, October 1, 2014 (Supplemental Elements).**

Print your name below, sign the honor code pledge, circle your course number, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: _Ali Ismail_

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: _Ali_

Signoff Checklist

Required Elements

- ☑ Schematic of acceptable quality, correct memory map, SPLD .PLD file
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board
- ☑ NVRAM (as EPROM substitute), decode logic, and LED functional
- ☑ Understands device programmer.
- ☑ Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM. Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display.
- ☑ Shows and discusses logic analyzer screen captures:
- ☑ Assembly program and timer ISR functional: _____ 09/25/14

                                                  TA signature and date

Supplemental Elements (Qualifies ECEN 5613 students for higher grade.)

- ☑ 74LS374 debug port functional
- ☐ Understands timing analysis, setup/hold/propagation   _____ 9/27/2014

                                                  TA signature and date

Instructor/TA Comments: ☐ ☐ ☐

FOR INSTRUCTOR USE ONLY **Required Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑	☐	☐
Hardware physical implementation	☐	☐	☑	☐	☐
Required Elements functionality	☐	☐	☐	☐	☐
Sign-off done without excessive retries			☑		
Student understanding and skills	☐	☐	☑	☐	☐
Overall Demo Quality (Required Elements)	☐	☐	☑	☐	☐

FOR INSTRUCTOR USE ONLY **Supplemental Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑	☐	☐
Hardware physical implementation	☐	☐	☑	☐	☐
Supplemental Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries			☑		
Student understanding and skills	☐	☐	☑	☐	☐
Overall Demo Quality (Supplemental)	☐	☐	☐	☐	☐

Schematics - Update Document info & no sheet

NOTE: This signoff sheet should be the top/first sheet of your submission.

→ SoS implementation
→ Include Propagation delay in submission