Computer Systems and Programming, Spring 2021 Assignment 6

Understanding Cache Memories

Assigned: Wednesday, May 12, 2021

Due: Monday, May 26, 11:59PM

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1 Logistics

This is an individual project. You must run this assignment on a 64-bit x86-64 machine. You are highly recommended to use Linuxpool to complete this assignment.

2 Overview

This lab will help you understand the impact that cache memories can have on the performance of your C programs.

In this lab assignment, you will write a small C program (about 200-300 lines) that simulates the behavior of a cache memory.

3 Downloading the assignment

Start by copying cachelab-handout.zip to a protected Linux directory in which you plan to do your work. Then give the command

```
linux> unzip cachelab-handout.zip
```

This will create a directory called cachelab-handout that contains a number of files. You will be modifying only csim.c.

To compile this files, type:

```
linux> make clean
linux> make
```

4 Description

For this lab, you will implement a cache simulator.

4.1 Reference Trace Files

The traces subdirectory of the handout directory contains a collection of *reference trace files* that we will use to evaluate the correctness of the cache simulator you write in Part A. The trace files are generated by a Linux program called valgrind. For example, typing

```
linux> valgrind --log-fd=1 --tool=lackey -v --trace-mem=yes ls -l
```

on the command line runs the executable program "ls -1", captures a trace of each of its memory accesses in the order they occur, and prints them on stdout.

Valgrind memory traces have the following form:

```
I 0400d7d4,8
M 0421c7f0,4
L 04f6b868,8
S 7ff0005c8,8
```

Each line denotes one or two memory accesses. The format of each line is

```
[space]operation address, size
```

The *operation* field denotes the type of memory access: "I" denotes an instruction load, "L" a data load, "S" a data store, and "M" a data modify (i.e., a data load followed by a data store). There is never a space before each "I". There is always a space before each "M", "L", and "S". The *address* field specifies a 64-bit hexadecimal memory address. The *size* field specifies the number of bytes accessed by the operation.

4.2 Writing a Cache Simulator

You will write a cache simulator in csim.c that takes a valgrind memory trace as input, simulates the hit/miss behavior of a cache memory on this trace, and outputs the total number of hits, misses, and evictions.

We have provided you with the binary executable of a *reference cache simulator*, called <code>csim-ref</code>, that simulates the behavior of a cache with arbitrary size and associativity on a <code>valgrind</code> trace file. It uses the LRU (least-recently used) replacement policy when choosing which cache line to evict.

The reference simulator takes the following command-line arguments:

```
Usage: ./csim-ref[-hv] -s < s > -E < E > -b < b > -t < tracefile >
```

• -h: Optional help flag that prints usage info

- -v: Optional verbose flag that displays trace info
- -s <s>: Number of set index bits $(S = 2^s)$ is the number of sets)
- -E <E>: Associativity (number of lines per set)
- -b

b>: Number of block bits ($B = 2^b$ is the block size)
- -t <tracefile>: Name of the valgrind trace to replay

The command-line arguments are based on the notation (s, E, and b) from page 597 of the CS:APP2e textbook. For example:

```
linux> ./csim-ref -s 4 -E 1 -b 4 -t traces/yi.trace
hits:4 misses:5 evictions:3
```

The same example in verbose mode:

```
linux> ./csim-ref -v -s 4 -E 1 -b 4 -t traces/yi.trace
L 10,1 miss
M 20,1 miss hit
L 22,1 hit
S 18,1 hit
L 110,1 miss eviction
L 210,1 miss eviction
M 12,1 miss eviction hit
hits:4 misses:5 evictions:3
```

Your job is to fill in the csim.c file so that it takes the same command line arguments and produces the identical output as the reference simulator. Notice that this file is almost completely empty. You'll need to write it from scratch.

Programming Rules

- Include your name in the header comment for csim.c.
- Your csim.c file must compile without warnings in order to receive credit.
- Your simulator must work correctly for arbitrary s, E, and b. This means that you will need to allocate storage for your simulator's data structures using the malloc function. Type "man malloc" for information about this function.
- For this lab, we are interested only in data cache performance, so your simulator should ignore all instruction cache accesses (lines starting with "I"). Recall that valgrind always puts "I" in the first column (with no preceding space), and "M", "L", and "S" in the second column (with a preceding space). This may help you parse the trace.

• To receive credit you must call the function printSummary, with the total number of hits, misses, and evictions, at the end of your main function:

```
printSummary(hit_count, miss_count, eviction_count);
```

• For this this lab, you should assume that memory accesses are aligned properly, such that a single memory access never crosses block boundaries. By making this assumption, you can ignore the request sizes in the valgrind traces.

5 Evaluation

This section describes how your work will be evaluated. The full score for this lab is 33 points:

• Simulator: 27 Points

• Style: 6 Points

The final score will be out 100 points. It will be the full score multiplied by 3.

5.1 Evaluation

For evaluation, we will run your cache simulator using different cache parameters and traces. There are eight test cases, each worth 3 points, except for the last case, which is worth 6 points:

```
linux> ./csim -s 1 -E 1 -b 1 -t traces/yi2.trace
linux> ./csim -s 4 -E 2 -b 4 -t traces/yi.trace
linux> ./csim -s 2 -E 1 -b 4 -t traces/dave.trace
linux> ./csim -s 2 -E 1 -b 3 -t traces/trans.trace
linux> ./csim -s 2 -E 2 -b 3 -t traces/trans.trace
linux> ./csim -s 2 -E 4 -b 3 -t traces/trans.trace
linux> ./csim -s 5 -E 1 -b 5 -t traces/trans.trace
linux> ./csim -s 5 -E 1 -b 5 -t traces/long.trace
```

You can use the reference simulator csim-ref to obtain the correct answer for each of these test cases. During debugging, use the -v option for a detailed record of each hit and miss.

For each test case, outputting the correct number of cache hits, misses and evictions will give you full credit for that test case. Each of your reported number of hits, misses and evictions is worth 1/3 of the credit for that test case. That is, if a particular test case is worth 3 points, and your simulator outputs the correct number of hits and misses, but reports the wrong number of evictions, then you will earn 2 points.

5.2 Evaluation for Style

There are 6 points for coding style. These will be assigned manually by the course staff. Style guidelines can be found on the course website.

6 Working on the Lab

We have provided you with an autograding program, called test-csim, that tests the correctness of your cache simulator on the reference traces. Be sure to compile your simulator before running the test:

linux> make								
linux> ./test-csim								
			Your si	mulator	Reference simulator			
Points	(s, E, b)	Hits	Misses	Evicts	Hits	Misses	Evicts	
3	(1, 1, 1)	9	8	6	9	8	6	traces/yi2.trace
3	(4, 2, 4)	4	5	2	4	5	2	traces/yi.trace
3	(2, 1, 4)	2	3	1	2	3	1	traces/dave.trace
3	(2,1,3)	167	71	67	167	71	67	traces/trans.trace
3	(2, 2, 3)	201	37	29	201	37	29	traces/trans.trace
3	(2, 4, 3)	212	26	10	212	26	10	traces/trans.trace
3	(5, 1, 5)	231	7	0	231	7	0	traces/trans.trace
6	(5, 1, 5)	265189	21775	21743	265189	21775	21743	traces/long.trace
27								

For each test, it shows the number of points you earned, the cache parameters, the input trace file, and a comparison of the results from your simulator and the reference simulator.

Here are some hints and suggestions for working on Part A:

- Do your initial debugging on the small traces, such as traces/dave.trace.
- The reference simulator takes an optional -v argument that enables verbose output, displaying the hits, misses, and evictions that occur as a result of each memory access. You are not required to implement this feature in your csim.c code, but we strongly recommend that you do so. It will help you debug by allowing you to directly compare the behavior of your simulator with the reference simulator on the reference trace files.
- We recommend that you use the getopt function to parse your command line arguments. You'll need the following header files:

```
#include <getopt.h>
#include <stdlib.h>
#include <unistd.h>
```

See "man 3 getopt" for details.

• Each data load (L) or store (S) operation can cause at most one cache miss. The data modify operation (M) is treated as a load followed by a store to the same address. Thus, an M operation can result in two cache hits, or a miss and a hit plus a possible eviction.

6.1 Putting it all Together

We have provided you with a *driver program*, called ./driver.py, that performs a complete evaluation of your simulator and transpose code. This is the same program your instructor uses to evaluate your

handins. The driver uses test-csim to evaluate your simulator. Then it prints a summary of your results and the points you have earned.

To run the driver, type:

```
linux> ./driver.py
```

Each time you type make in the cachelab-handout directory, the Makefile creates a tarball, called userid-handin.tar, that contains your current csim.c. Please upload this tarball on the blackboard.

IMPORTANT: Do not create the handin tarball on a Windows or Mac machine, and do not handin files in any other archive format, such as .zip, .gzip, or .tgz files.

7 Oral Assessment

Important Note: We use automated plagiarism detection to compare your assignment submission with others and also the code repositories on GitHub and similar sites. Moreover, we plan to ask randomly selected 10 % of students to explain their code verbally after the assignments are graded. And one may lose full credit if he or she fails from this oral part.

8 Late Submission Policy

- You may use up to 7 grace days (in total) over the course of the semester for the assignments. That is you can submit your solutions without any penalty if you have free grace days left.
- Any additional unapproved late submission will be punished (1 day late: 20% off, 2 days late: 40% off) and no submission after 2 days will be accepted.

9 Coding Style Evaluation

We have reserved 7 points for a subjective evaluation of the style of your solutions and your commenting. Your solutions should be as clean and straightforward as possible. Your comments should be informative, but they need not be extensive.

10 Academic Integrity

All work on assignments must be done individually unless stated otherwise. You are encouraged to discuss with your classmates about the given assignments, but these discussions should be carried out in an abstract way. That is, discussions related to a particular solution to a specific problem (either in actual code or in the pseudocode) will not be tolerated. In short, turning in someone else's work, in whole or in part, as your own will be considered as a violation of academic integrity. Please note that the former condition also holds for the material found on the web as everything on the web has been written by someone else. See

11 Acknowledgement

This assignment is adapted from CMU Introduction to Computer Systems (ICS) assignment.