Notes:
1) Each BPM has 4 identical DDC channels (antennas A, B, C, D). Each BPM FPGA process 2 BPMs, what gives a total of 16 identical DDC channels
2) All components belongs to the same clock domain (ADC clock)
3) Since all DDC channels must have identical filters, multi-channel filter implementation (8 or 16 channels) can be considered
4) All components must be reconfigurable during runtime via Local bus (AXI-Lite or Wishbone, to be defined)

adc_rate: ADC data rate (ADC clock)
tbt_rate: turn-by-turn data rate (beam revolution frequency)
fofb_rate: fast orbit feedback data rate
monit_rate: monitoring data rate

SIRIUS
adc_rate = ~117.5 MHz
tbt_rate = adc_rate/188
fofb_rate = tbt_rate/62
monit_rate = fofb_rate/1000