1) Each BPM has 4 identical DDC channels (antennas A, B, C, D). Each BPM FPGA process 2 BPMs, what gives a total of 16 identical DDC channels 2) All components belongs to the same clock domain (ADC clock)
3) Since all DDC channels must have identical filters, multi-channel filter implementation (8 or 16 channels) can be considered
4) All components must be reconfigurable during runtime via Local bus (AXI-Lite or Wishbone, to be defined)

adc_rate = ~117.5 MHz tbt_rate = adc_rate/188 fofb_rate = tbt_rate/62 monit_rate = fofb_rate/1000 adc_rate: ADC data rate (ADC clock)
tbt_rate: Intru-by-tun data rate (beam revolution frequency)
fbf_rate: fast orbit feedback data rate
monit_rate: monitoring data rate

SIRIUS

monit_amb @monit_rate x 4 @monit_rate x 2 @monit_rate HB FIR (PFIR) HB FIR (CFIR) CIC (Decimator) fofb_amp @fofb_rate Polyphase FIR (Decimator) @tbt_rate (rect to polar) CORDIC @tbt_rate HB FIR HB FIR (PFIR) (PFIR) @tbt_rate x 2 HB FIR (CFIR) HB FIR (CFIR) @tbt_rate x 4 CIC (Decimator) CIC (Decimator) SFDR > 100 dB -sin (NCO) @adc_rate SOO lata ►IR (BPF)