**Guidelines for VHDL coding**

This document describes the guidelines for VHDL coding in the context of the Beam Position Monitor project for the new Brazilian synchrotron light source, Sirius, developed by the Beam Diagnostics Group (DIG) at the Brazilian Synchrotron Light Laboratory (LNLS/CNPEM).

It is largely based on the Open Hardware Repository’s guidelines for VHDL coding [1], with some modifications listed below:

1. Signals don’t have prefix ***s\_***
2. Signals that represent counters receive the suffix ***\_cnt***
3. Generics are prefixed with ***g\_*** but its names are typed in ***lowercase***
4. The standard header is showed in fig. Illustration.

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-- Title :

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-- Author :

-- Company : CNPEM LNLS-DIG

-- Platform : FPGA-generic

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-- Description:

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-- Revisions :

-- Date Version Author Description

-- yyyy-dd-mm 1.0

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Figure 1: VHDL files header text

**Others White Rabbit Project's Suggestions [**2**]**

* If the module interface comprises multiple repetitive signals, use structures instead of flattened std\_logic ports. This makes the interconnections between the modules much easier to understand and less error prone. For compatibility with Verilog and gate-level simulations, you should provide a module with flattened ports. Names of modules with structs in ports are prefixed with x, fig. Illustration for example.
* Do not type signals, names and keywords in UPPERCASE.
* For every Wishbone module, implement a generic g\_interface\_mode, allowing the user to choose between Classic and Pipelined (B4) bus operation.
* Use Emacs-style formatting VHDL formatting rules (2-space indentation) and file header.

**Figure** 2**: Names of modules with structs in ports**

**References**

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| [1] | P. Loschmidt *et al*, "Guidelines for VHDL coding", <http://www.ohwr.org/projects/hdl-core-lib/documents>, 2010. |

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| [2] | T. Wlostowski; G. Daniluk, "Development instructions", <http://www.ohwr.org/projects/wr-cores/wiki/Development_Instructions>, 2012. |