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1. Verification requirement document

Label	Description	Stimulus Generation	Functional Coverage	Functionality Check
ALSU_1	Incase of invalid cases do not occur, when opcode is ADD, then out should perform the addition on ports A and B taking cin if parameter FULL_ADDER is high	Randomization under constraints on A and B to have the maximum, minimum and zero values most of the time	Included as coverpoint for A and B. Included with cross coverage when ALU opcode is addition with cin taking 0 or 1	Output checked against golden model
ALSU_2	Incase of invalid cases do not occur, when opcode is MULT, then out should perform the multiplication on ports A and B	Randomization under constraints on A and B to have the maximum, minimum and zero values most of the time	Included in coverpoint for A and B. Included with cross coverage when ALU opcode is multiplication	Output checked against golden model
ALSU_3	Incase of invalid cases do not occur, when opcode is OR or XOR, then out should perform bitwise operation on ports A and B. incase of red_op inputs are high, then out should be the reduction operation on port A or B based on the prioirty if the both red_op ports are high.	Randomization under constraints on A and B, incase of red_op_A is high, constrain A to have one bit high most of the time and B to be zero. incase of red_op_B is high, constrain B to have one bit high most of the time and A to be zero.	Included in coverpoint for A and B. Included with cross coverage when ALU opcode is OR or XOR.	Output checked against golden model
ALSU_4	When invalid cases exist (opcode is 110/111 or red_op inputs are high when opcode isn't OR/XOR), out should be low and leds should blink	Randomization under constraints where invalid cases do not occur as frequent as valid cases	Included in a coverpoint for opcode. Included with cross coverage to make sure invalid cases occur	Output checked against golden model
ALSU_5	If invalid cases do not occur and the bypass inputs are high, then the output out should by bypass port A or B based on the prioirty if the both bypass ports are high	Randomization for bypass_A and bypass_B inputs.	Included in a coverpoint for bypass	Output checked against golden model
ALSU_6	Incase of invalid cases do not occur, when opcode is SHIFT, then out should be shifted left or right with adding "serial_in" input based on "direction" input is high or low respectively.	Randomization for direction and serial_in inputs with no constraints on both of them and on ports A and B.	Included in a coverpoint for opcode. Included in cross coverage with serial_in and direction taking 0 or 1	Output checked against golden model
ALSU_7	Incase of invalid cases do not occur, when opcode is ROTATE, then out should be rotated left or right based on "direction" input is high or low respectively.	Randomization for direction input with no constraints on it and on ports A and B.	Included in a coverpoint for opcode. Included in cross coverage with direction taking 0 or 1	Output checked against golden model
ALSU_8	When the asynchronous reset is asserted, then out and leds output should be low.	Randomization for rst input to be asserted with a low probability.	not included	Output Checked against golden model

2. Code Coverage Report

```
================================================================================
=== Instance: /ALSU_tb/dut
=== Design Unit: work.ALSU
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        28        27         1    100%

================================Branch Details================================

Branch Coverage for instance /ALSU_tb/dut

    Line         Item                      Count     Source
```

```
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      46        46         0   100.00%

================================Statement Details================================

Statement Coverage for instance /ALSU_tb/dut --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
```

```
Expression Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Expressions                      8         8         0   100.00%

================================Expression Details================================

Expression Coverage for instance /ALSU_tb/dut --

  File ALSU.sv
----------------Focused Expression View-----------------
Line       24 Item    1  ((red_op_A_reg | red_op_B_reg) & (opcode_reg[1] | opcode_reg[2]))
Expression totals: 4 of 4 input terms covered = 100.00%
```

```
Condition Coverage:
    Enabled Coverage              Bins    Covered    Misses  Coverage
    ----------------              ----       ----    ------  --------
    Conditions                       6          6         0   100.00%

================================Condition Details================================

Condition Coverage for instance /ALSU_tb/dut --

  File ALSU.sv
----------------Focused Condition View-------------------
Line       60 Item    1  (bypass_A_reg && bypass_B_reg)
Condition totals: 2 of 2 input terms covered = 100.00%
```

```
Toggle Coverage:
    Enabled Coverage             Bins      Hits    Misses  Coverage
    ----------------             ----      ----    ------  --------
    Toggles                       118       118         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /ALSU_tb/dut --
```

```
DIRECTIVE COVERAGE:
--------------------------------------------------------------------------------------------
Name                                    Design Design   Lang File(Line)      Hits Status
                                        Unit   UnitType
--------------------------------------------------------------------------------------------
/ALSU_tb/check_result/leds_check_cover  ALSU_tb Verilog  SVA  ALSU_tb.sv(201) 69499 Covered
/ALSU_tb/check_result/out_check_cover   ALSU_tb Verilog  SVA  ALSU_tb.sv(203) 69499 Covered
/ALSU_tb/Async_reset_cover              ALSU_tb Verilog  SVA  ALSU_tb.sv(211)  482 Covered

TOTAL DIRECTIVE COVERAGE: 100.00%  COVERS: 3

ASSERTION RESULTS:
---------------------------------------------------------------------
Name                File(Line)                   Failure      Pass
                                                 Count        Count
---------------------------------------------------------------------
/ALSU_tb/#ublk#102282978#43/immed__44
                    ALSU_tb.sv(44)                     0          1
/ALSU_tb/#ublk#102282978#65/immed__67
                    ALSU_tb.sv(67)                     0          1
/ALSU_tb/#anonblk#102282978#86#4#/#ublk#102282978#86/immed__87
                    ALSU_tb.sv(87)                     0          1
/ALSU_tb/check_result/leds_check_assert
                    ALSU_tb.sv(200)                    0          1
/ALSU_tb/check_result/out_check_assert
                    ALSU_tb.sv(202)                    0          1
/ALSU_tb/Async_reset_assert
                    ALSU_tb.sv(210)                    0          1

Total Coverage By Instance (filtered view): 100%
```

-

3. Functional Coverage Report

Covergroup Coverage:						
Covergroups	1	na	na	100.00%		
Coverpoints/Crosses	17	na	na	na		
Covergroup Bins	31	31	0	100.00%		

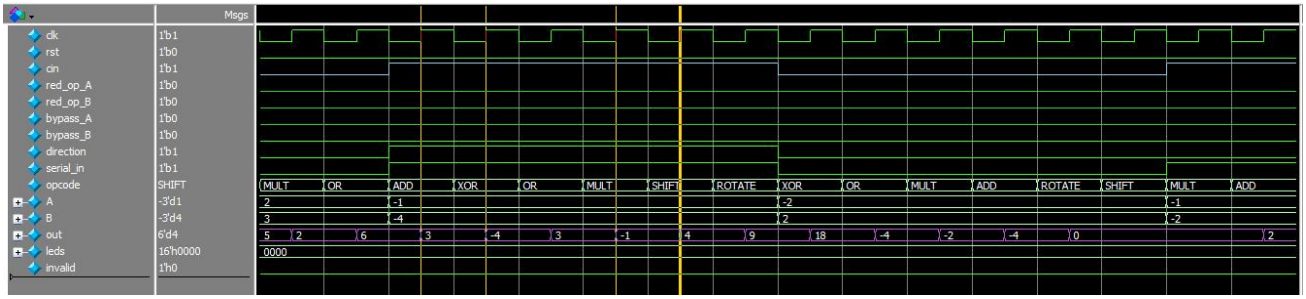
Covergroup	Metric	Goal	Bins	Status
Coverpoint A_cp	100.00%	100	-	Covered
covered/total bins:	3	3	-	
missing/total bins:	0	3	-	
% Hit:	100.00%	100	-	
bin A_data_0	8990	1	-	Covered
bin A_data_max	9067	1	-	Covered
bin A_data_min	8963	1	-	Covered
default bin A_data_default	41540		-	Occurred
Coverpoint A_walkingones_cp	100.00%	100	-	Covered
covered/total bins:	3	3	-	
missing/total bins:	0	3	-	
% Hit:	100.00%	100	-	
bin A_data_walkingones[-4]	726	1	-	Covered
bin A_data_walkingones[1]	487	1	-	Covered
bin A_data_walkingones[2]	477	1	-	Covered
Coverpoint B_cp	100.00%	100	-	Covered
covered/total bins:	3	3	-	
missing/total bins:	0	3	-	
% Hit:	100.00%	100	-	
bin B_data_0	9559	1	-	Covered
bin B_data_max	9154	1	-	Covered
bin B_data_min	9057	1	-	Covered
default bin B_data_default	40790		-	Occurred
Coverpoint B_walkingones_cp	100.00%	100	-	Covered
covered/total bins:	3	3	-	
missing/total bins:	0	3	-	
% Hit:	100.00%	100	-	
bin B_data_walkingones[-4]	361	1	-	Covered
bin B_data_walkingones[1]	208	1	-	Covered
bin B_data_walkingones[2]	207	1	-	Covered

Coverpoint ALU_cp	100.00%	100	-	Covered
covered/total bins:	7	7	-	
missing/total bins:	0	7	-	
% Hit:	100.00%	100	-	
illegal_bin Bins_invalid	15976		-	Occurred
bin Bins_shift[SHIFT]	9080	1	-	Covered
bin Bins_shift[ROTATE]	8310	1	-	Covered
bin Bins_arith[ADD]	8817	1	-	Covered
bin Bins_arith[MULT]	8953	1	-	Covered
bin Bins_bitwise[OR]	8932	1	-	Covered
bin Bins_bitwise[XOR]	8492	1	-	Covered
bin Bins_trans	1	1	-	Covered
Coverpoint cin_cp [1]	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
bin cin0_1	68560	1	-	Covered
Coverpoint serial_in_cp [1]	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
bin serial_in0_1	68560	1	-	Covered
Coverpoint direction_cp [1]	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
bin direction0_1	68560	1	-	Covered
Coverpoint red_op_A_cp [1]	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
bin red_op_A_high	3619	1	-	Covered

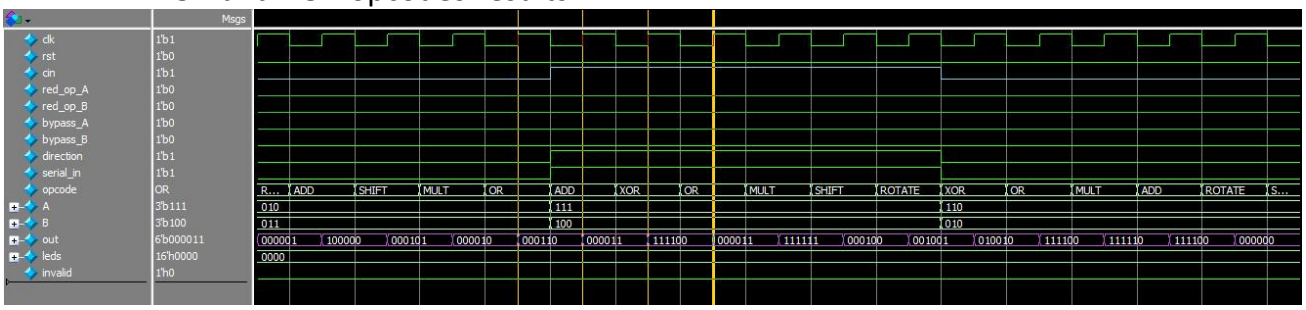
Coverpoint red_op_B_cp [1]	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
bin red_op_B_high	3605	1	-	Covered
Cross arith_corner_cases_cross	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin arith_corner_cases	3492	1	-	Covered
Cross ADD_cin_cross	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin ADD_cin0_1	8817	1	-	Covered
Cross SHIFT_serial_in_cross	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin SHIFT_serial_in0_1	9080	1	-	Covered
Cross SHIFT_direction_cross	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin SHIFT_ROTATE_direction0_1	17390	1	-	Covered
Cross bitwise_red_op_A_cross	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin bitwise_A_pattern	584	1	-	Covered
Cross bitwise_red_op_B_cross	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin bitwise_B_pattern	247	1	-	Covered
Cross Invalid_case_cross	100.00%	100	-	Covered
covered/total bins:	1	1	-	
missing/total bins:	0	1	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin invalid_case	1277	1	-	Covered

4. Waveforms

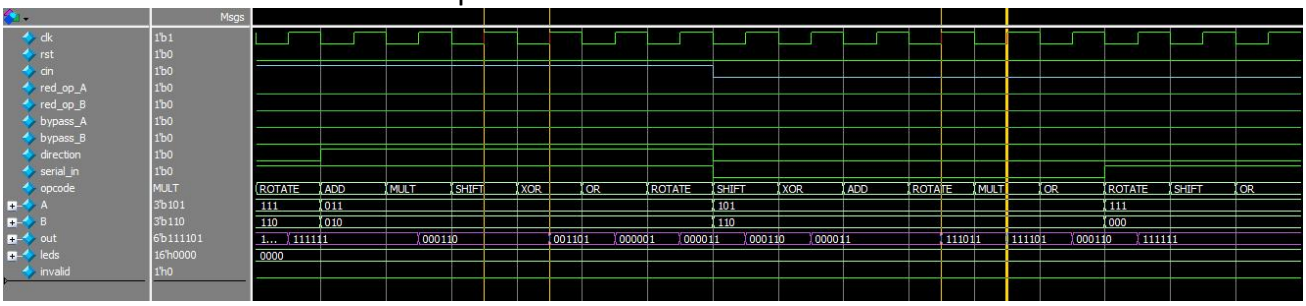
- ✓ ADD and MULT opcodes results



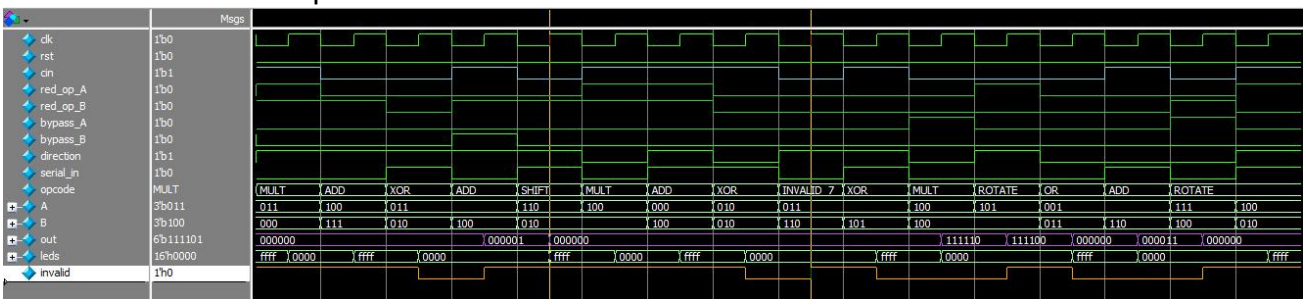
- ✓ OR and XOR opcodes results



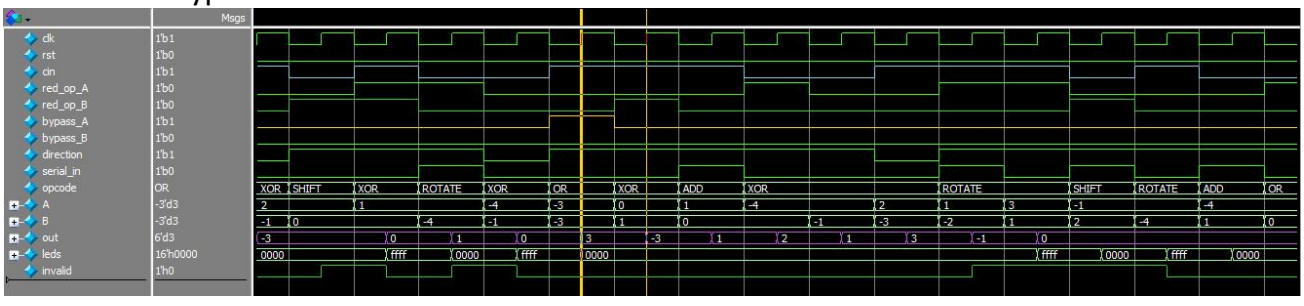
- ✓ SHIFT and ROTATE opcodes results



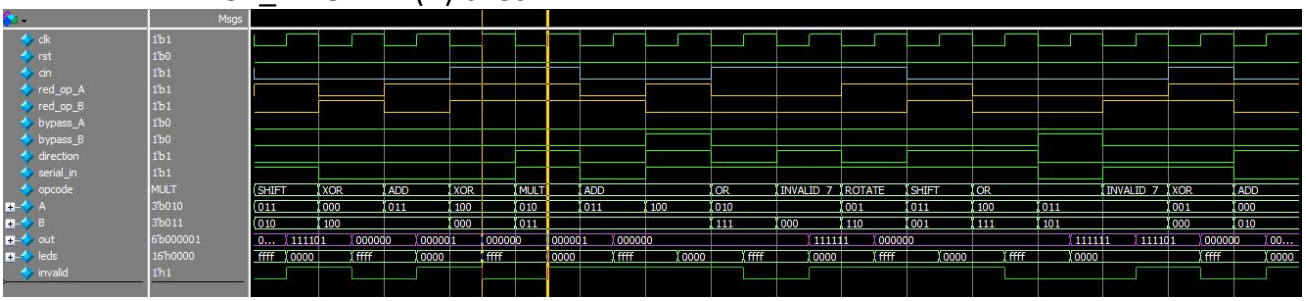
- ✓ INVALID opcode results



- ✓ bypass A result



✓ INPUT_PRIORITY (A) check



✓ Constraint no. 8 (array of valid unique opcodes)