1. APB Master

AMBA APB Ports:

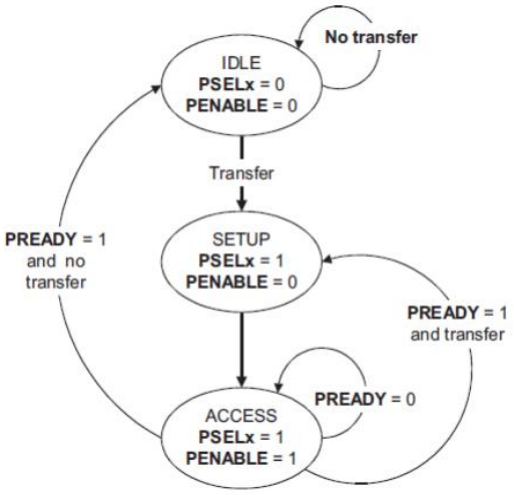
Signal	Source	Description
PCLK	Clock source	Clock. The rising edge of **PCLK** times all transfers on the APB.
PRESETn	System bus equivalent	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PADDR	APB bridge	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PPROT	APB bridge	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
PSELx	APB bridge	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a **PSELx** signal for each slave.
PENABLE	APB bridge	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	APB bridge	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PWDATA	APB bridge	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when **PWRITE** is HIGH. This bus can be up to 32 bits wide.
PSTRB	APB bridge	Write strobes. This signal indicates which byte lanes to update during a write transfer. There is one write strobe for each eight bits of the write data bus. Therefore, **PSTRB[n]** corresponds to **PWDATA[(8n + 7):(8n)]**. Write strobes must not be active during a read transfer.
PREADY	Slave interface	Ready. The slave uses this signal to extend an APB transfer.
PRDATA	Slave interface	Read Data. The selected slave drives this bus during read cycles when **PWRITE** is LOW. This bus can be up to 32-bits wide.
PSLVERR	Slave interface	This signal indicates a transfer failure. APB peripherals are not required to support the **PSLVERR** pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.

Additional Ports:

Port	Size	Direction	Function
READ_WRITE	1-bit	Input	When High, read operation When low, write operation
apb_write_paddr	9-bit		[7:0]: Write address, [8]: select the slave (if 0, select slave1, if 1, select slave2)
apb_write_data	8-bit		Write data
apb_read_paddr	9-bit		[7:0]: Read address, [8]: select the slave (if 0, select slave1, if 1, select slave2)
apb_read_data_out	8-bit	Output	Read data

APB Operation: 3 states

- IDLE
- SETUP
- ACCESS/ENABLE



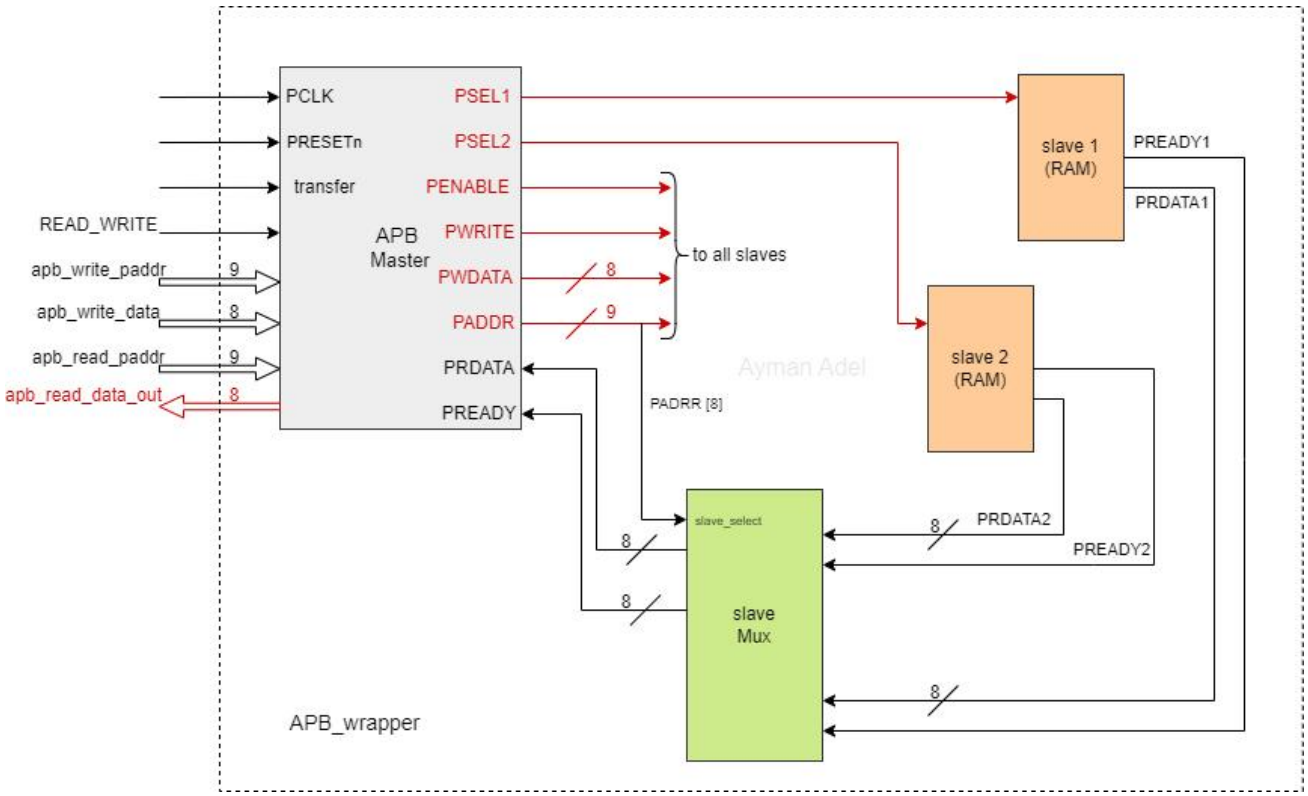
For more information and to understand AMBA APB transfers, refer to the following document, https://www.eecs.umich.edu/courses/eecs373/readings/IHI0024C_amba_apb_protocol_spec.pdf

2. Single-port Synchronous RAM

Ports

Port	Size	Direction	Function
PWDATA	8-bit	Input	Data Input
PCLK	1-bit		Clock signal
PRESETn	1-bit		Active low asynchronous reset
PADDR	8-bit		Address line
PSEL	1-bit		Select of the RAM
PENABLE	1-bit		Enable of the RAM
PWRITE	1-bit		When High, write operation to RAM When low, read operation from RAM
PRDATA	8-bit	Output	Data Output
PREADY	1-bit		Asserts when the data is valid on PRDATA

3. Design Wrapper (APB Master + 2 Slaves/RAMs)



Slave Mux: selects a certain slave outputs (PREADY, PRDATA) depending on slave select input