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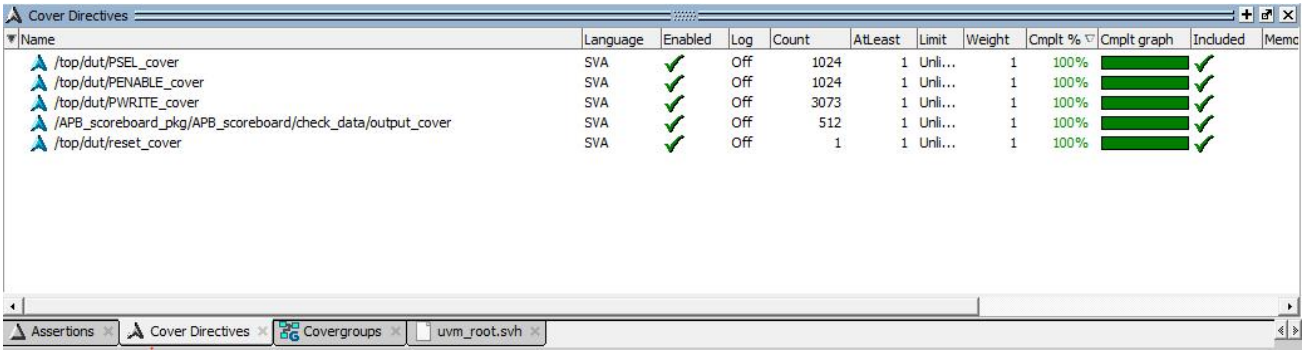
1. Functional coverage Report

Coverpoint WR_address_cp	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
bin wr_addr1	64	1	-	Covered
bin wr_addr2	64	1	-	Covered
bin wr_addr3	64	1	-	Covered
bin wr_addr4	64	1	-	Covered
bin wr_addr5	64	1	-	Covered
bin wr_addr6	64	1	-	Covered
bin wr_addr7	64	1	-	Covered
bin wr_addr8	64	1	-	Covered
Coverpoint RD_address_cp	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
bin rd_addr1	64	1	-	Covered
bin rd_addr2	64	1	-	Covered
bin rd_addr3	64	1	-	Covered
bin rd_addr4	64	1	-	Covered
bin rd_addr5	64	1	-	Covered
bin rd_addr6	64	1	-	Covered
bin rd_addr7	64	1	-	Covered
bin rd_addr8	64	1	-	Covered
Coverpoint data_patterns_cp	100.00%	100	-	Covered
covered/total bins:	3	3	-	
missing/total bins:	0	3	-	
% Hit:	100.00%	100	-	
bin all_ones	21	1	-	Covered
bin all_zeros	22	1	-	Covered
bin alternating_bits	48	1	-	Covered
default bin random	421		-	Occurred
Coverpoint write_slave_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin slave1	256	1	-	Covered
bin slave2	256	1	-	Covered
Coverpoint read_slave_cp	100.00%	100	-	Covered
covered/total bins:	2	2	-	
missing/total bins:	0	2	-	
% Hit:	100.00%	100	-	
bin slave1	256	1	-	Covered
bin slave2	256	1	-	Covered

2. Assertions Report

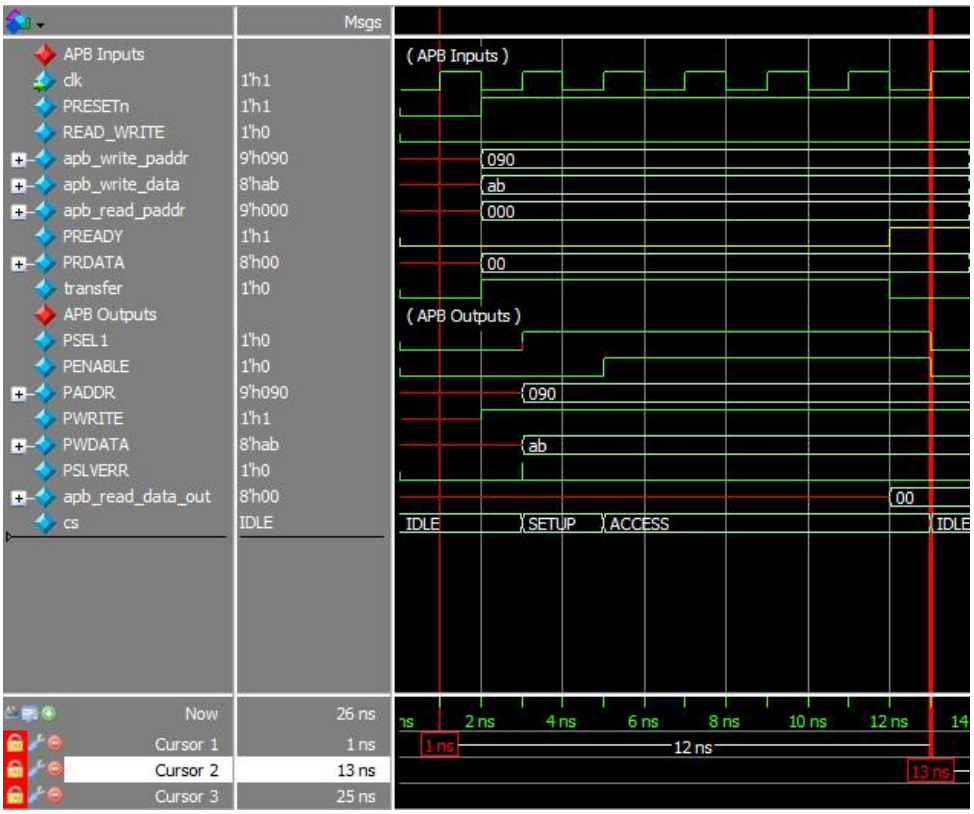
```
ASSERTION RESULTS:
---------------------------------------------------------------------
Name                File(Line)                    Failure      Pass
                                                  Count        Count
---------------------------------------------------------------------
/top/dut/reset_assert
                    U:/AYMAN/DIGITAL/1.Verification/Final Course Projects/APB_with_slave/APB_wrapper.sv(60)
                                                  0            1
/top/dut/PSEL_assert U:/AYMAN/DIGITAL/1.Verification/Final Course Projects/APB_with_slave/APB_wrapper.sv(66)
                                                  0            1
/top/dut/PENABLE_assert
                    U:/AYMAN/DIGITAL/1.Verification/Final Course Projects/APB_with_slave/APB_wrapper.sv(70)
                                                  0            1
/top/dut/PWRITE_assert
                    U:/AYMAN/DIGITAL/1.Verification/Final Course Projects/APB_with_slave/APB_wrapper.sv(74)
                                                  0            1
/APB_read_sequence_pkg/APB_read_sequence/body/#anonblk#175054199#22#4#/#ublk#175054199#22/immed__24
                    U:/AYMAN/DIGITAL/1.Verification/Final Course Projects/APB_with_slave/APB_read_sequence.sv(24)
                                                  0            1
/APB_write_sequence_pkg/APB_write_sequence/body/#anonblk#82609287#22#4#/#ublk#82609287#22/immed__24
                    U:/AYMAN/DIGITAL/1.Verification/Final Course Projects/APB_with_slave/APB_write_sequence.sv(24)
                                                  0            1
/APB_scoreboard_pkg/APB_scoreboard/check_data/output_assert
                    U:/AYMAN/DIGITAL/1.Verification/Final Course Projects/APB_with_slave/APB_scoreboard.sv(72)
                                                  0            1

Total Coverage By Instance (filtered view): 100.00%
```



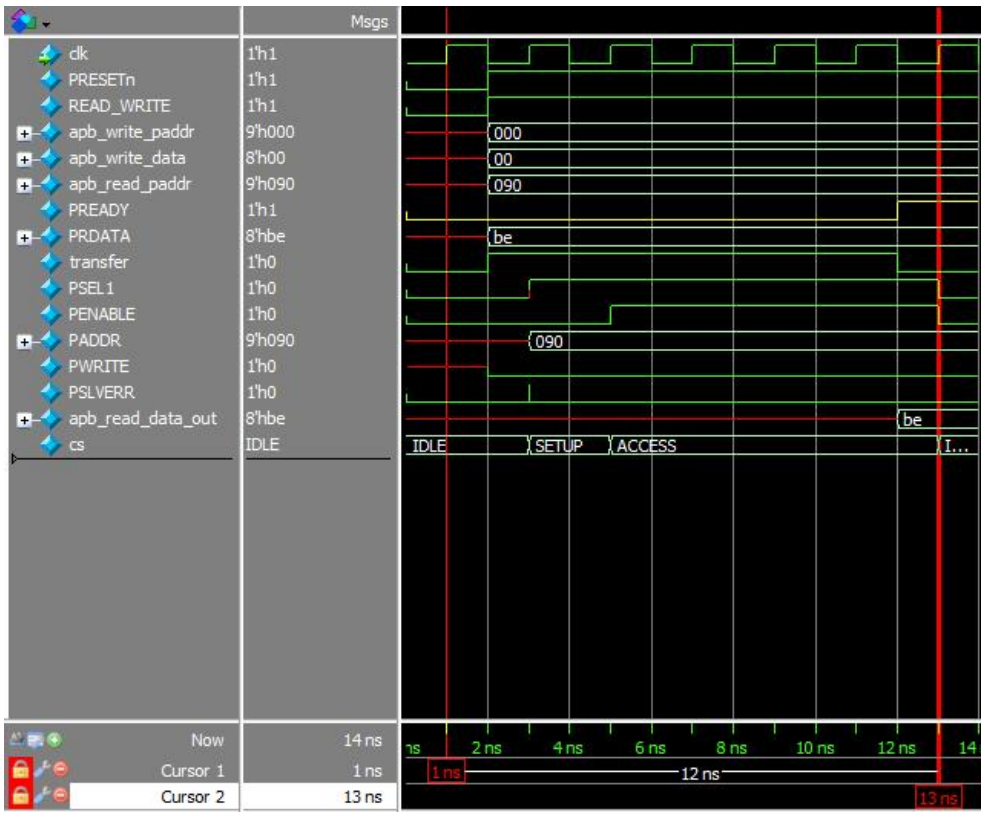
3. Wave forms

APB without Slaves/RAMs:

1. Write with wait states

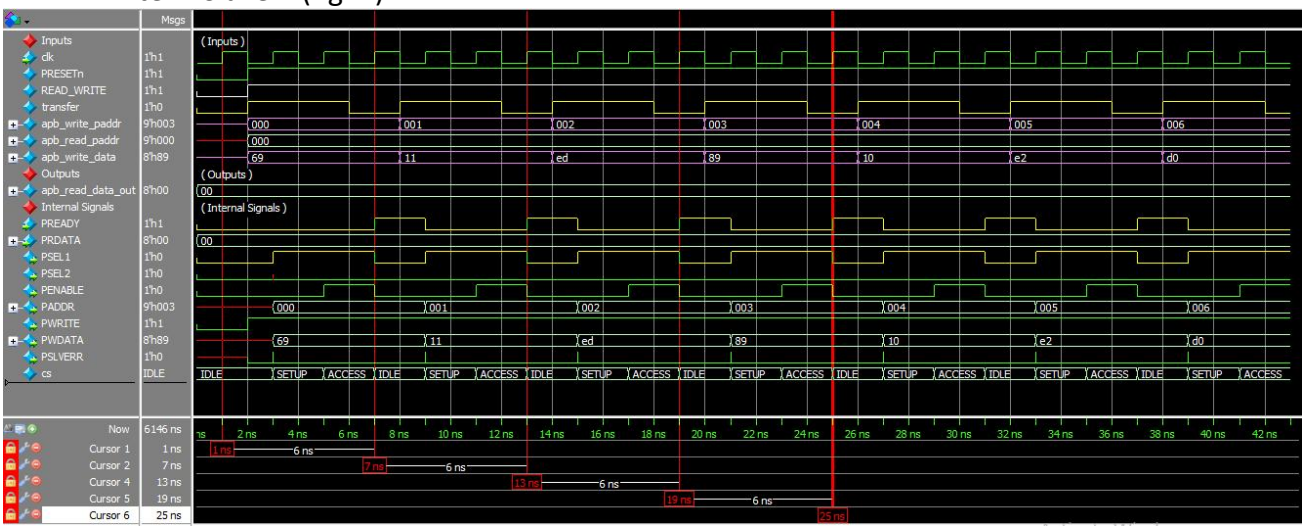


2. Read with wait states

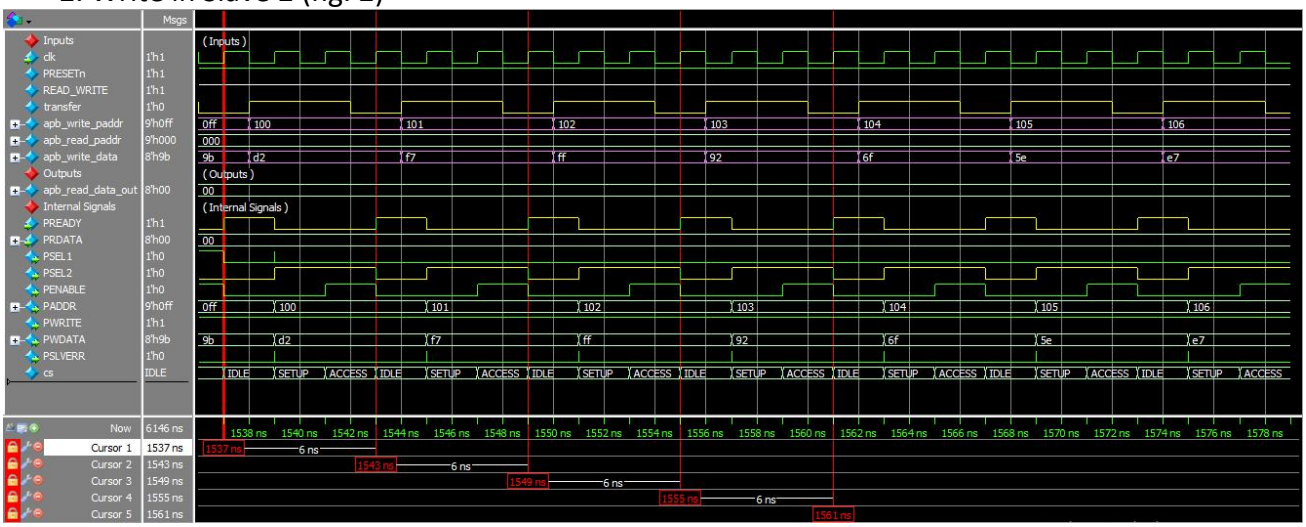


APB with Slaves/RAMs (with no wait states):

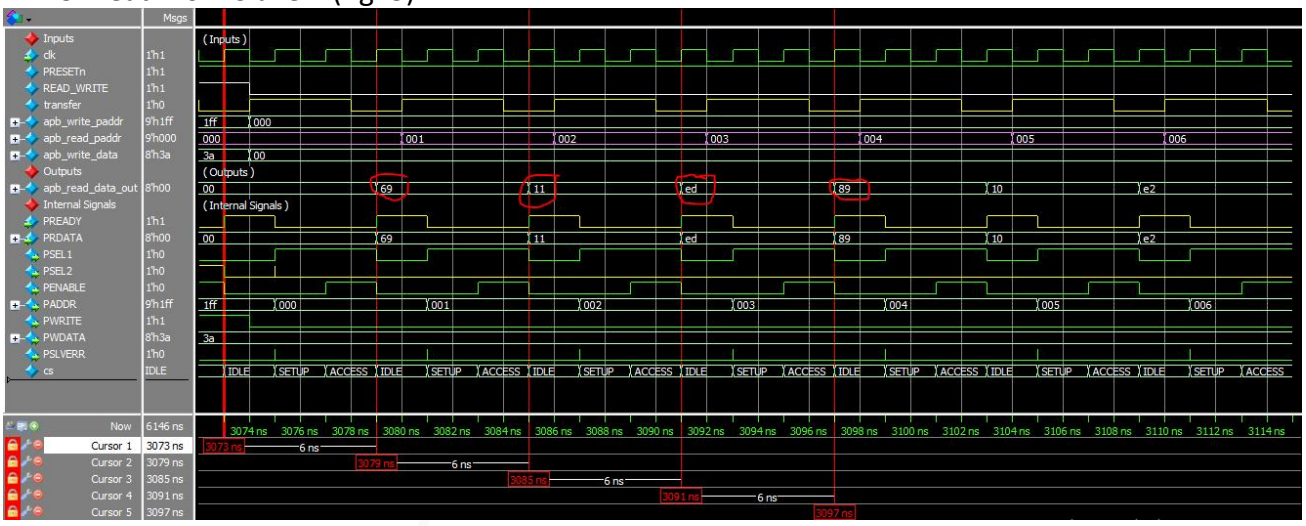
1. Write in Slave 1 (fig. 1)



2. Write in Slave 2 (fig. 2)

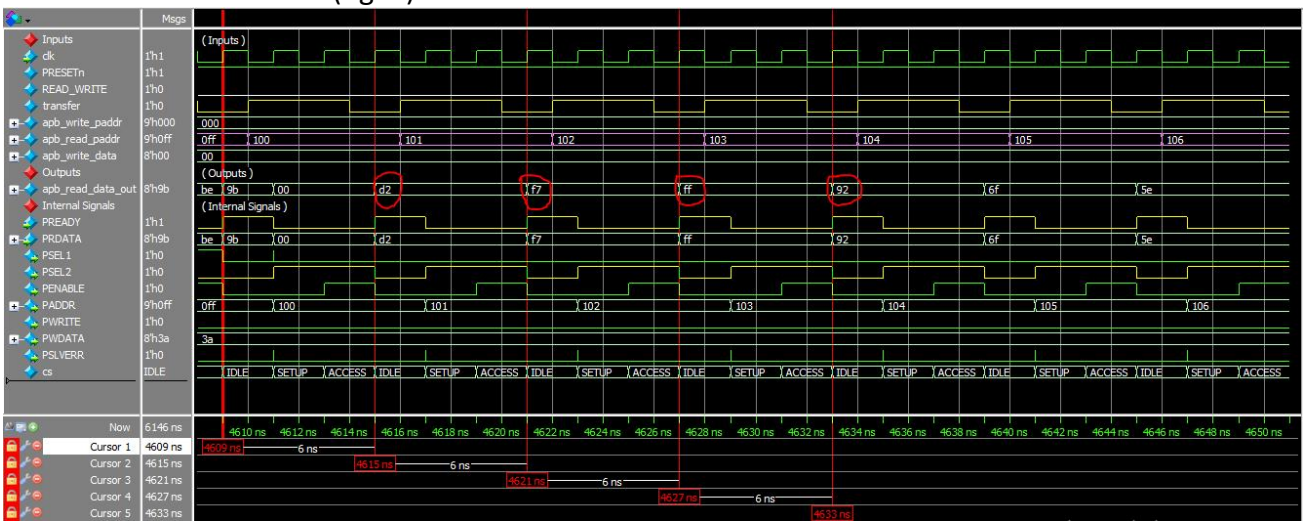


3. Read from Slave 1 (fig. 3)



✓ Correct, compared to the data written in RAM 1 as we see in fig. 1.

4. Read from Slave 2 (fig. 4)



✓ Correct, compared to the data written in RAM 2 as we see in fig. 2.

4. QuestaSim transcript

```
# UVM_INFO U                                    /APB_with_slave/APB_scoreboard.sv(49) @ 6146: uvm_test_top.env.sb [report_phase] At time 6146: Simulation Ends and Error Count
= 0, Correct Count= 512
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :   15
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [Questa UVM]     2
# [RNTST]     1
# [TEST_DONE]     1
# [report_phase]     1
# [run_phase]    10
# ** Note: $finish    : C:/questasim64_2021.1/win64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 6146 ns  Iteration: 61  Instance: /top
# 1
# Break in Task uvm_pkg/uvm_root::run_test at C:/questasim64_2021.1/win64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh line 430
```