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1. Verification Plan

- Check for reset
- Write only sequence and make the FIFO full
- Read only sequence and make the FIFO empty
- Consecutive write and read
- Simultaneous write and read

2. Verification Requirement document

Label	Description	Stimulus Generation	Functional Coverage	Functionality Check
FIFO_1	empty should not be HIGH if write enable is HIGH	Randomization on wr_en under constraint that write occurs more than read	Included as cross cover for wr_en and empty.	Output checked against golden model and also with assertion
FIFO_2	full should not be HIGH if read enable is HIGH	Randomization on rd_en under constraint that write occurs more than read	Included as cross cover for rd_en and full	Output checked against golden model and also with assertion
FIFO_3	overflow should not be HIGH if write enable is LOW	Randomization on wr_en under constraint that write occurs more than read	Included as cross cover for wr_en and overflow	Output checked against golden model and also with assertion
FIFO_4	underflow should not be HIGH if read enable is LOW	Randomization on rd_en under constraint that write occurs more than read	Included as cross cover for rd_en and underflow	Output checked against golden model and also with assertion
FIFO_5	write ack should not be HIGH if write enable is LOW	Randomization on wr_en under constraint that write occurs more than read	Included as cross cover for wr_en and wr_ack	Output checked against golden model and also with assertion
FIFO_6	in case of both read enable and write enable are HIGH and the FIFO is full then only read occurs	Randomization on wr_en and rd_en under constraint that write occurs more than read	Included as cross cover for wr_en and rd_en and all the output flags	Output checked against golden model and also with assertion
FIFO_7	in case of both read enable and write enable are HIGH and the FIFO is empty then only write occurs	Randomization on wr_en and rd_en under constraint that write occurs more than read	Included as cross cover for wr_en and rd_en and all the output flags	Output checked against golden model and also with assertion
FIFO_8	in case of both read enable and write enable are HIGH and the FIFO is not full or empty then both write and read occur	Randomization on wr_en and rd_en under constraint that write occurs more than read	Included as cross cover for wr_en and rd_en and all the output flags	Output Checked against golden model and also with assertion
FIFO_9	if the reset is asserted then the output flags will be LOW	Randomization on rst_n under constraint that reset is deasserted most of the time	not included	Output Checked against golden model

3. Code coverage Report

```
================================================================================
=== Instance: /top/dut
=== Design Unit: work.FIFO
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        27        27         0   100.00%

================================Branch Details================================
```

```
Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      20        18         2    90.00%

================================Condition Details================================
```

```
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      34        34         0   100.00%

================================Statement Details================================

Statement Coverage for instance /top/dut --
```

```
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                        106       106         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /top/dut --
```

4. Functional coverage Report

Not 100% but it's logical because there are cases that shouldn't happen.

Cross W_R_with_wr_ack_cross	75.00%	100	-	Uncovered
covered/total bins:	6	8	-	
missing/total bins:	2	8	-	
% Hit:	75.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	1260	1	-	Covered
bin <auto[1],auto[0],auto[1]>	2905	1	-	Covered
bin <auto[1],auto[1],auto[0]>	852	1	-	Covered
bin <auto[0],auto[1],auto[0]>	941	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1941	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2118	1	-	Covered
bin <auto[0],*,auto[1]>	0	1	2	ZERO
Cross W_R_with_overflow_cross	75.00%	100	-	Uncovered
covered/total bins:	6	8	-	
missing/total bins:	2	8	-	
% Hit:	75.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	816	1	-	Covered
bin <auto[1],auto[0],auto[1]>	1830	1	-	Covered
bin <auto[1],auto[1],auto[0]>	1296	1	-	Covered
bin <auto[0],auto[1],auto[0]>	941	1	-	Covered
bin <auto[1],auto[0],auto[0]>	3016	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2118	1	-	Covered
bin <auto[0],*,auto[1]>	0	1	2	ZERO

Cross W_R_with_full_cross	75.00%	100	-	Uncovered
covered/total bins:	6	8	-	
missing/total bins:	2	8	-	
% Hit:	75.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[0],auto[1]>	3092	1	-	Covered
bin <auto[0],auto[0],auto[1]>	813	1	-	Covered
bin <auto[1],auto[1],auto[0]>	2112	1	-	Covered
bin <auto[0],auto[1],auto[0]>	941	1	-	Covered
bin <auto[1],auto[0],auto[0]>	1754	1	-	Covered
bin <auto[0],auto[0],auto[0]>	1305	1	-	Covered
bin <*,auto[1],auto[1]>	0	1	2	ZERO
Cross W_R_with_empty_cross	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	36	1	-	Covered
bin <auto[0],auto[1],auto[1]>	89	1	-	Covered
bin <auto[1],auto[0],auto[1]>	111	1	-	Covered
bin <auto[0],auto[0],auto[1]>	122	1	-	Covered
bin <auto[1],auto[1],auto[0]>	2076	1	-	Covered
bin <auto[0],auto[1],auto[0]>	852	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4735	1	-	Covered
bin <auto[0],auto[0],auto[0]>	1996	1	-	Covered

Cross W_R_with_almostfull_cross	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	1333	1	-	Covered
bin <auto[0],auto[1],auto[1]>	359	1	-	Covered
bin <auto[1],auto[0],auto[1]>	388	1	-	Covered
bin <auto[0],auto[0],auto[1]>	513	1	-	Covered
bin <auto[1],auto[1],auto[0]>	779	1	-	Covered
bin <auto[0],auto[1],auto[0]>	582	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4458	1	-	Covered
bin <auto[0],auto[0],auto[0]>	1605	1	-	Covered
Cross W_R_with_almostempty_cross	100.00%	100	-	Covered
covered/total bins:	8	8	-	
missing/total bins:	0	8	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	177	1	-	Covered
bin <auto[0],auto[1],auto[1]>	39	1	-	Covered
bin <auto[1],auto[0],auto[1]>	163	1	-	Covered
bin <auto[0],auto[0],auto[1]>	99	1	-	Covered
bin <auto[1],auto[1],auto[0]>	1935	1	-	Covered
bin <auto[0],auto[1],auto[0]>	902	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4683	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2019	1	-	Covered

Cross W_R_with_underflow_cross	75.00%	100	-	Uncovered
covered/total bins:	6	8	-	
missing/total bins:	2	8	-	
% Hit:	75.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	73	1	-	Covered
bin <auto[0],auto[1],auto[1]>	42	1	-	Covered
bin <auto[1],auto[1],auto[0]>	2039	1	-	Covered
bin <auto[0],auto[1],auto[0]>	899	1	-	Covered
bin <auto[1],auto[0],auto[0]>	4846	1	-	Covered
bin <auto[0],auto[0],auto[0]>	2118	1	-	Covered
bin <*,auto[0],auto[1]>	0	1	2	ZERO

Cross wr_empty_cross [2]	0.00%	100	-	ZERO
covered/total bins:	0	0	-	
missing/total bins:	0	0	-	
% Hit:	100.00%	100	-	
Illegal and Ignore Bins:				
illegal_bin ill_1	0		-	ZERO
Cross rd_full_cross [2]	0.00%	100	-	ZERO
covered/total bins:	0	0	-	
missing/total bins:	0	0	-	
% Hit:	100.00%	100	-	
Illegal and Ignore Bins:				
illegal_bin ill_2	0		-	ZERO
Cross wr_overflow_cross [2]	0.00%	100	-	ZERO
covered/total bins:	0	0	-	
missing/total bins:	0	0	-	
% Hit:	100.00%	100	-	
Illegal and Ignore Bins:				
illegal_bin ill_3	0		-	ZERO
Cross rd_underflow_cross [2]	0.00%	100	-	ZERO
covered/total bins:	0	0	-	
missing/total bins:	0	0	-	
% Hit:	100.00%	100	-	
Illegal and Ignore Bins:				
illegal_bin ill_4	0		-	ZERO
Cross wr_wr_ack_cross [2]	0.00%	100	-	ZERO
covered/total bins:	0	0	-	
missing/total bins:	0	0	-	
% Hit:	100.00%	100	-	
Illegal and Ignore Bins:				
illegal_bin ill_5	0		-	ZERO

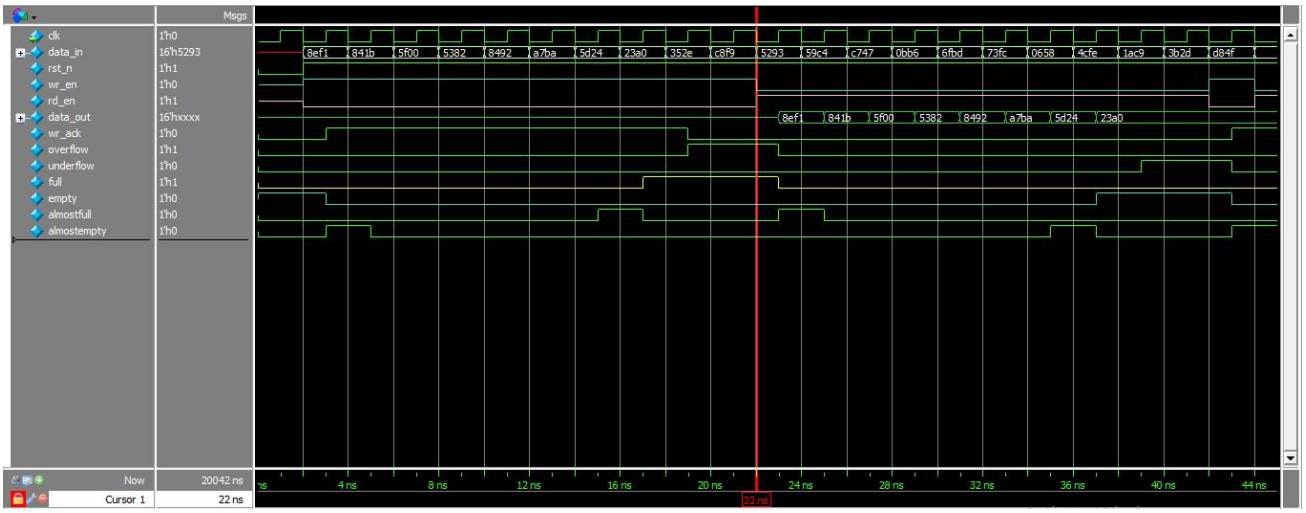
5. Assertions Report

Name	Assertion Type	Language	Enable	Failure Count	Pass Count
/FIFO_scoreboard_pkg::FIFO_scoreboard::check_data/outputs_check_assert	Immediate	SVA	on	0	1
/top/dut/FIFO_sva_inst/full_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/empty_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/almostfull_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/almostempty_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/wr_ack_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/overflow_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/underflow_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/count_up_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/count_down_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/wr_empty_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/rd_full_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/wr_overflow_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/rd_underflow_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/wr_wr_ack_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/almostfull_full_assert	Concurrent	SVA	on	0	1
/top/dut/FIFO_sva_inst/almostempty_empty_assert	Concurrent	SVA	on	0	1

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included
/top/dut/FIFO_sva_inst/full_cover	SVA	✓	Off	4048	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/empty_cover	SVA	✓	Off	524	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/almostfull_cover	SVA	✓	Off	2631	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/almostempty_cover	SVA	✓	Off	441	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/wr_ack_cover	SVA	✓	Off	4030	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/overflow_cover	SVA	✓	Off	2774	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/underflow_cover	SVA	✓	Off	96	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/count_up_cover	SVA	✓	Off	2812	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/count_down_cover	SVA	✓	Off	864	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/wr_empty_cover	SVA	✓	Off	6804	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/rd_full_cover	SVA	✓	Off	3062	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/wr_overflow_cover	SVA	✓	Off	2950	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/rd_underflow_cover	SVA	✓	Off	6957	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/wr_wr_ack_cover	SVA	✓	Off	2950	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/almostfull_full_cover	SVA	✓	Off	1269	1	Unli...	1	100%		✓
/top/dut/FIFO_sva_inst/almostempty_empty_cover	SVA	✓	Off	31	1	Unli...	1	100%		✓
/FIFO_scoreboard_pkg/FIFO_scoreboard/check_data/outputs_check_cover	SVA	✓	Off	10021	1	Unli...	1	100%		✓

6. Wave forms

Write only then Read only:



Simultaneous Write and Read: