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1. Functional coverage Report

```
Covergroup Coverage:
    Covergroups                 1        na        na   100.00%
        Coverpoints/Crosses     3        na        na        na
            Covergroup Bins    19        19         0   100.00%
--------------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

--------------------------------------------------------------------------------------------------------
 TYPE /spi_wrapper_coverage_pkg/spi_wrapper_coverage/cvr_grp
                                                   100.00%        100          -    Covered
    covered/total bins:                                 19         19          -
    missing/total bins:                                  0         19          -
    % Hit:                                         100.00%        100          -
    Coverpoint WR_address_cp                       100.00%        100          -    Covered
        covered/total bins:                              8          8          -
        missing/total bins:                              0          8          -
        % Hit:                                     100.00%        100          -
        bin wr_addr1                                    33          1          -    Covered
        bin wr_addr2                                    32          1          -    Covered
        bin wr_addr3                                    32          1          -    Covered
        bin wr_addr4                                    32          1          -    Covered
        bin wr_addr5                                    32          1          -    Covered
        bin wr_addr6                                    33          1          -    Covered
        bin wr_addr7                                    32          1          -    Covered
        bin wr_addr8                                    32          1          -    Covered
```

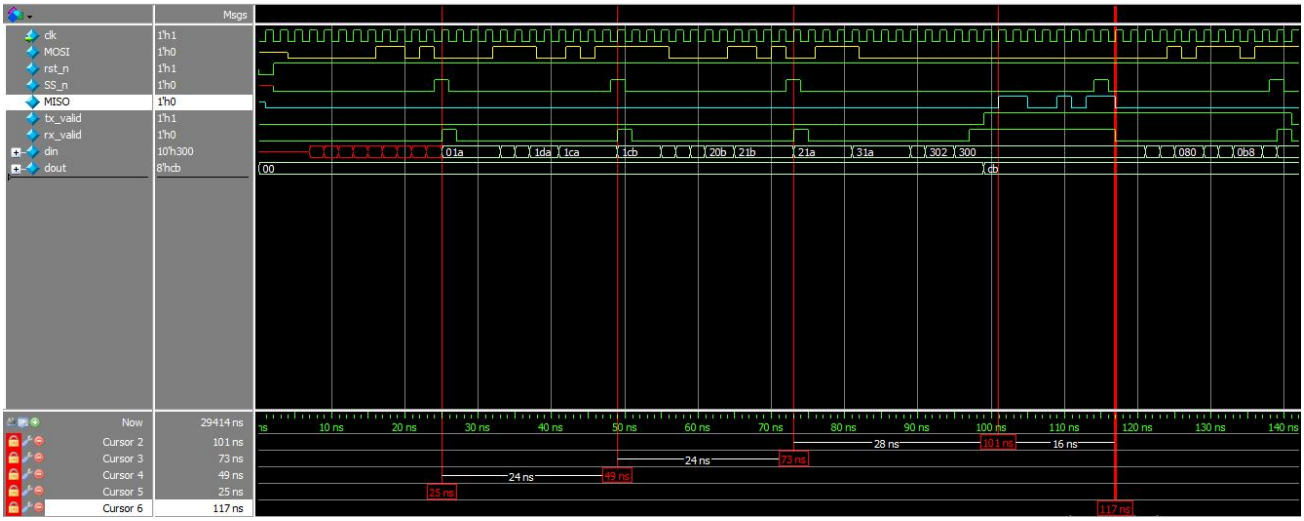
```
Coverpoint RD_address_cp                       100.00%        100          -    Covered
    covered/total bins:                              8          8          -
    missing/total bins:                              0          8          -
    % Hit:                                     100.00%        100          -
    bin rd_addr1                                    33          1          -    Covered
    bin rd_addr2                                    32          1          -    Covered
    bin rd_addr3                                    32          1          -    Covered
    bin rd_addr4                                    32          1          -    Covered
    bin rd_addr5                                    32          1          -    Covered
    bin rd_addr6                                    33          1          -    Covered
    bin rd_addr7                                    32          1          -    Covered
    bin rd_addr8                                    32          1          -    Covered
Coverpoint data_patterns_cp                    100.00%        100          -    Covered
    covered/total bins:                              3          3          -
    missing/total bins:                              0          3          -
    % Hit:                                     100.00%        100          -
    bin all_ones                                     1          1          -    Covered
    bin all_zeros                                    1          1          -    Covered
    bin alternating_bits                             3          1          -    Covered
    default bin random                             253                     -    Occurred
```

2. Assertions Report

Name	Assertion Type	Language	Enable	Failure Count	Pass Count
/uvm_pkg::uvm_reg_map::do_write/#ublk#215181159#1731/immed__1735	Immediate	SVA	on	0	0
/uvm_pkg::uvm_reg_map::do_read/#ublk#215181159#1771/immed__1775	Immediate	SVA	on	0	0
/spi_wrapper_main_sequence_pkg::spi_wrapper_main_sequence::body/immed__24	Immediate	SVA	on	0	1
/spi_wrapper_scoreboard_pkg::spi_wrapper_scoreboard::check_data/outputs_check_assert	Immediate	SVA	on	0	1
/top/dut/rx_valid_assert	Concurrent	SVA	on	0	1
/top/dut/tx_rx_valid_assert	Concurrent	SVA	on	0	1

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	In
/top/dut/rx_valid_cover	SVA	✓	Off	1032	1	Unli...	1	100%		✓
/top/dut/tx_rx_valid_cover	SVA	✓	Off	258	1	Unli...	1	100%		✓
/spi_wrapper_scoreboard_pkg/spi_wrapper_scoreboard/check_data/outputs_check...	SVA	✓	Off	14707	1	Unli...	1	100%		✓

3. Wave form



Here, I want to write data = 0xCB (1100_1011) in address = 0x1A (0001_1010) so,

I. WADD: Write the address (1A)
II. WDATA: Write the data (CB) in the stored address

Then, I want to read that data = 0xCB (1100_1011) from that address = 0x1A (0001_1010) to check,

I. RADD: Write the read address (1A)
II. RDATA: Read the data in that address which should be (CB)

As we see, the MISO output (from 101 to 117 ns) = 1100_1011 (CB) which is correct.

4. QuestaSim transcript

```
# UVM_INFO spi_wrapper_scoreboard.sv(45) @ 29414: uvm_test_top.env.sb [report_phase] At time 29414: Simulation Ends and Error Count= 0, Correct Count= 14707
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :    7
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [Questa UVM]     2
# [RNTST]     1
# [TEST_DONE]     1
# [report_phase]     1
# [run_phase]     2
# ** Note: $finish    : C:/questasim64_2021.1/win64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 29414 ns  Iteration: 61  Instance: /top
```