

CPSC 359 Assignment 2

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1) Problem to Solve:

Create a synchronous sequential logic circuit that implements a 4-bit Gray Code counter.

The 4-bit Gray Code counter counts upward (from 0 to 15) using the following pattern:

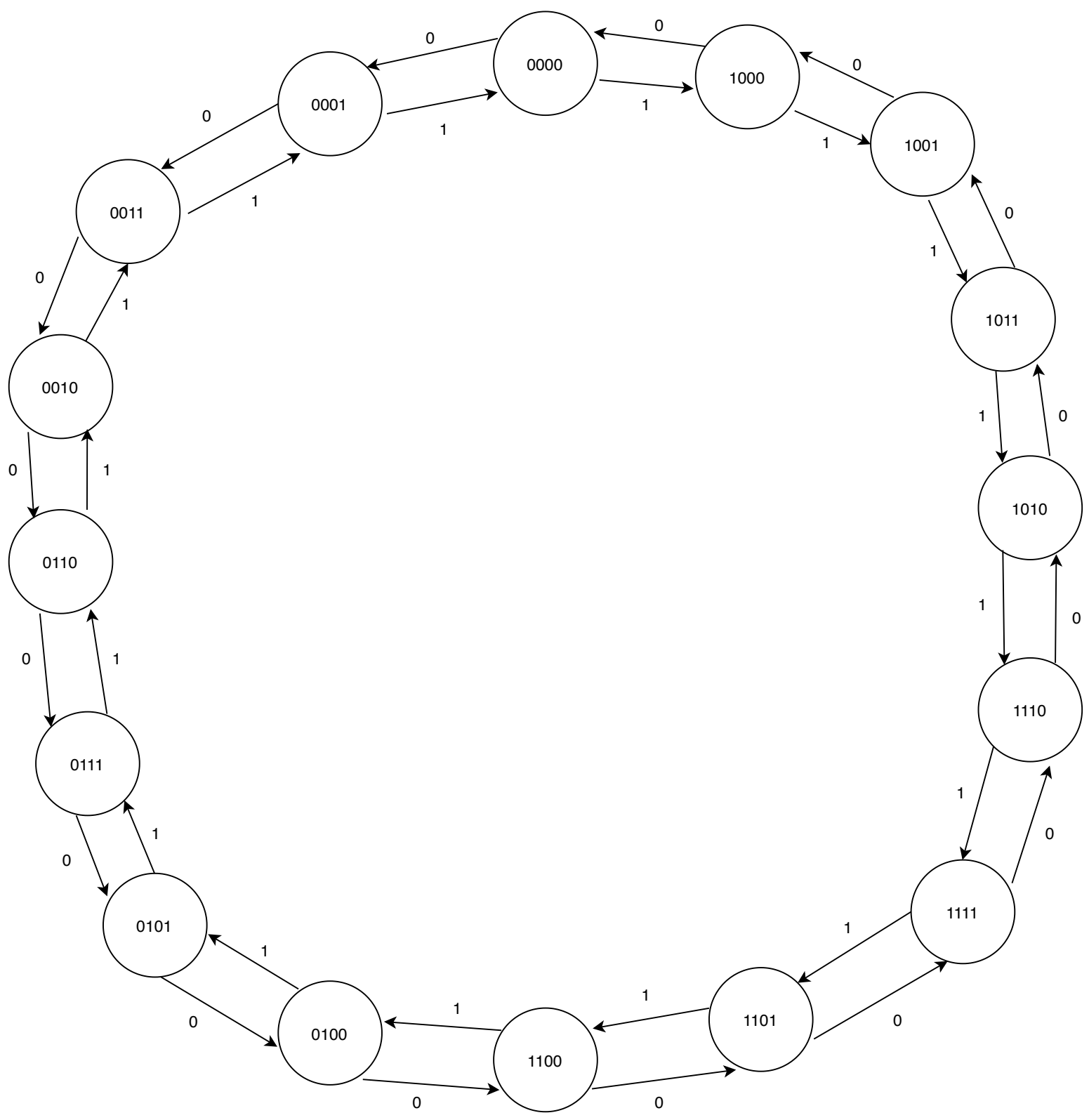
0000, 0001, 0011, 0010, 0110, 0111, 0101, 0100, 110, 1101, 1111, 1110, 1010, 1011, 1001, 1000

Once 1000 (15 in decimal) is reached, the code “wraps around” to 0000 (0 in decimal)

The circuit will have one input called *Direction*: if 0, the counter counts up; if 1, it counter counts down.

The circuit should have 4 outputs, one for each bit in the Gray Code. The design should be implemented using J K flip-flops.

Step 2: Create a state diagram



3) Determine the inputs, outputs, number of flip-flops needed, and their type

We need:

- One input called Direction
- 4 flip-flops (named A, B, C, D) to represent each bit in the 4-bit binary counter
- The flip-flops used will be JK flip-flops
- The outputs of the circuit will be the outputs (ie. states) of the flip-flops.

4) The excitation table for the state machine is on page 4.

5) The circuit output functions, flip-flop input functions and the steps needed to derive them are in pages 5-8.

6) The logic designs of the flip flop outputs are in pages 9-13.