UCI Fall 2022

EECS 119

Project # 2

CMOS Combinational Logic Gate

Prepared by

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Introduction:

In this lab, the circuit representation of a static CMOS and its standard cell layout will be drawn. The standard cell layout is obtained through a logic graph and Euler's algorithm (see parts 2 and 3) [1]. Additionally, the circuit's schematic and layout will be modeled in Cadence.

Theory:

Logic graphs are diagrams where every transistor in a circuit is represented by an "edge" [1]. If a path can be drawn along all the edges without touching one of them twice, then that path (or sequence) has to be tested in the pull-up and pull-down networks (PUN and PDN). If the sequence results in never having to touch any edges twice in both PUN and PDN, then it is guaranteed that the standard cell layout will have an uninterrupted diffusion strip [1]. Using an uninterrupted diffusion strip reduces the number of metal connectors and gate polys that have to be used for transistors in series and in parallel (see below).

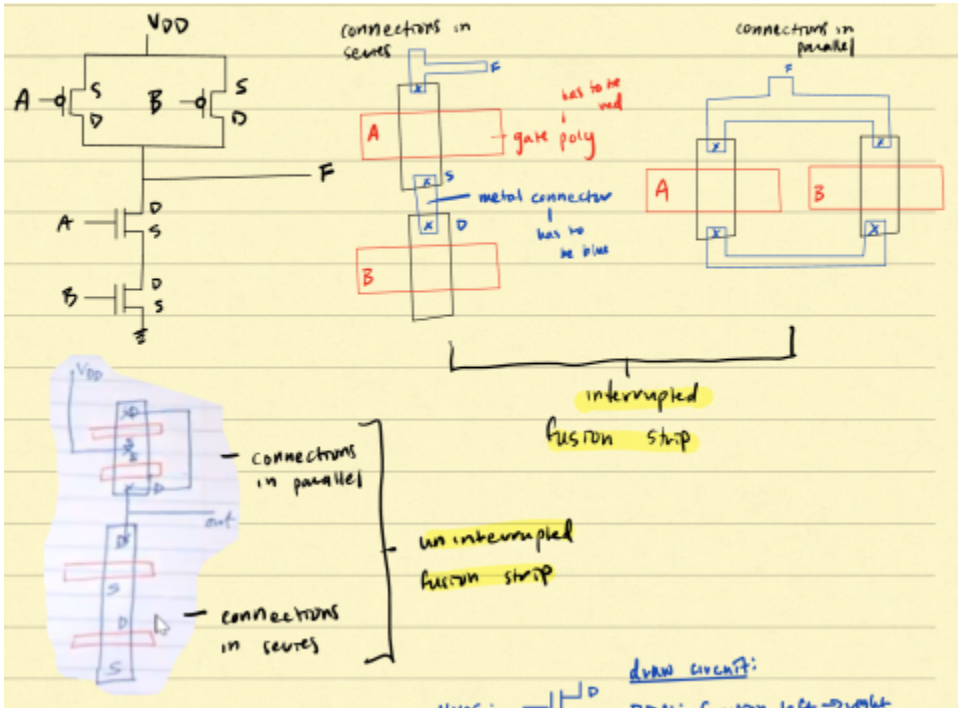

Figure 1: Difference between an interrupted and uninterrupted fusion strip

The general steps for creating the standard cell layout of a circuit is to: draw the circuit, create a logic graph, find an Euler's path that works as described above, and draw all connections for p-diffusion strips and n-diffusion strips (see below).

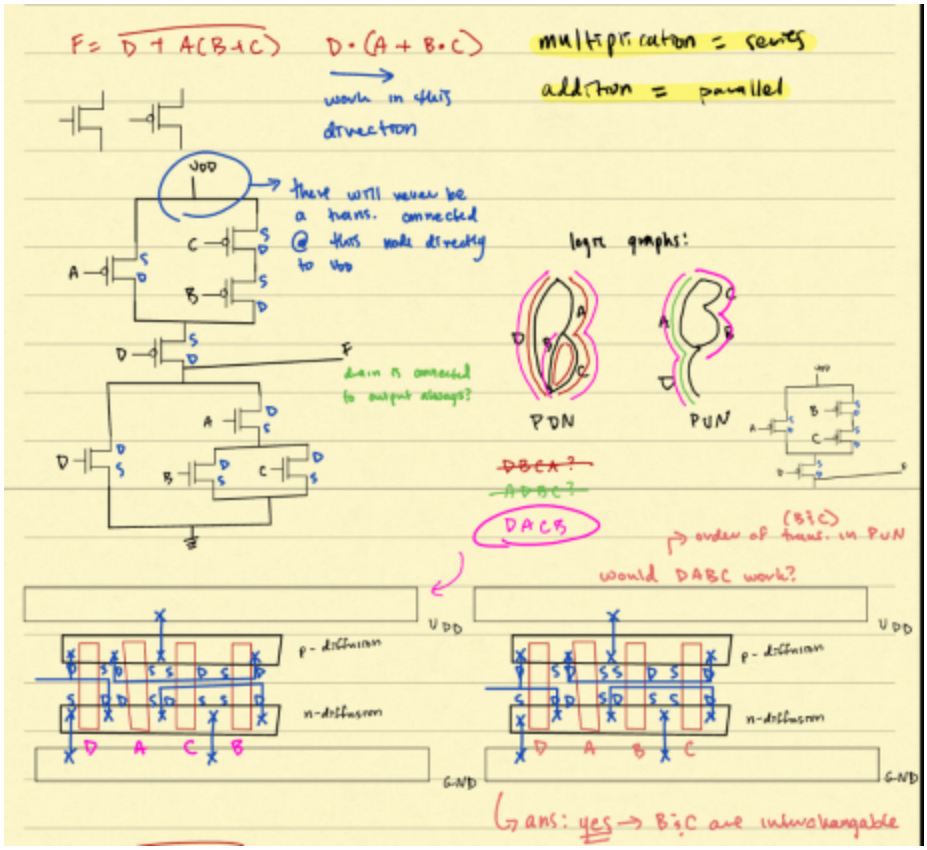

Figure 2: Method for drawing a circuit, finding the correct Euler's path through a logic graph, and constructing the standard cell layout

Design:

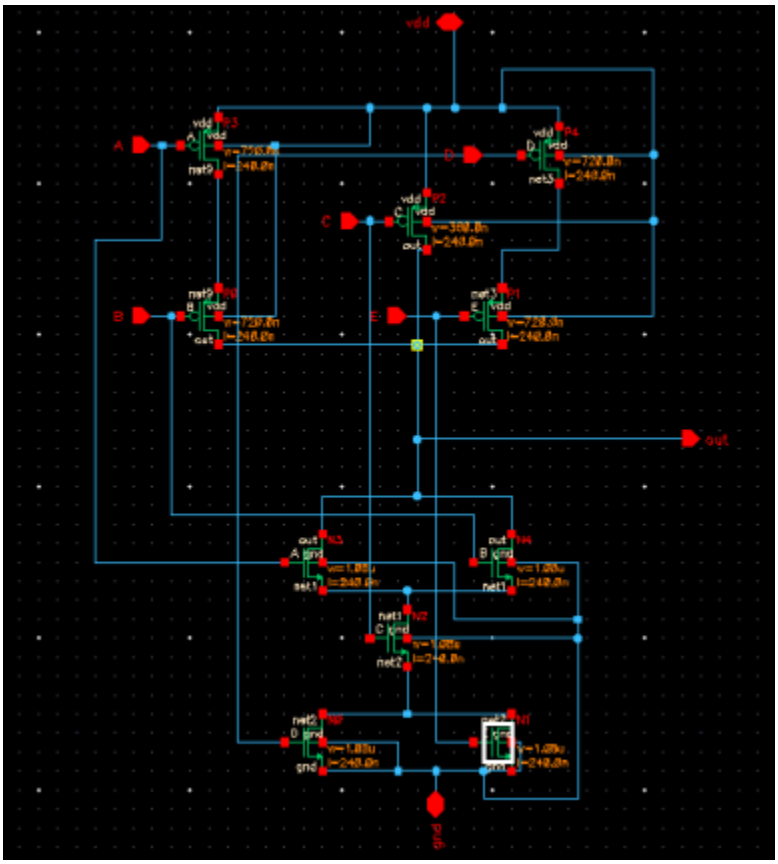

Figure 3: Circuit diagram (schematic)

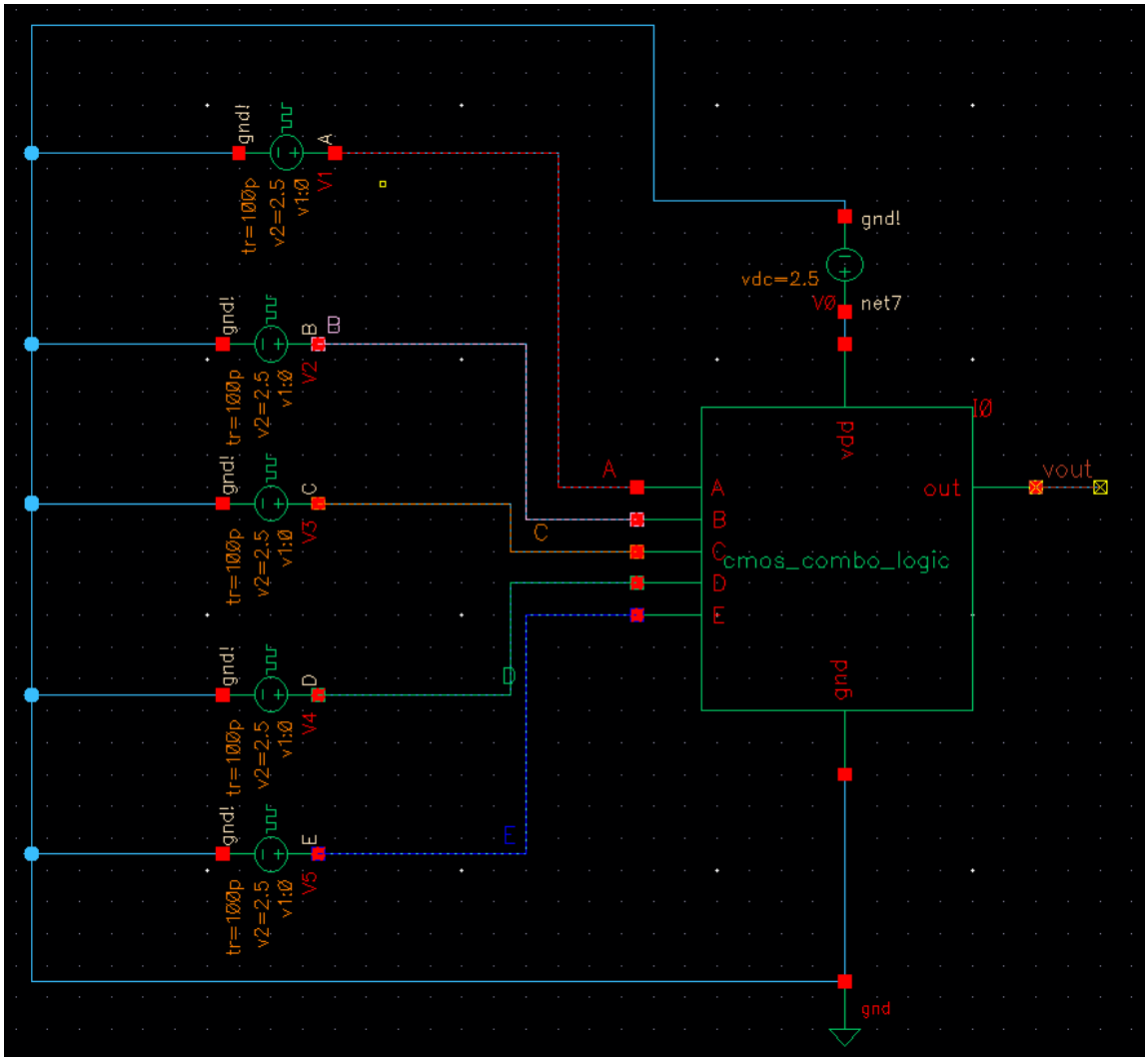

Figure 4: Testbench for the schematic

Results:

Part 1:

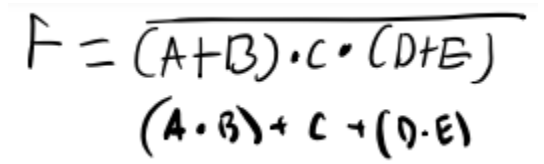

Figure 5: Function being replicated and tested

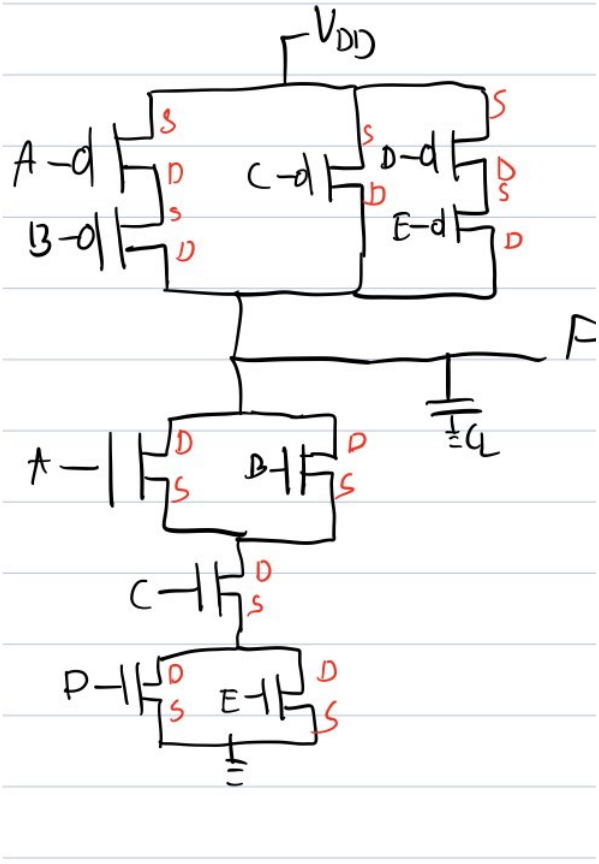

Figure 6: Circuit diagram of above function

Table 1: Calculated truth table for above function

A	B	C	D	E	F (out)
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	0	1	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	0

1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0

Part 2:

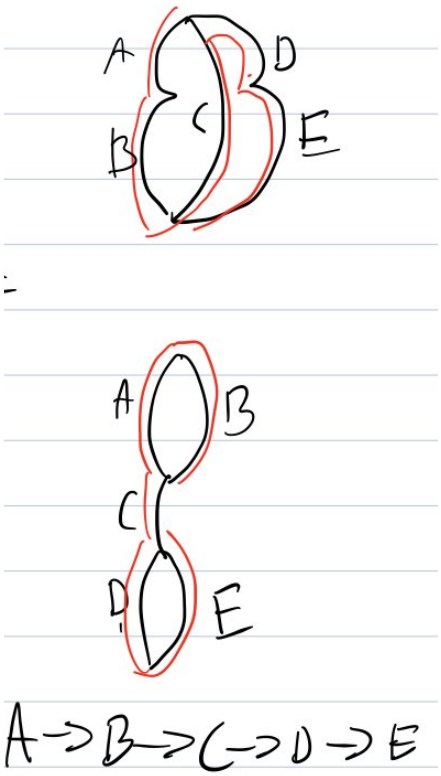

Figure 7: Logic graph and a Euler's path for above function

Part 3:

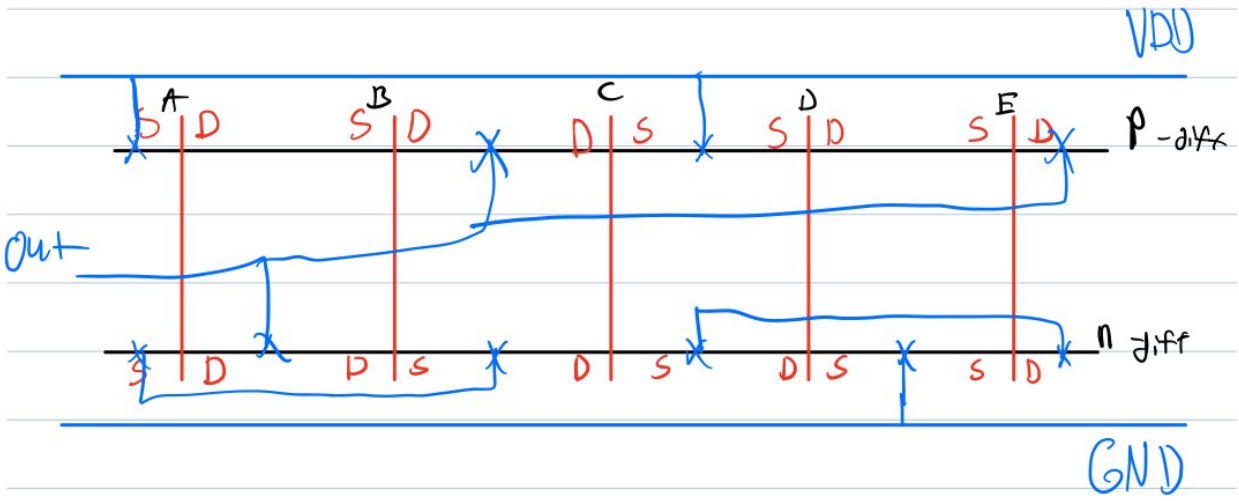

Figure 8: Standard cell layout of above function

Part 4:

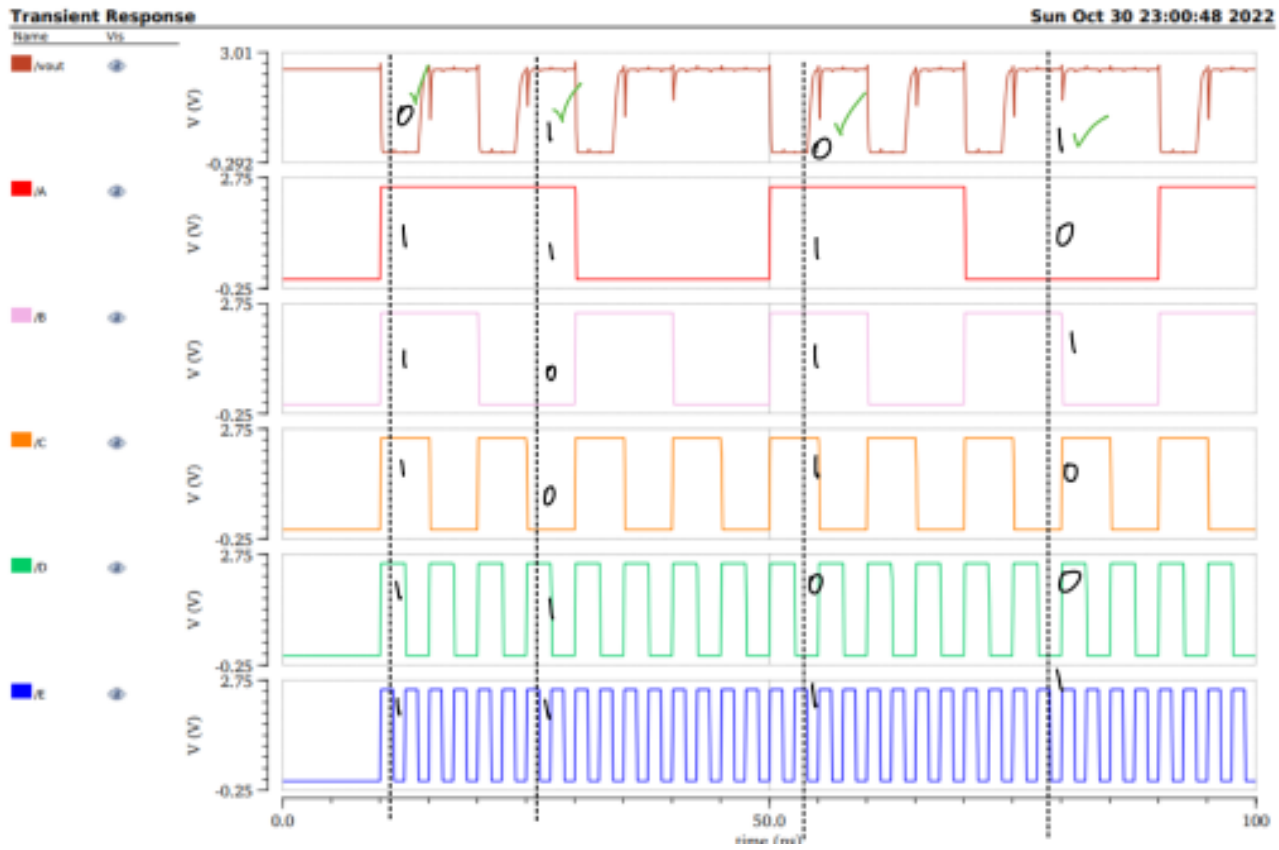

Figure 9: Output waveform of the simulated circuit, lines indicate rows in truth table with their corresponding (correct) outputs as vout

Part 5:

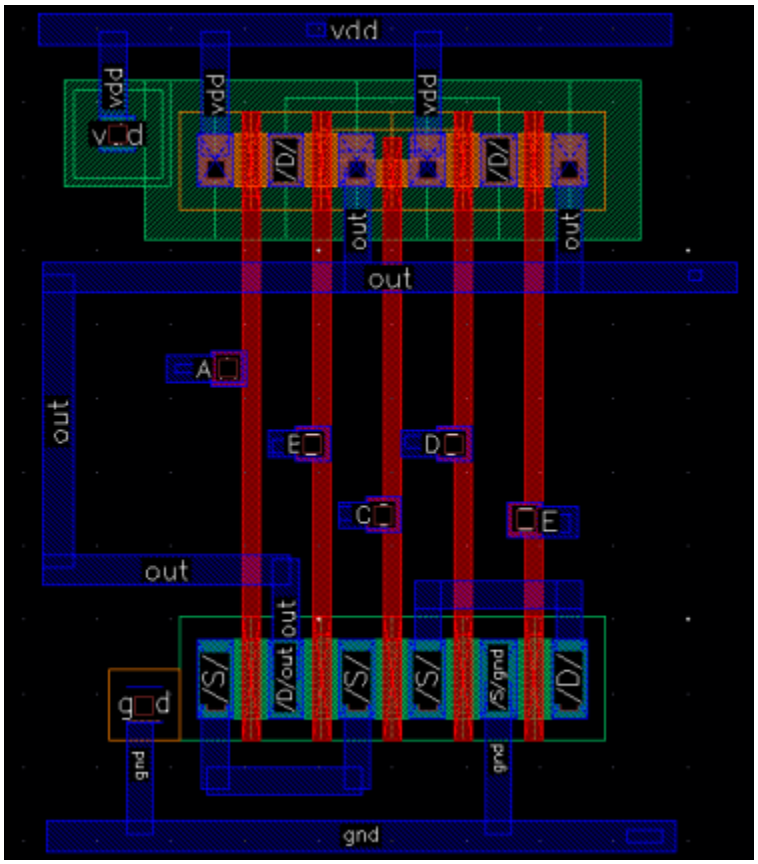

Figure 10: Standard cell layout of function

The above layout passed DRC without any errors, and all the netlists match according to the LVS report (see below for LVS results).

```
The net-lists match.

                          layout  schematic
                             instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                 10      10
        total                  10      10

                               nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                 12      12
        total                  12      12

                             terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   8       8


Probe files from /users/ugrad/2020/spring/taleba/eecs119/Cadence6/LVS/schematic
```

Figure 11: Standard cell layout passes the LVS test

The extracted capacitance of the layout also passes the LVS test (see below) and shows that the netlists match.

```
The net-lists match.

                          layout  schematic
                             instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                 10      10
        total                  10      10

                               nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                 12      12
        total                  12      12

                             terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   8       8


Probe files from /users/ugrad/2020/spring/taleba/eecs119/Cadence6/LVS/schematic
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Figure 12: Extracted capacitance of the layout passing the LVS test

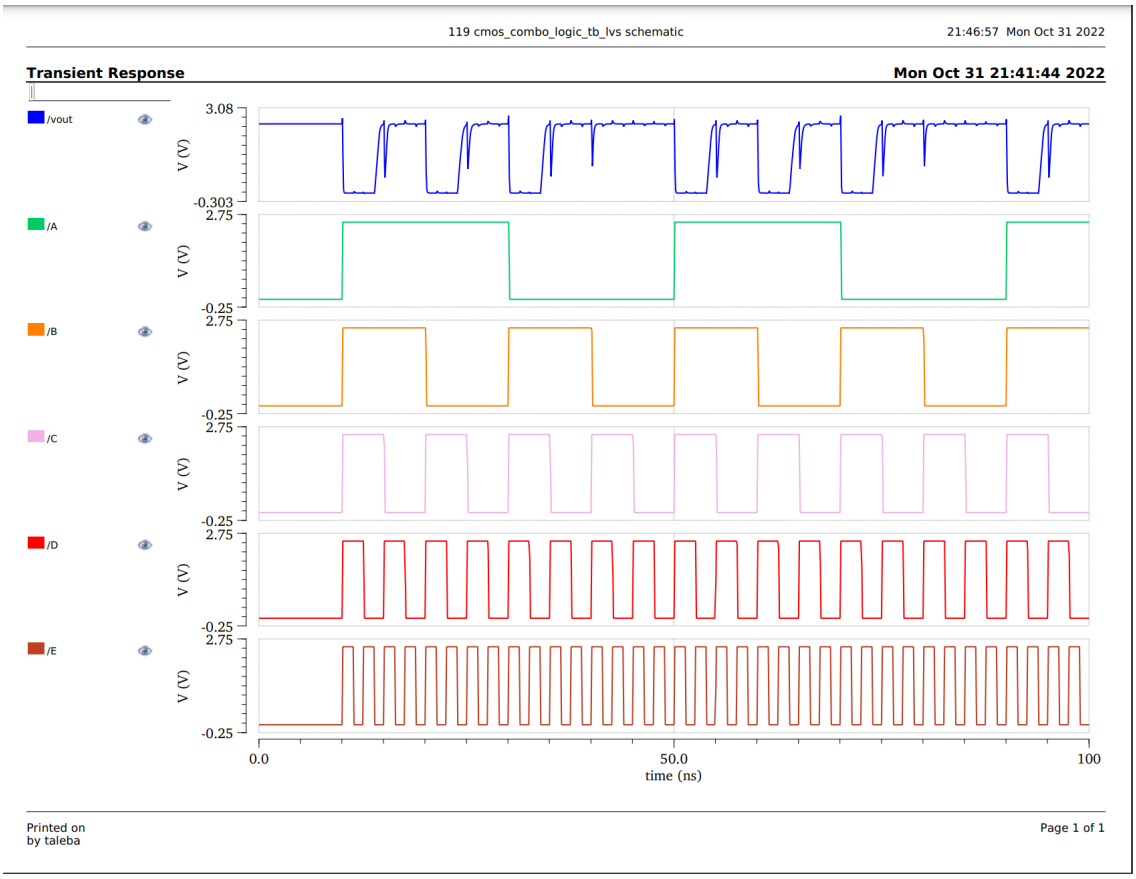

Figure 13: Output Waveform of the layout simulation, it follows the same logic as the schematic

Conclusion:

In this lab, we used Cadence to model a static CMOS, both as a circuit with a PDN and a PUN and as a standard cell layout. The standard cell layout was found by using Euler's algorithm to find a sequence that would allow for an uninterrupted fusion strip. The outputted waveform was cross-referenced with the calculated truth table for accuracy, and the waveform outputted values seen in the pictures (see output waveform, part 4). The standard cell layout passed the DRC and LVS tests and the extracted capacitances of the layout passed the LVS test (results can be seen in part 5). The output of the layout matched the output of the schematic. In the output waveform of the layout, you can see that the dips after a rise are lower than the waveform of the schematic. This shows how the parasitic capacitances affect the actual performance of the circuit.

Bibliography:

[1] Maqsood A. Chaudhry (2022), "Static CMOS"