

UCI Fall 2022

EECS 119

Project # 3

4-Bit Adder/Subtractor

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Introduction:

In this lab, a four-bit adder/subtractor will be constructed. To do so, inverters, XOR, and NAND gates will be used. These gates will be used to construct a one-bit adder, which then will be used to create the four adders/subtractors. Each of these individual components will have both their schematics and layouts completed.

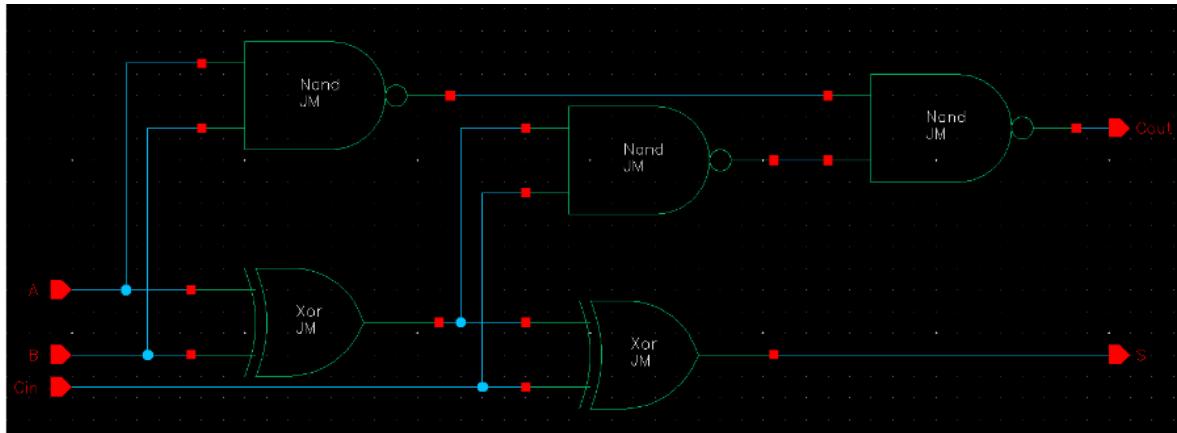


Fig 1. Full adder [4]

A full adder is constructed using three NAND gates and two XOR gates (see fig. 1).

Theory:

An adder/subtractor is capable of addition and subtraction of binary numbers. The operation depends on the binary value that the control signal, usually denoted as K, holds. It is a smaller component within an arithmetic logic unit (ALU). The one-bit adder/subtractors that make up the design of the four-bit adder/subtractor have an input carry (usually denoted as C_{in}) and an output carry (usually denoted as C_o).

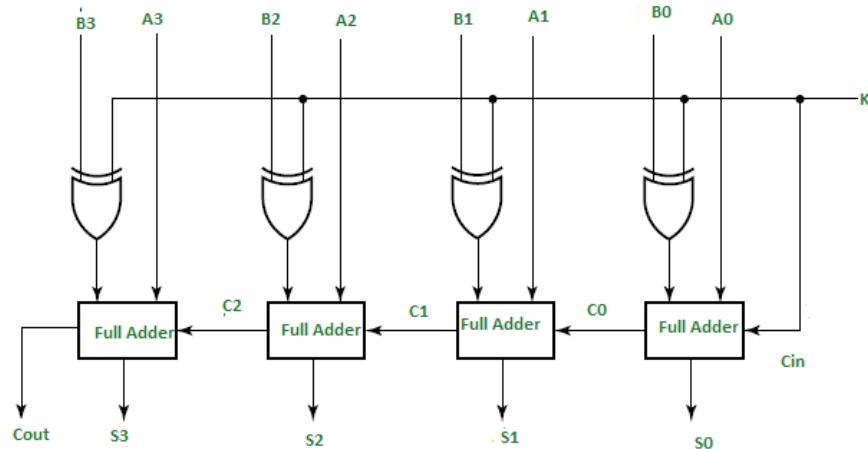


Fig 2. Four-bit adder/subtractor schematic [3]

Design 4-bit adder/subtractor:

Schematic:

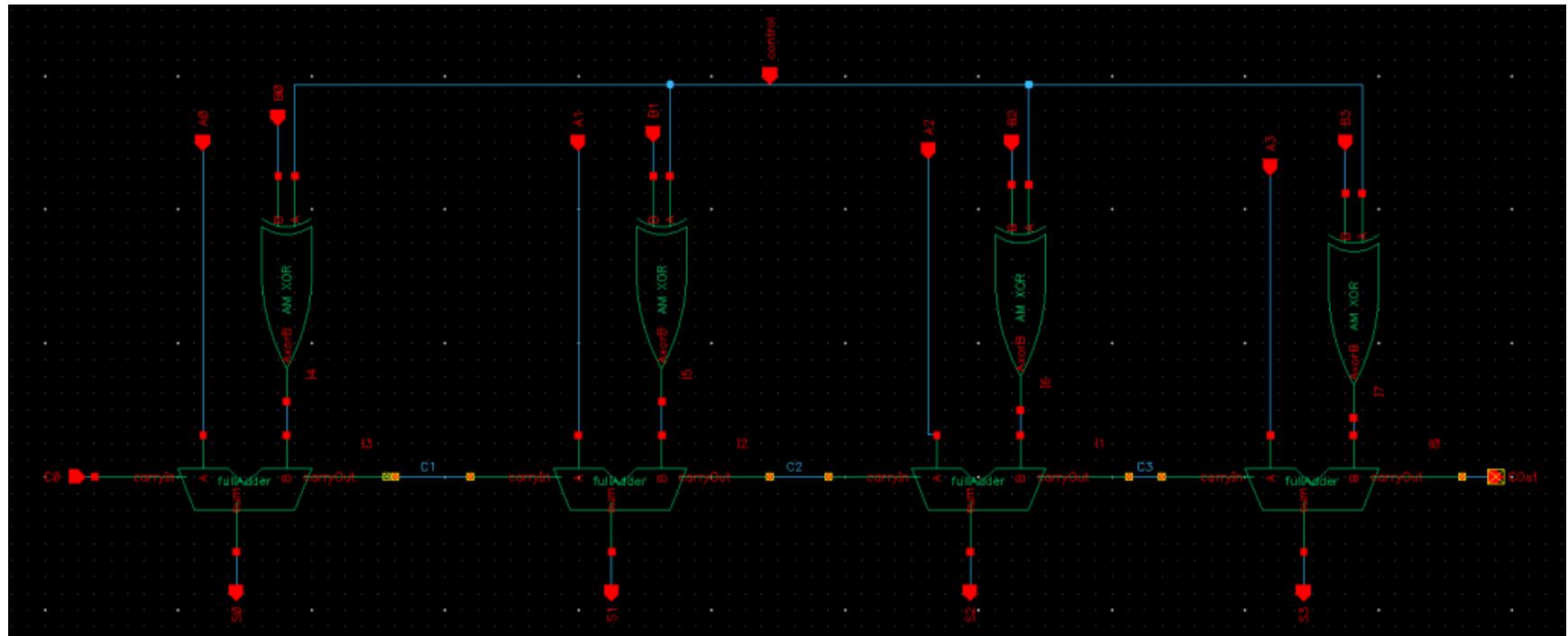


Fig 3. 4-bit adder/subtractor schematic

Test Schematic:

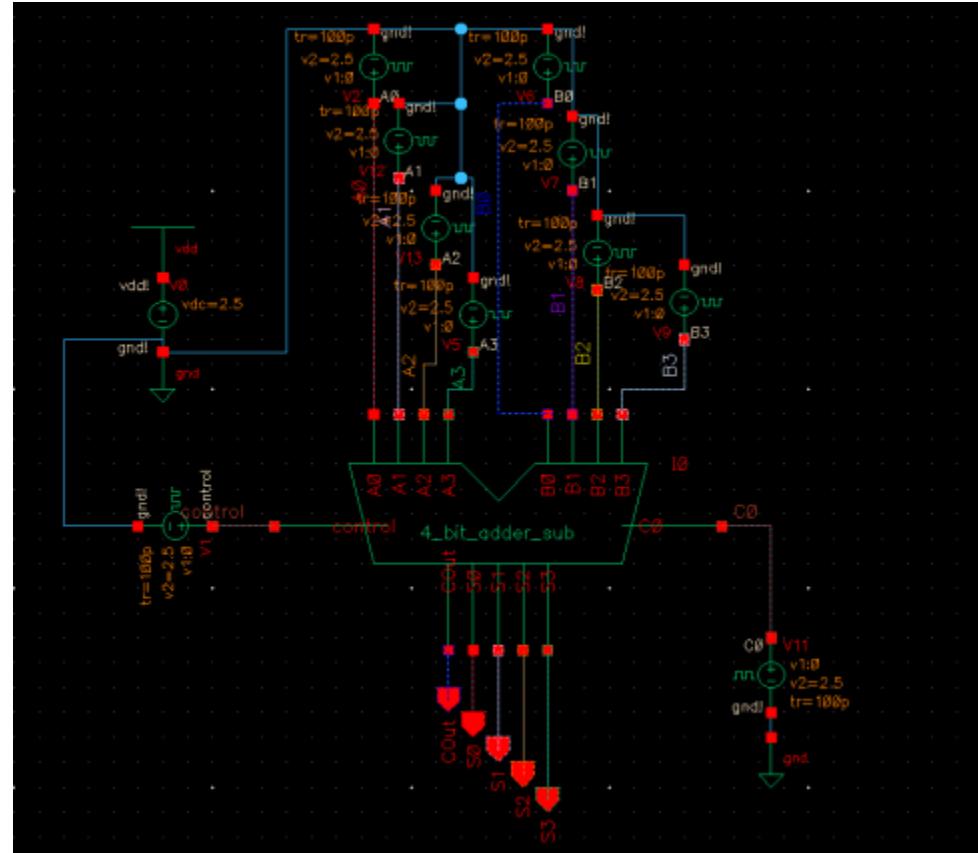


Fig 4. Test bench for 4-bit adder/subtractor

Symbol:

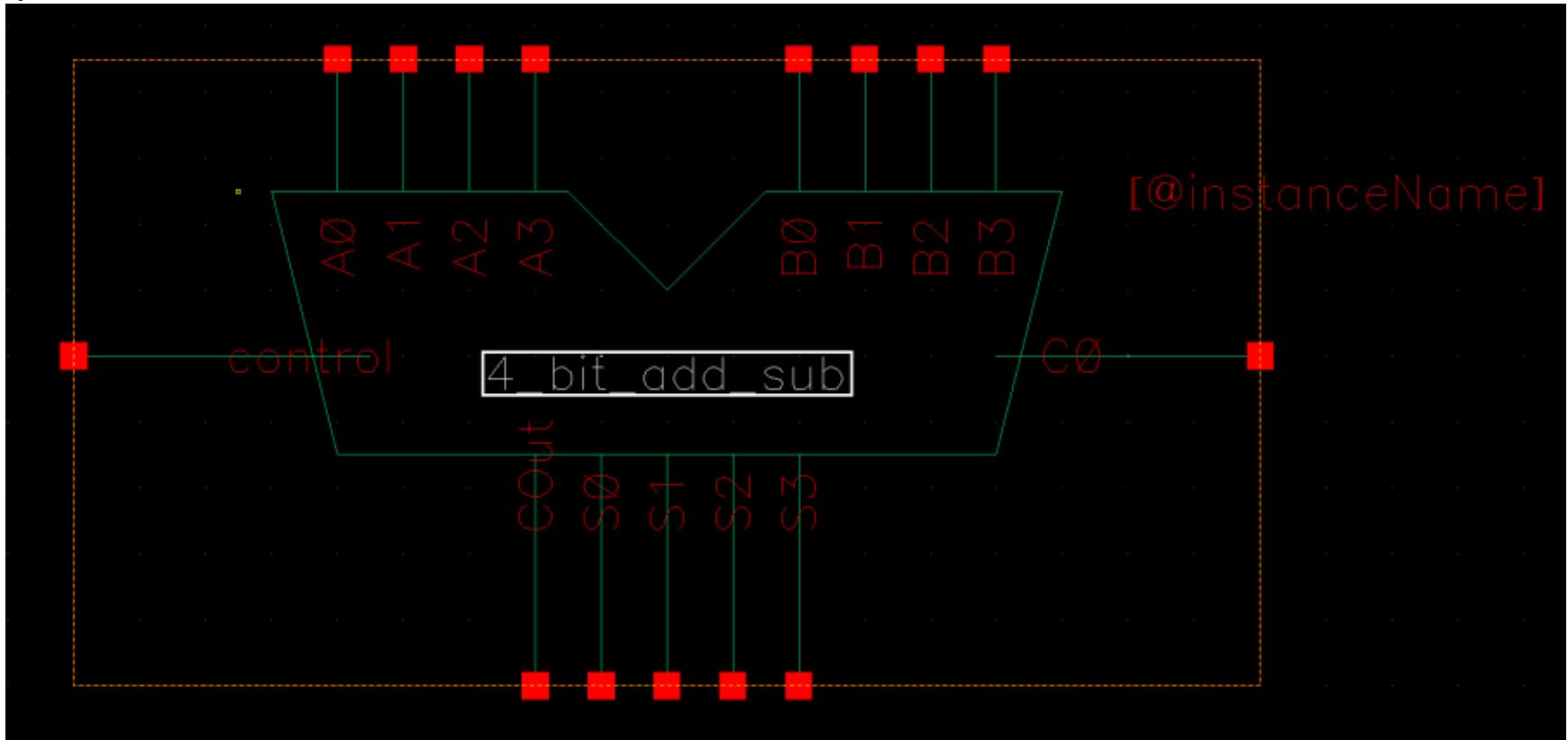
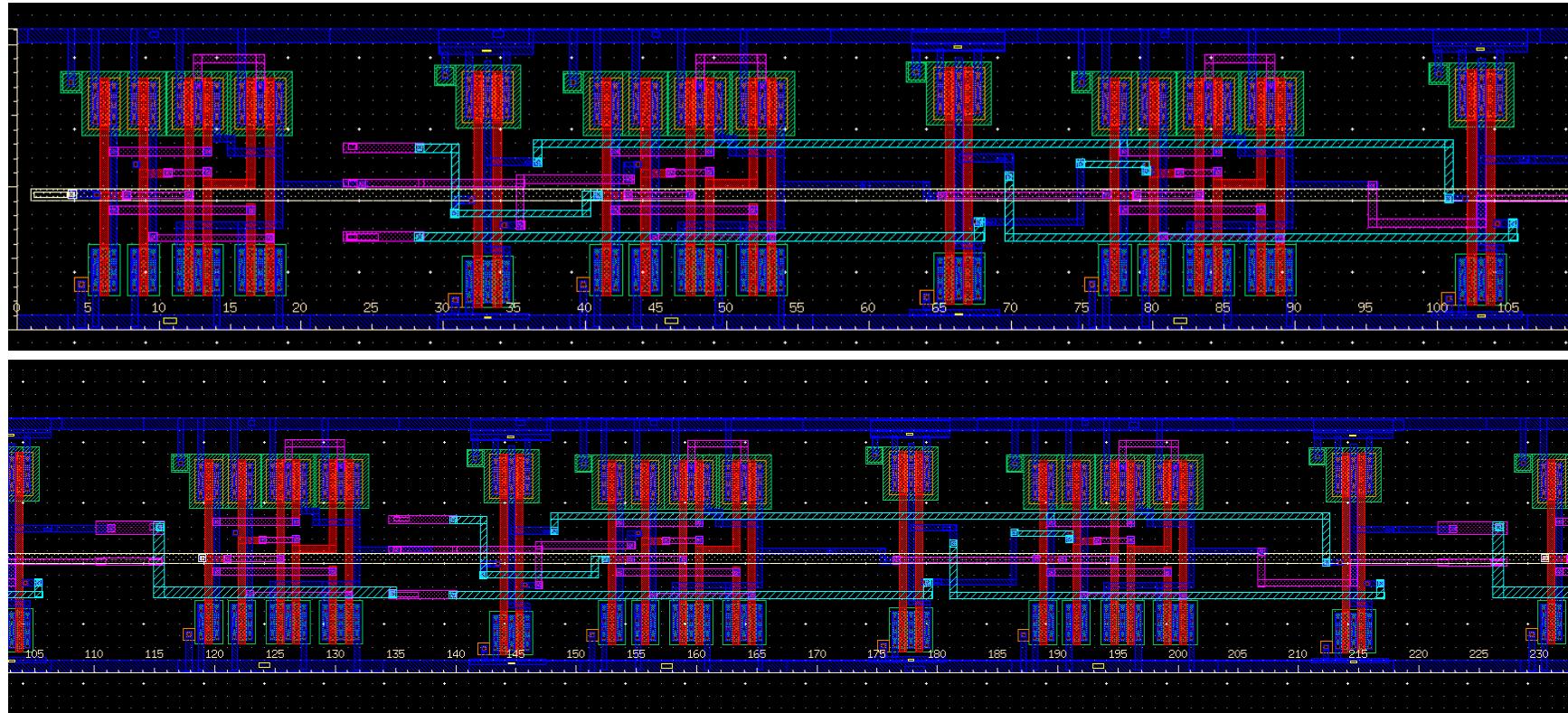


Fig 5. 4-bit adder/subtractor symbol

Layout:



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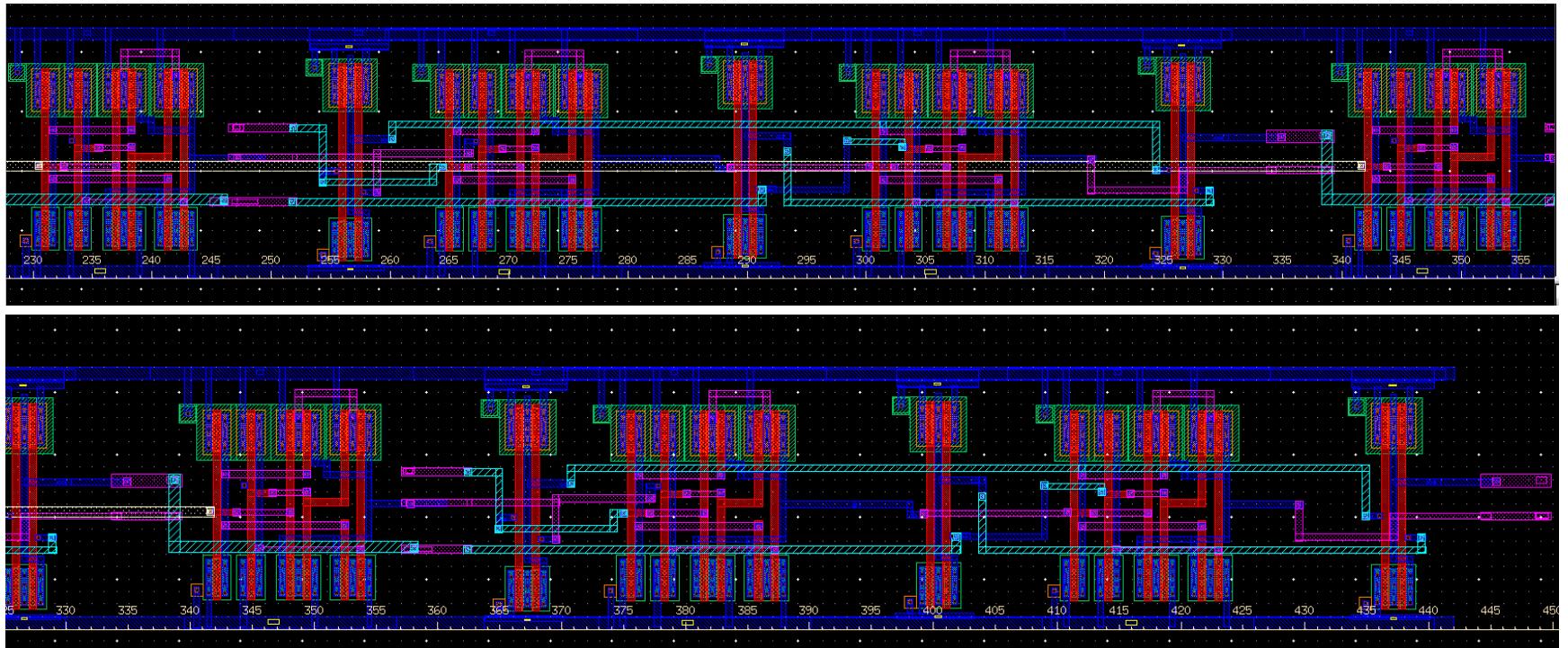


Fig 6. 4-bit adder/subtractor layout

Passes LVS Schematic

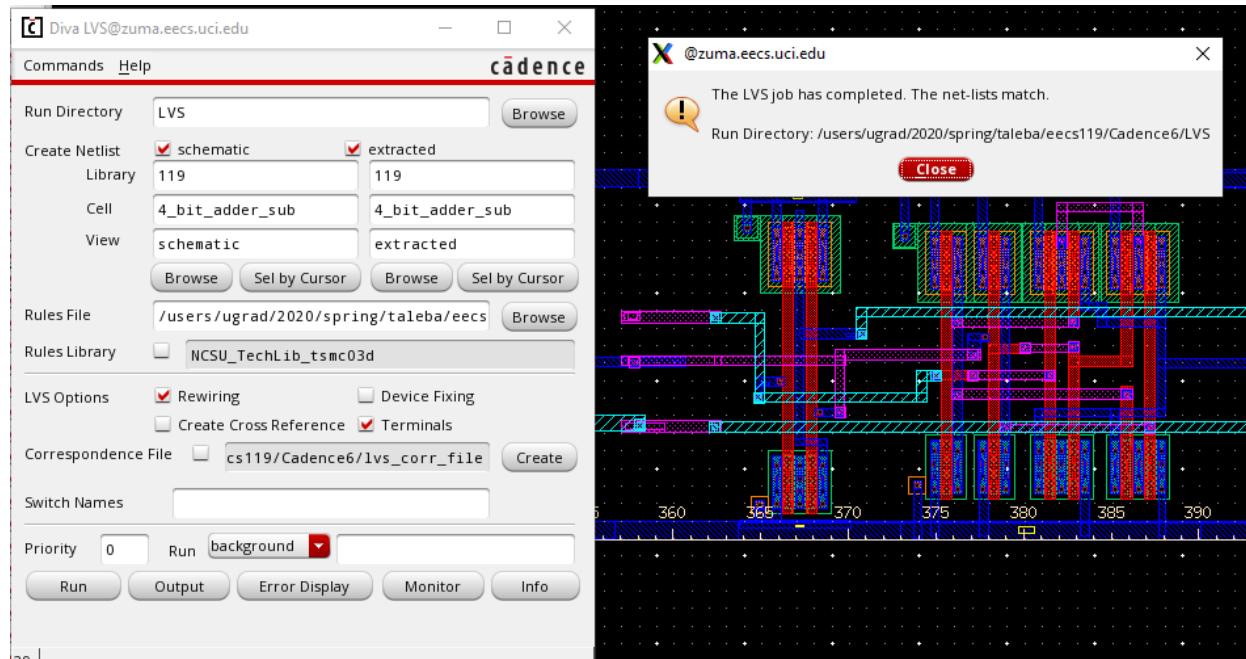


Fig 7. LVS for 4-bit adder/subtractor

Passes LVS extracted capacitance

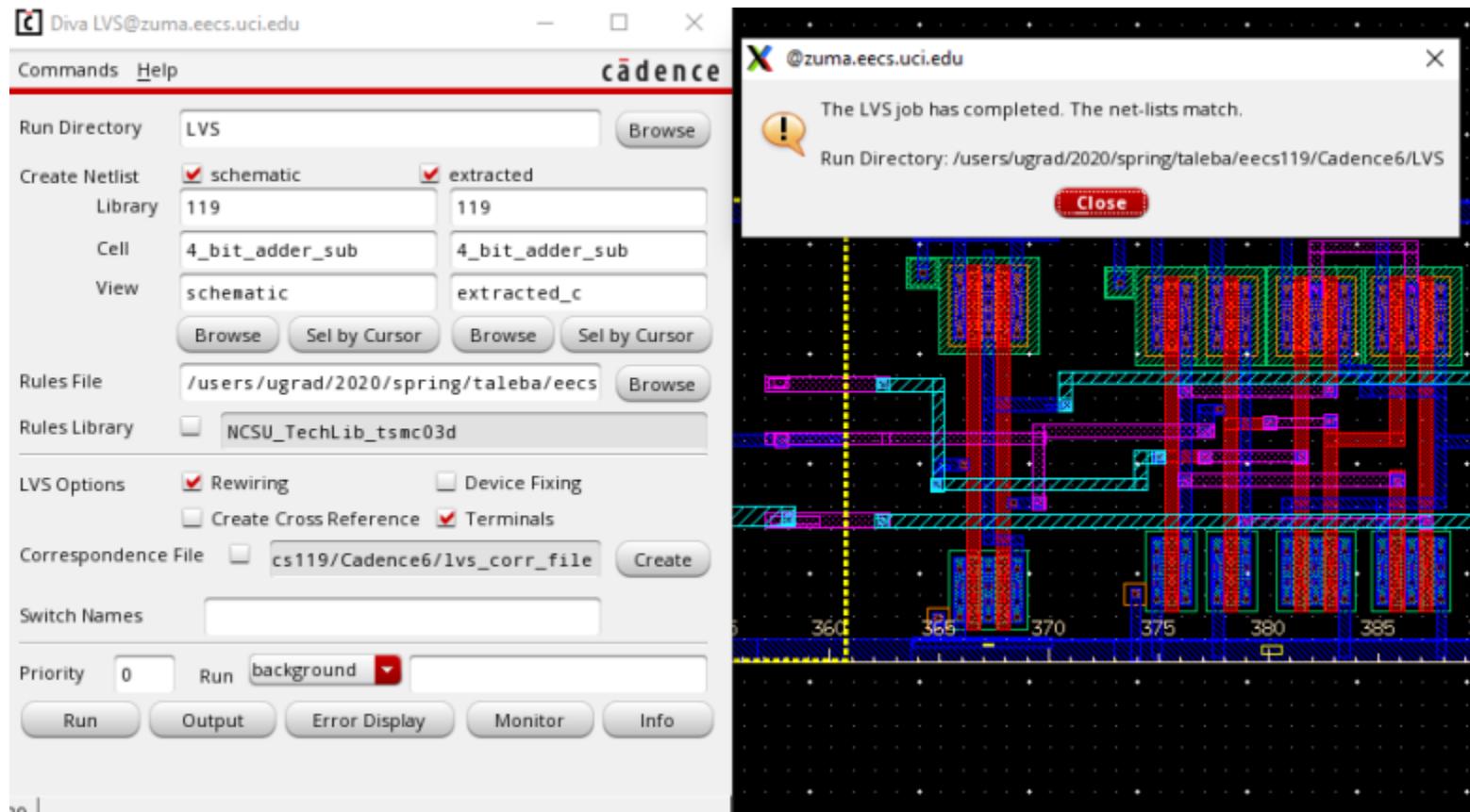


Fig 8. LVS for 4-bit adder/subtractor extracted capacitance

Design 1-bit adder/subtractor:

Schematic:

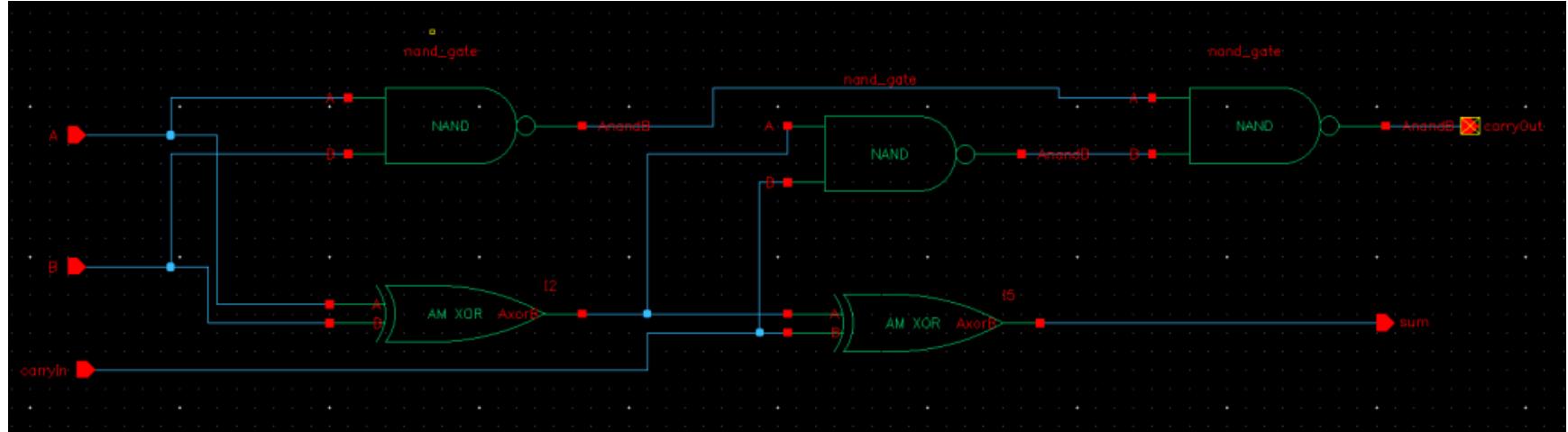


Fig 9. Schematic for 1-bit adder

Symbol:

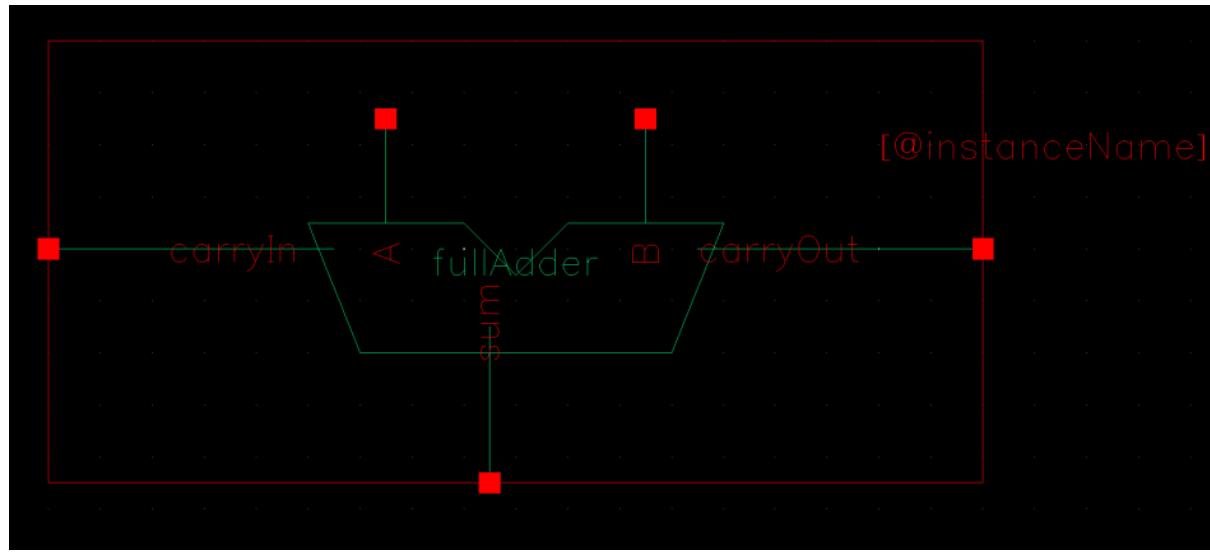


Fig 10. Symbol for 1-bit adder

Layout:

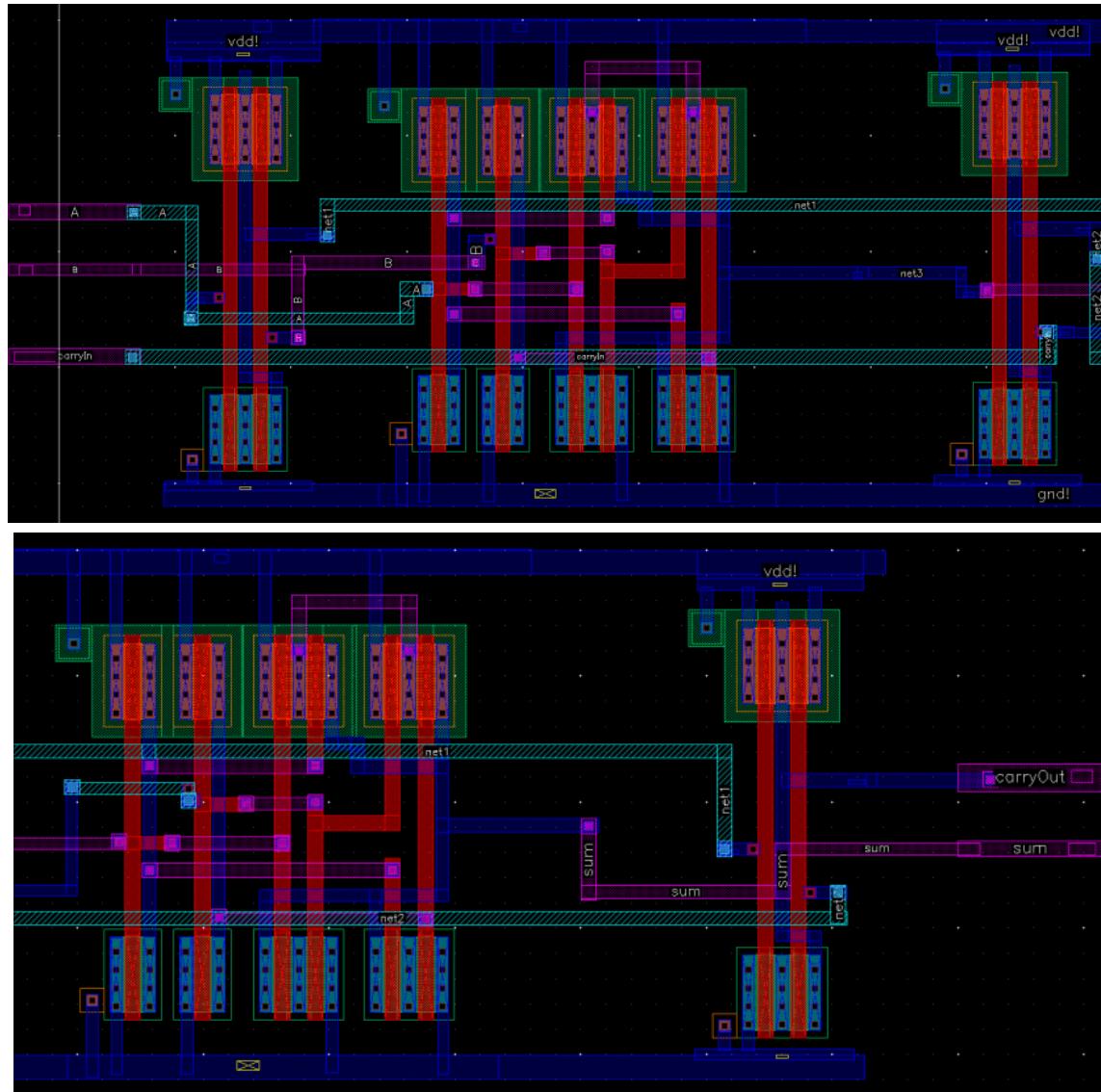


Fig 11. Layout for 1-bit adder

Passes LVS:

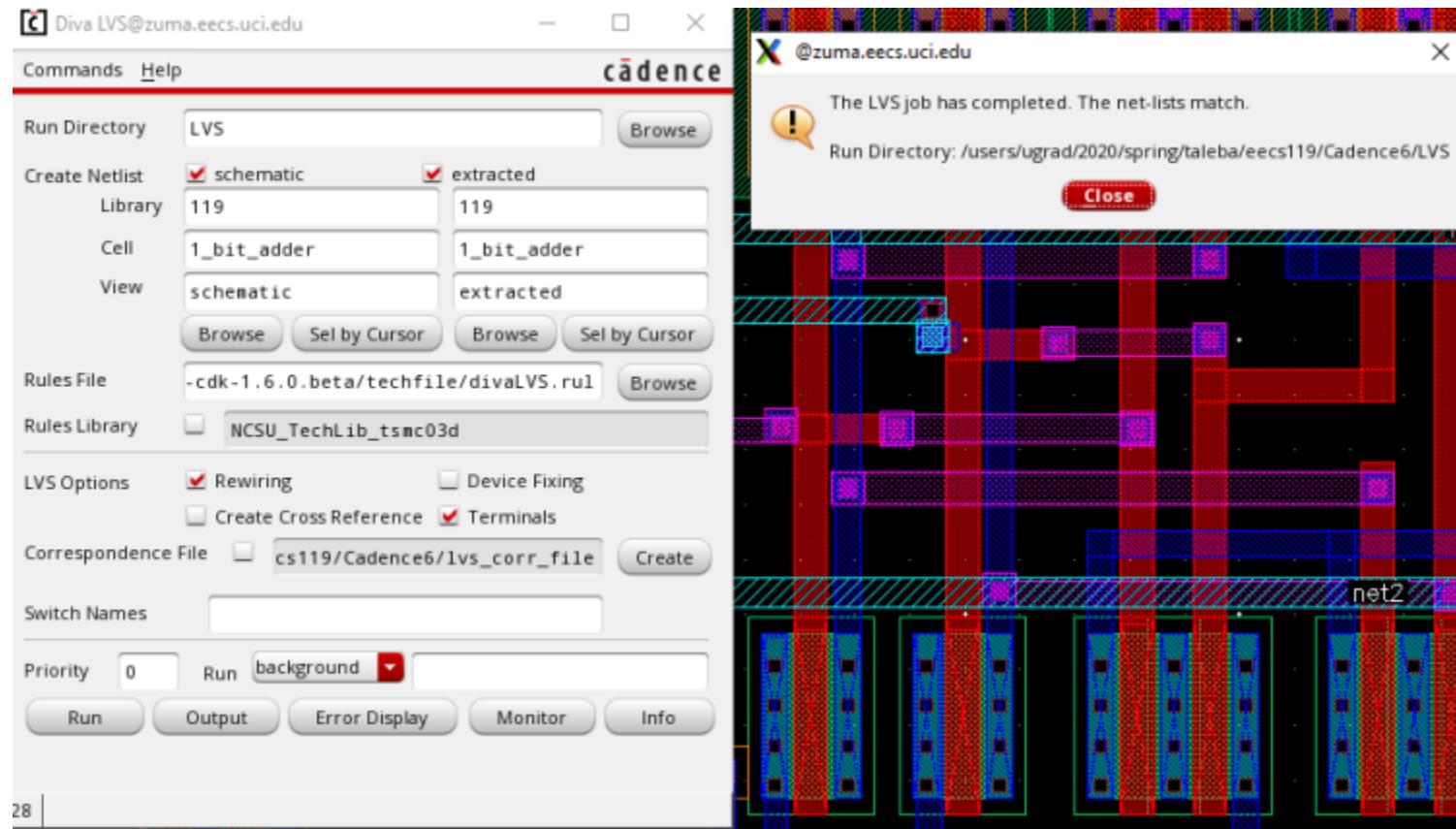


Fig 12. LVS for 1-bit adder

Design XOR

Schematic:

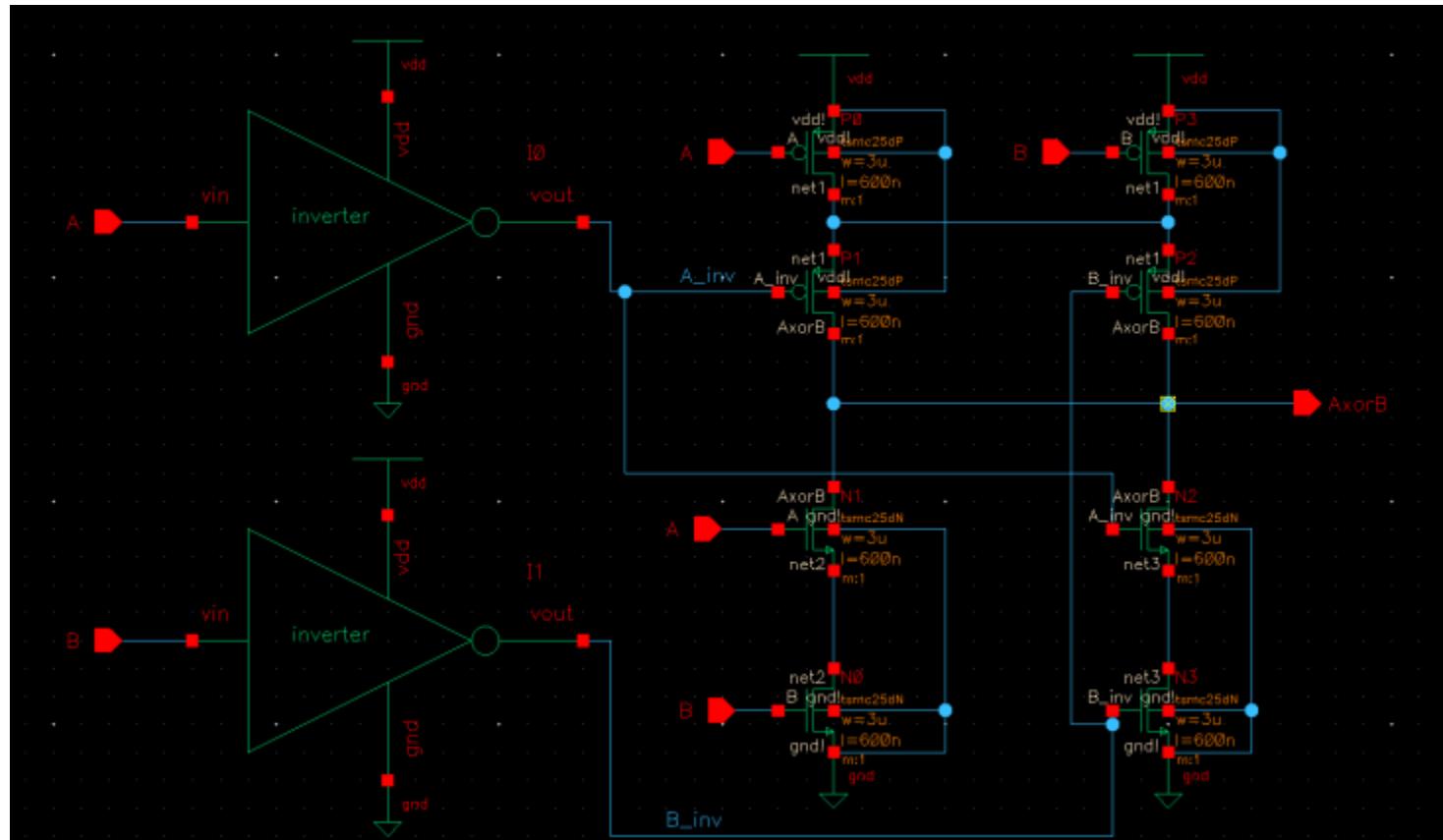


Fig 13. Schematic for XOR gate

Symbol:

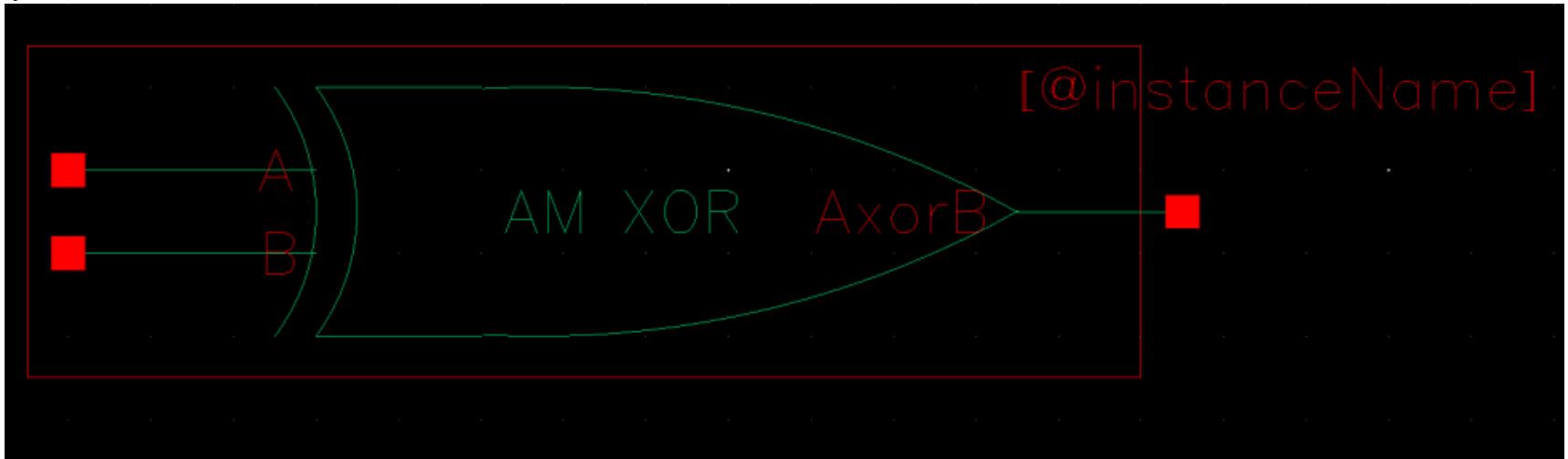


Fig 14. Symbol for XOR gate

Layout:

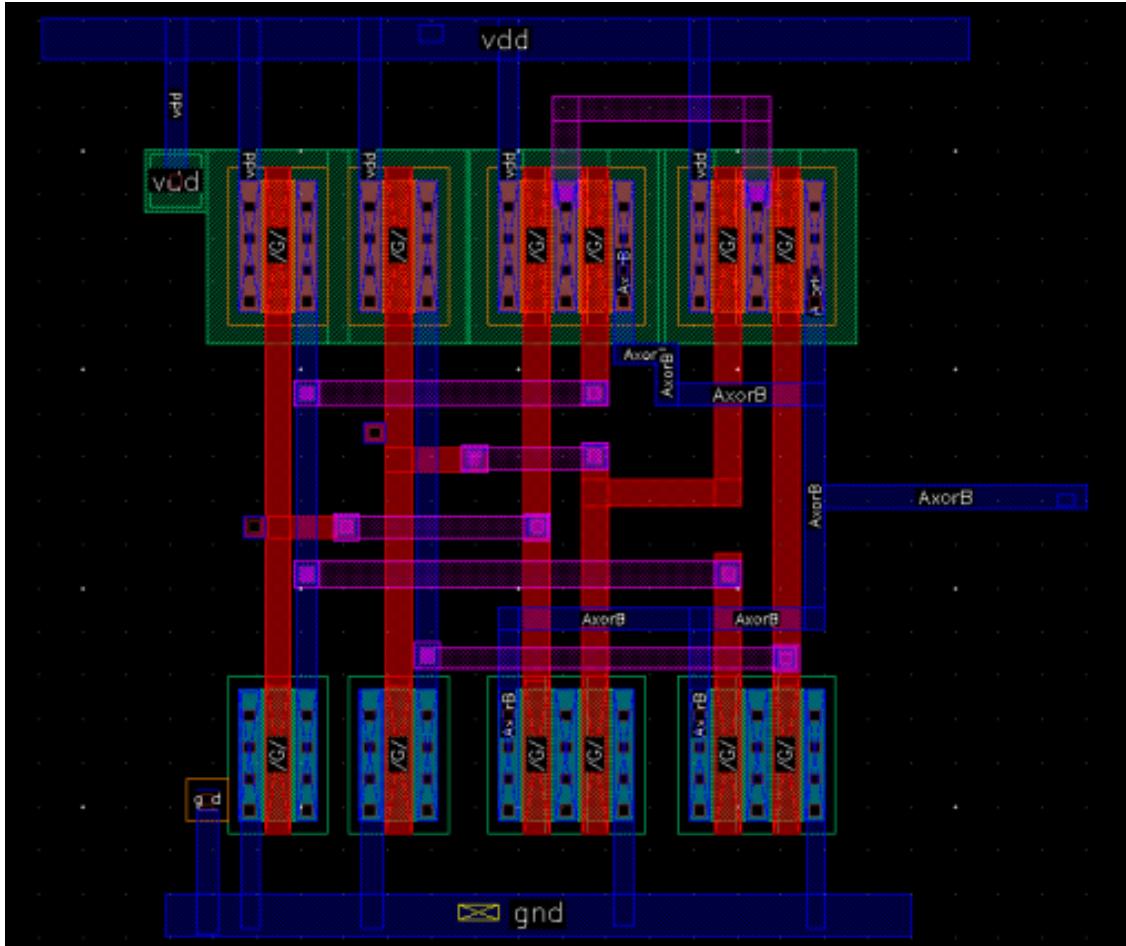


Fig 15. Layout for XOR gate

Passes LVS:

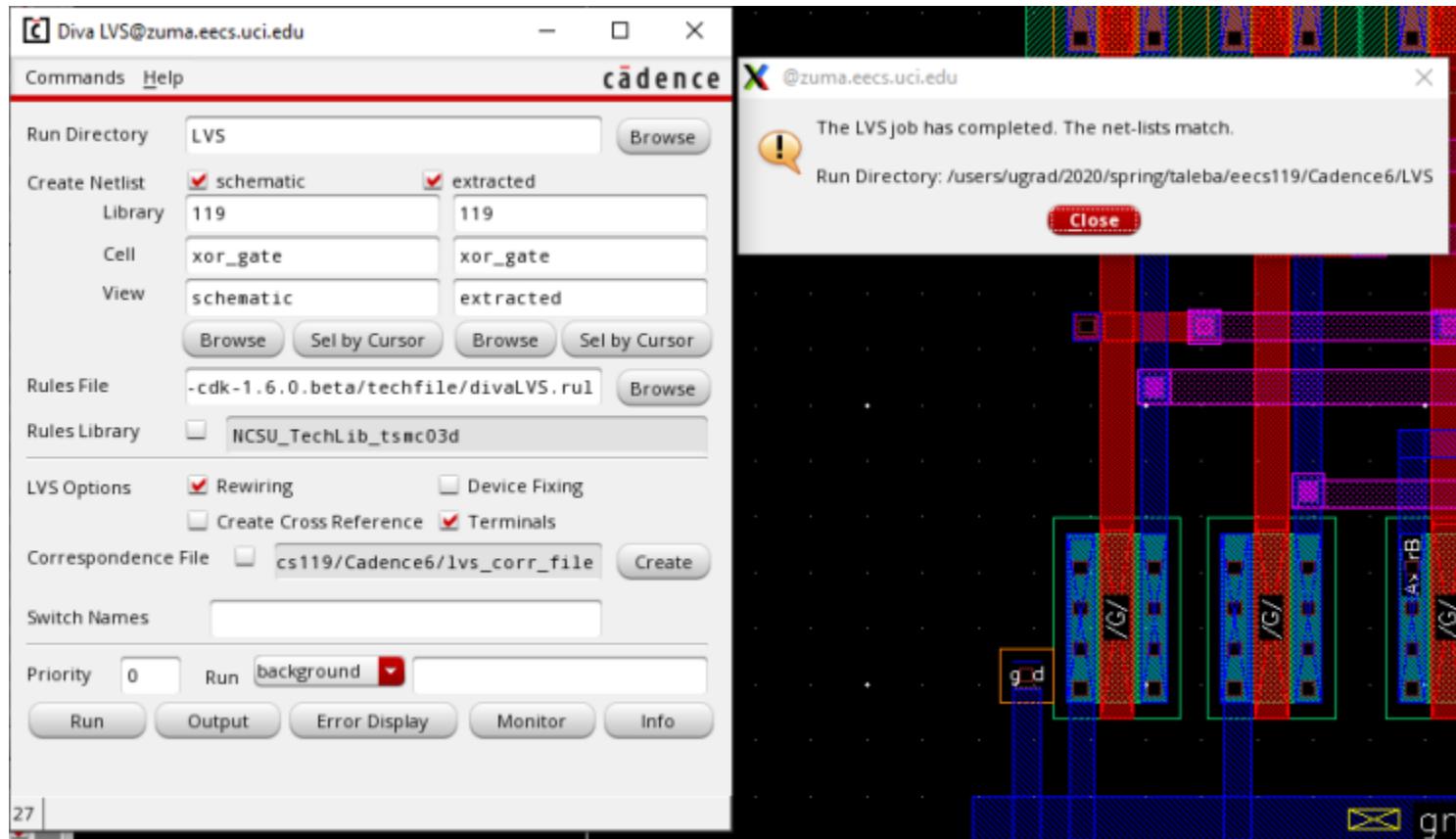


Fig 16. LVS for XOR gate

Design NAND:

Schematic:

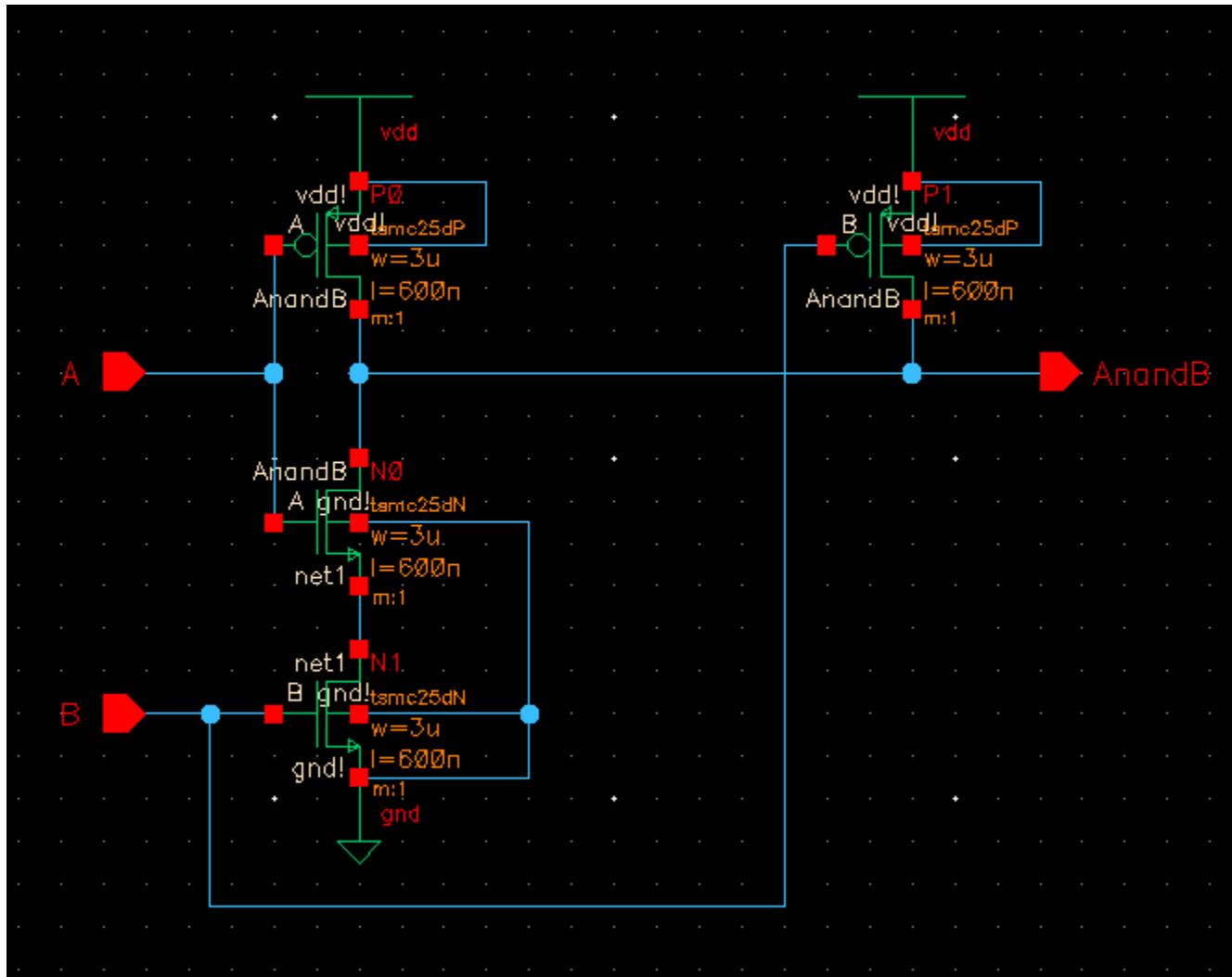


Fig 17. Schematic for NAND gate

Symbol:

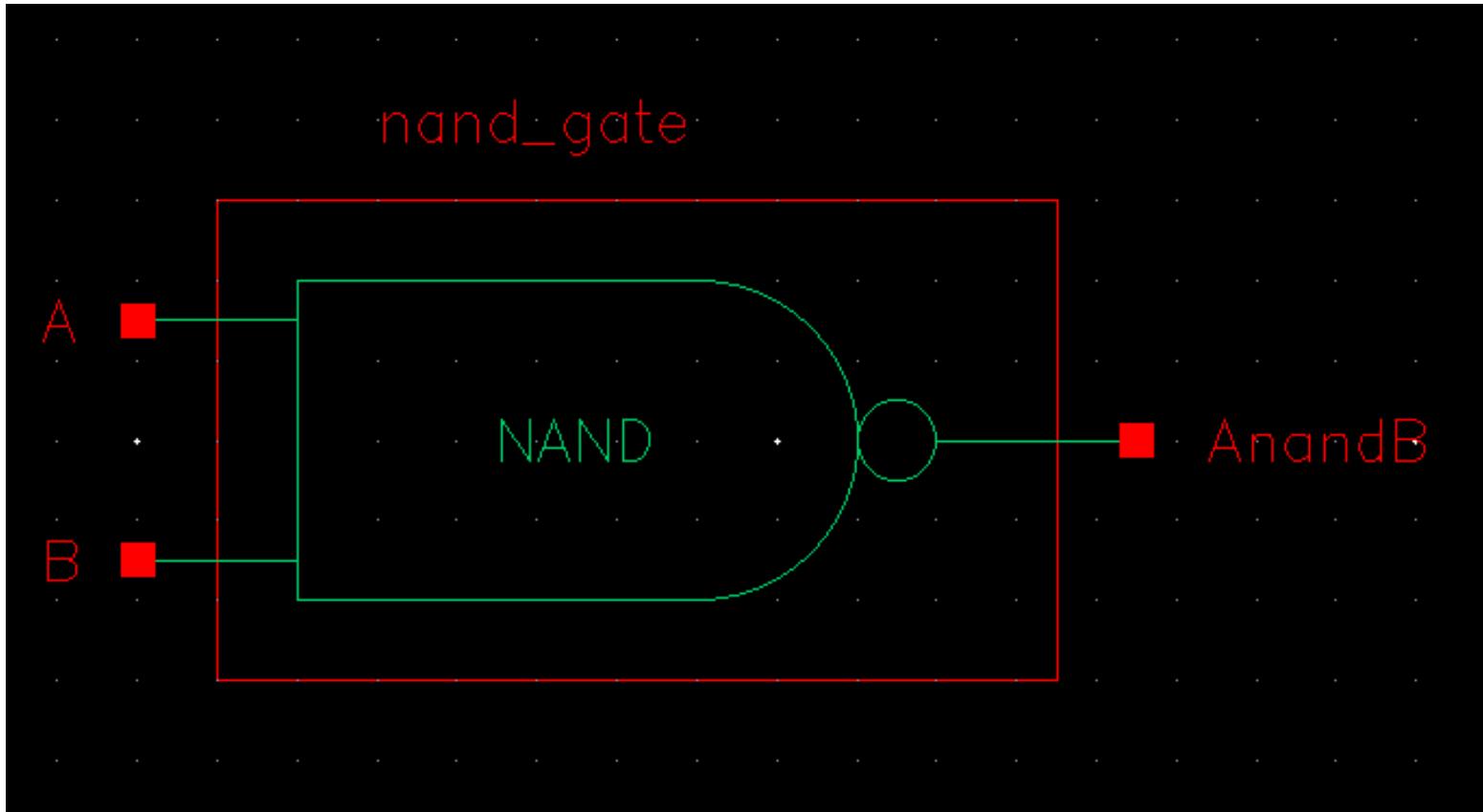


Fig 18. Symbol for NAND gate

Layout:

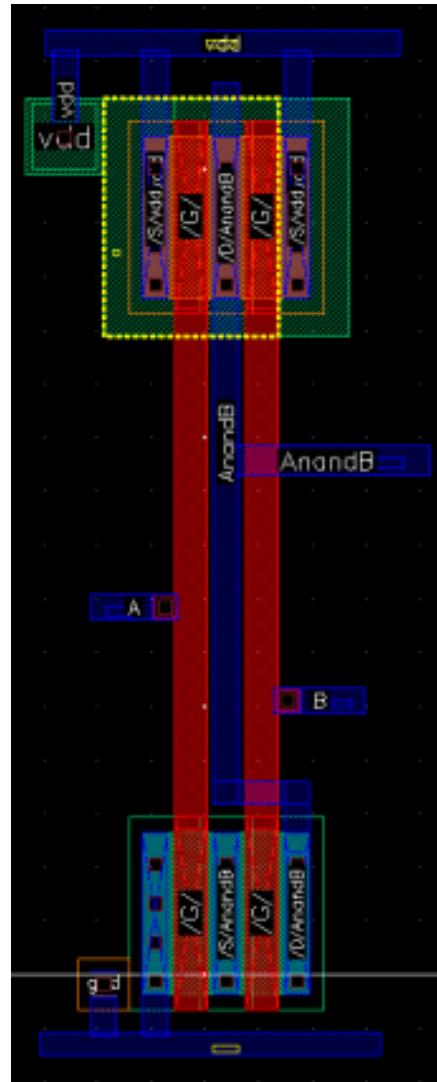


Fig 19. Layout for NAND gate

Passes LVS:

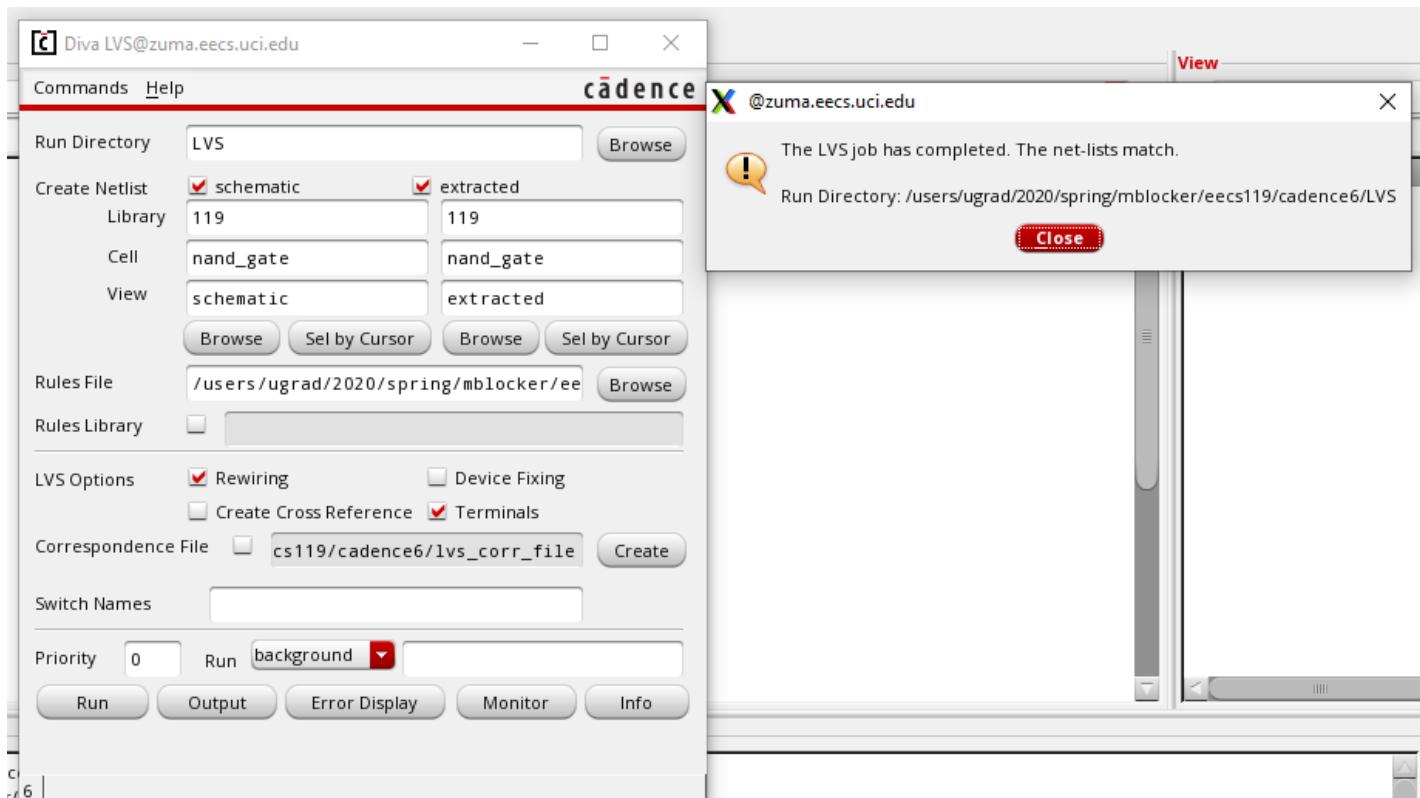


Fig 20. LVS for NAND gate

Results:

control	C0	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	CarryOut	
0	0	0	1	0	1	0	0	1	1	1	0	0	0	0	5+3=8
1	1	1	1	1	1	1	0	0	1	0	1	1	0	1	15-9=6
0	0	1	1	1	0	0	0	0	1	1	1	1	1	0	15+1=16
0	0	1	1	1	0	1	1	1	0	1	1	0	0	1	15+15=30
1	1	1	0	0	1	0	1	1	0	0	0	1	1	1	9-6=3
1	1	0	1	1	1	0	1	1	1	0	0	0	0	1	7-7=0

Table 1. Truth table for equations for testing

Simulations for the 4-bit adder schematic:

$$A_3 A_2 A_1 A_0 + B_3 B_2 B_1 B_0 = S_3 S_2 S_1 S_0 \quad Cout =$$

$$0101 + 0011 = 1000 \quad Cout = 0$$

$$5+3 = 8:$$

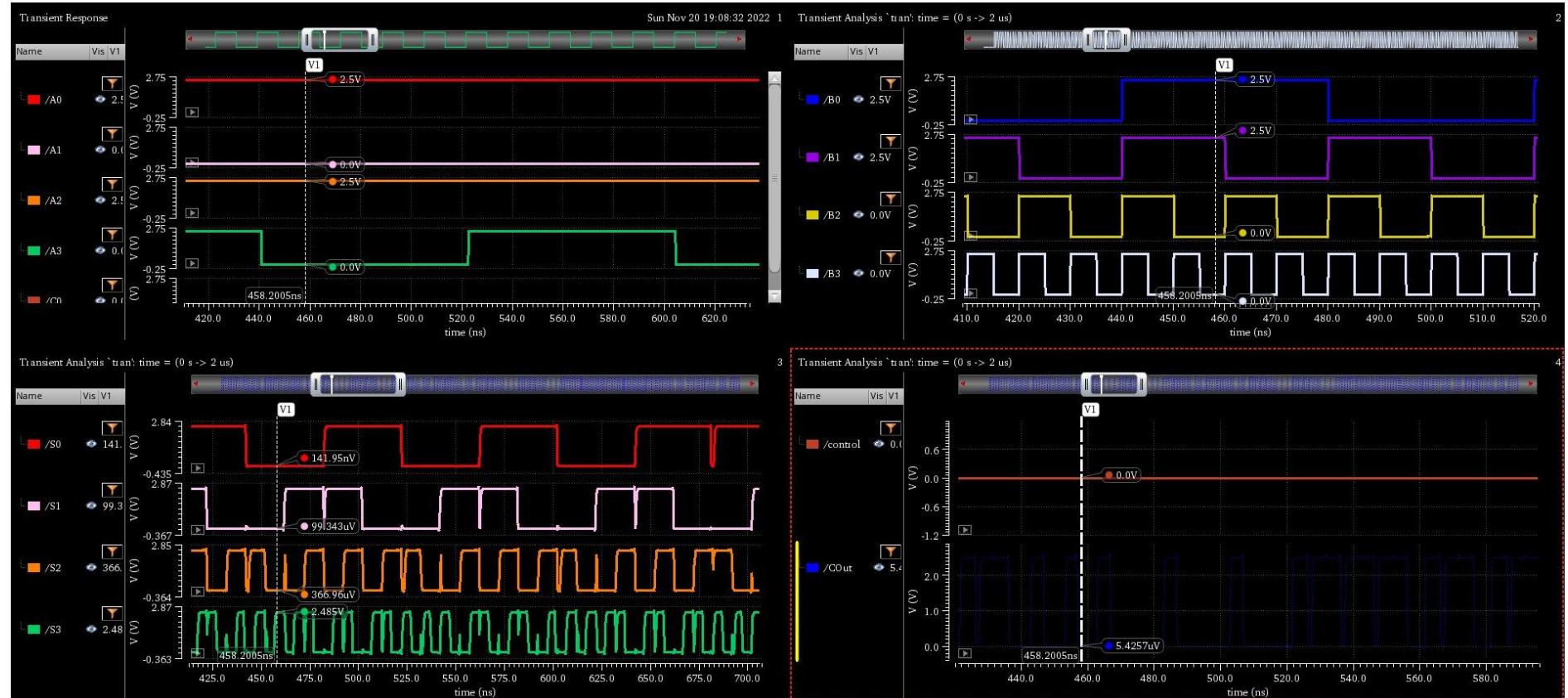


Fig 21. $5+3 = 8$ simulation

$$7-7 = 0:$$

$$0111 - 0111 = 0000 \text{ Cout} = 1$$

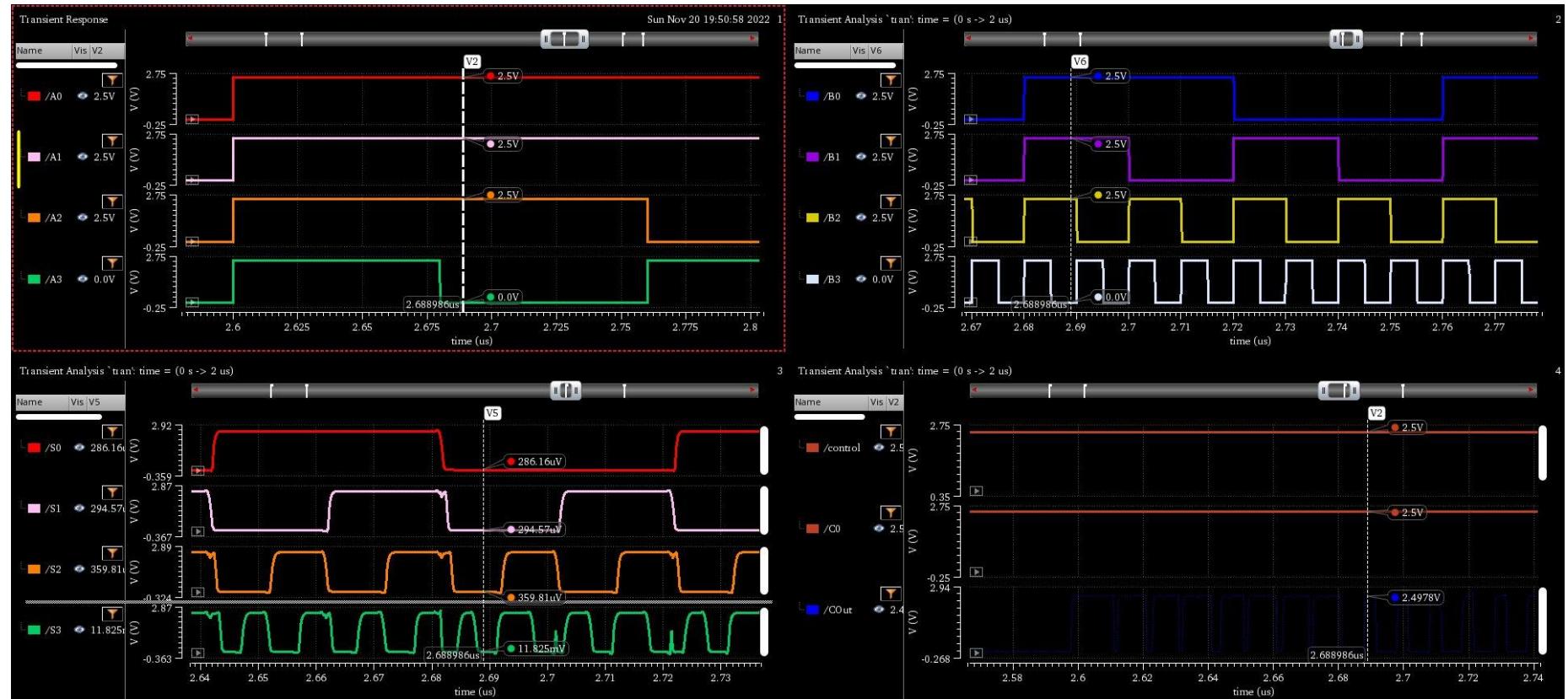


Fig 22. 7-7 = 0 simulation

$$9-6 = 3:$$

$$1001 - 0110 = 0011 \text{ Cout} = 1$$

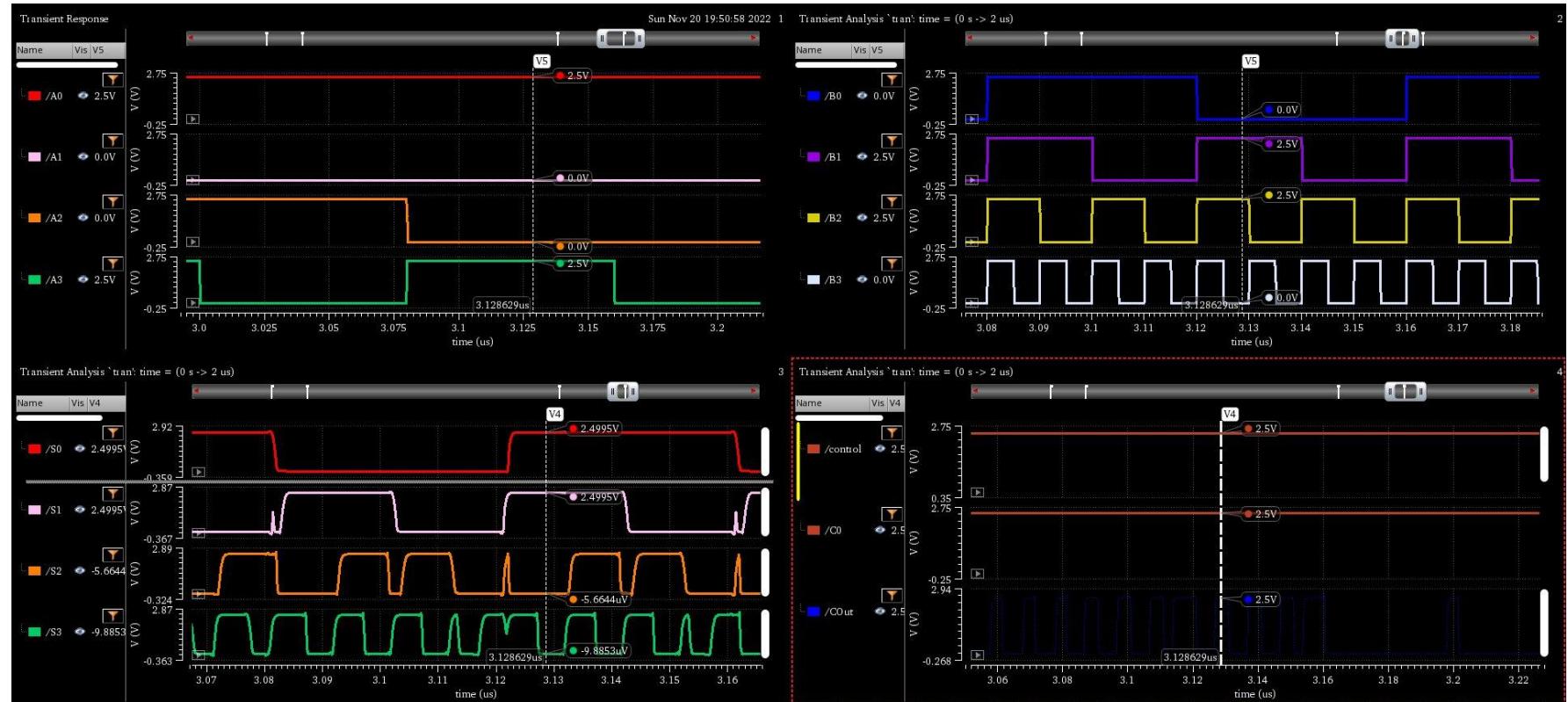


Fig 23. 9-6 = 3 simulation

$15+1 = 16$:

$$1110 + 0001 = 1111 \text{ Cout} = 0$$

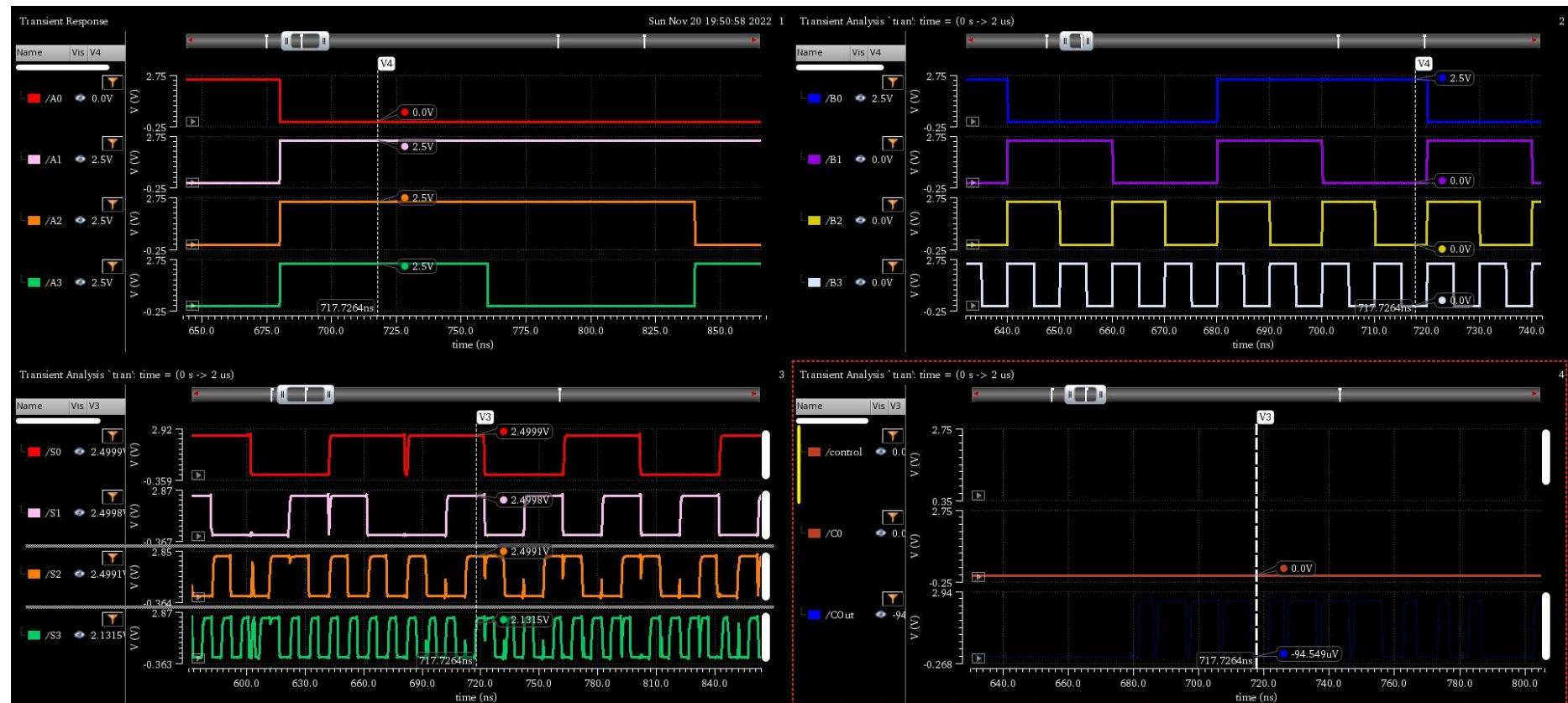


Fig 24. $15+1 = 16$ simulation

$$15+15 = 30:$$

$$1110 + 1110 = 0011 \text{ Cout} = 1$$

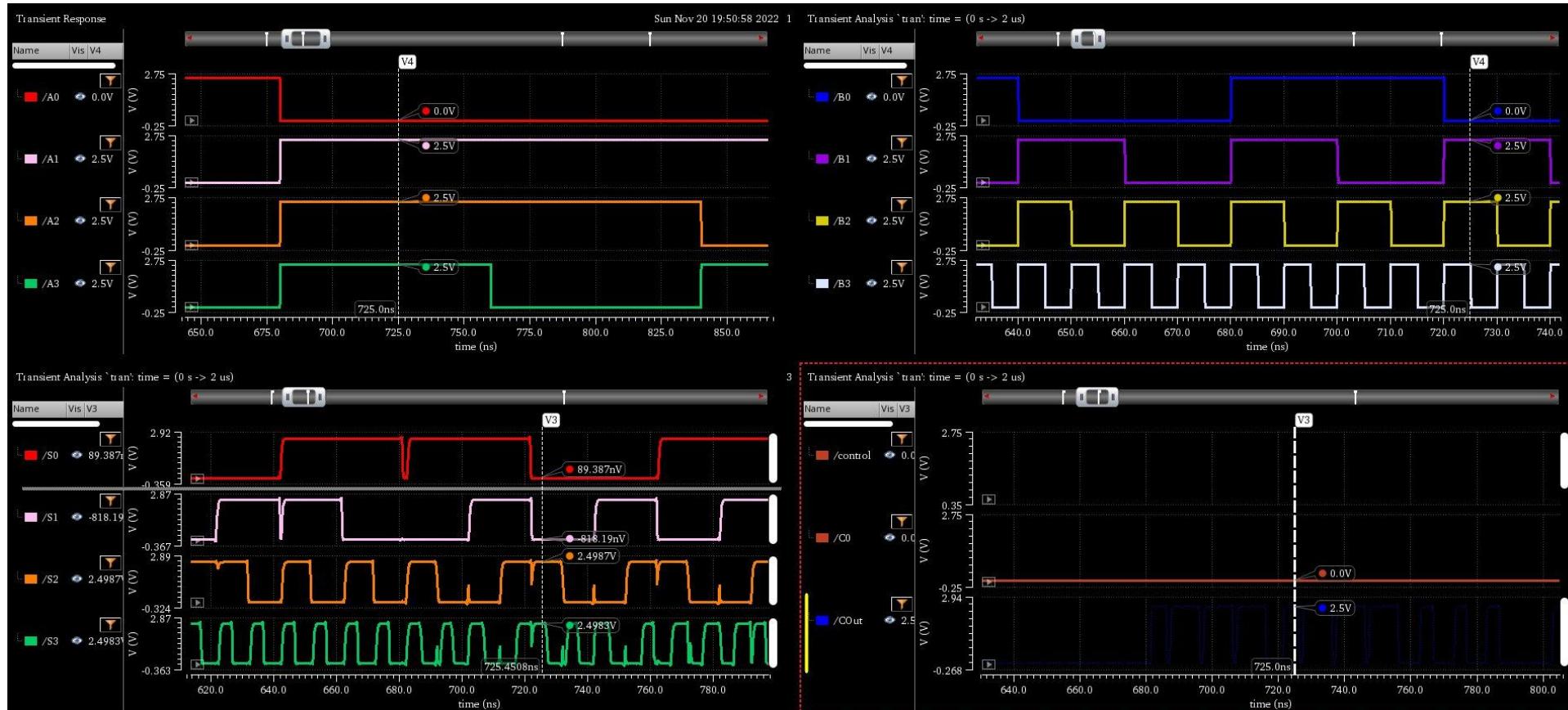


Fig 25. $15+15 = 30$ simulation

$$15-9 = 6:$$

$$1110 - 1001 = 0110 \text{ Cout} = 1$$

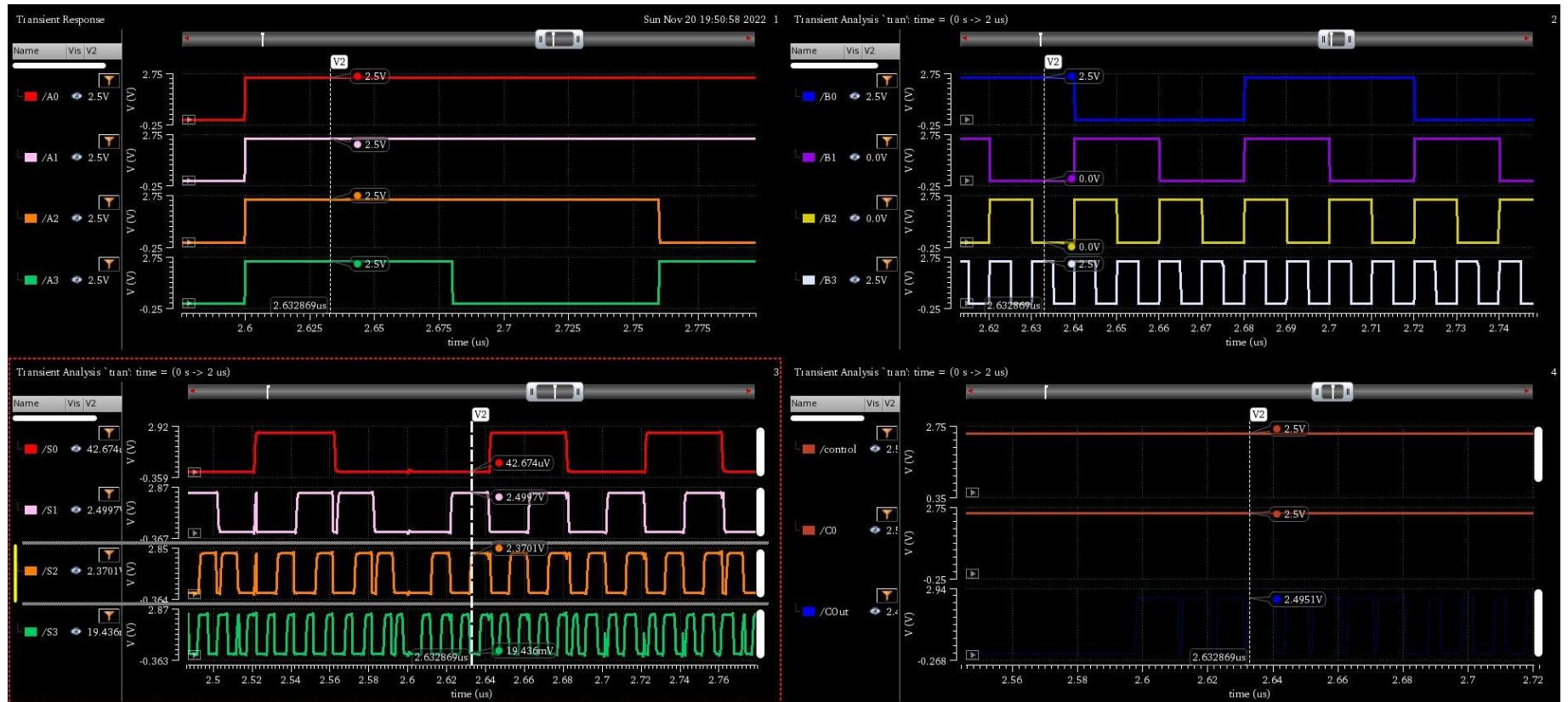


Fig 26. 15-9 = 6 simulation

Simulation for the 4-bit adder layout:

$$A_3 A_2 A_1 A_0 + B_3 B_2 B_1 B_0 = S_3 S_2 S_1 S_0 \quad Cout =$$

$$5+3 = 8:$$

$$0101 + 0011 = 1000 \quad Cout = 0$$

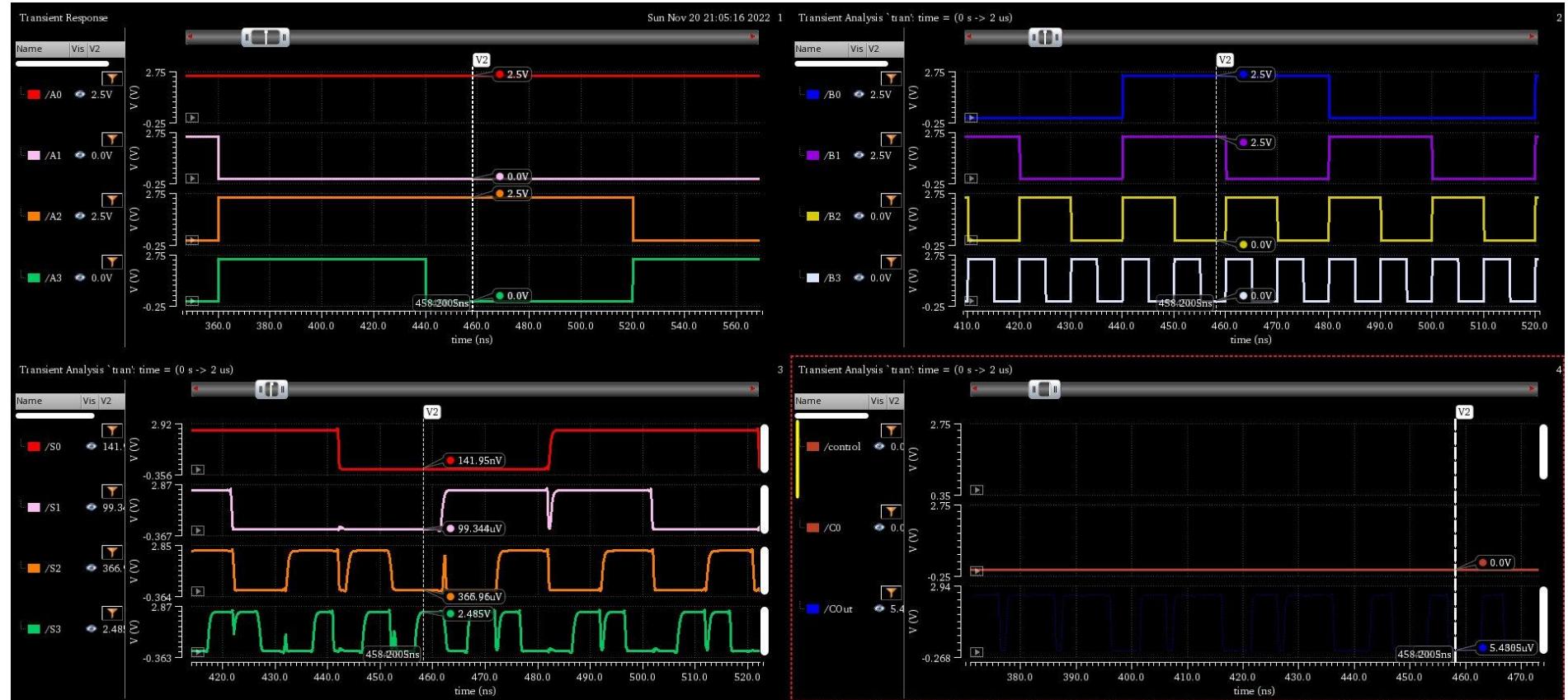


Fig 27. $5+3 = 8$ simulation (layout)

$$7-7 = 0:$$

$$0111 - 0111 = 0000 \text{ Cout} = 1$$

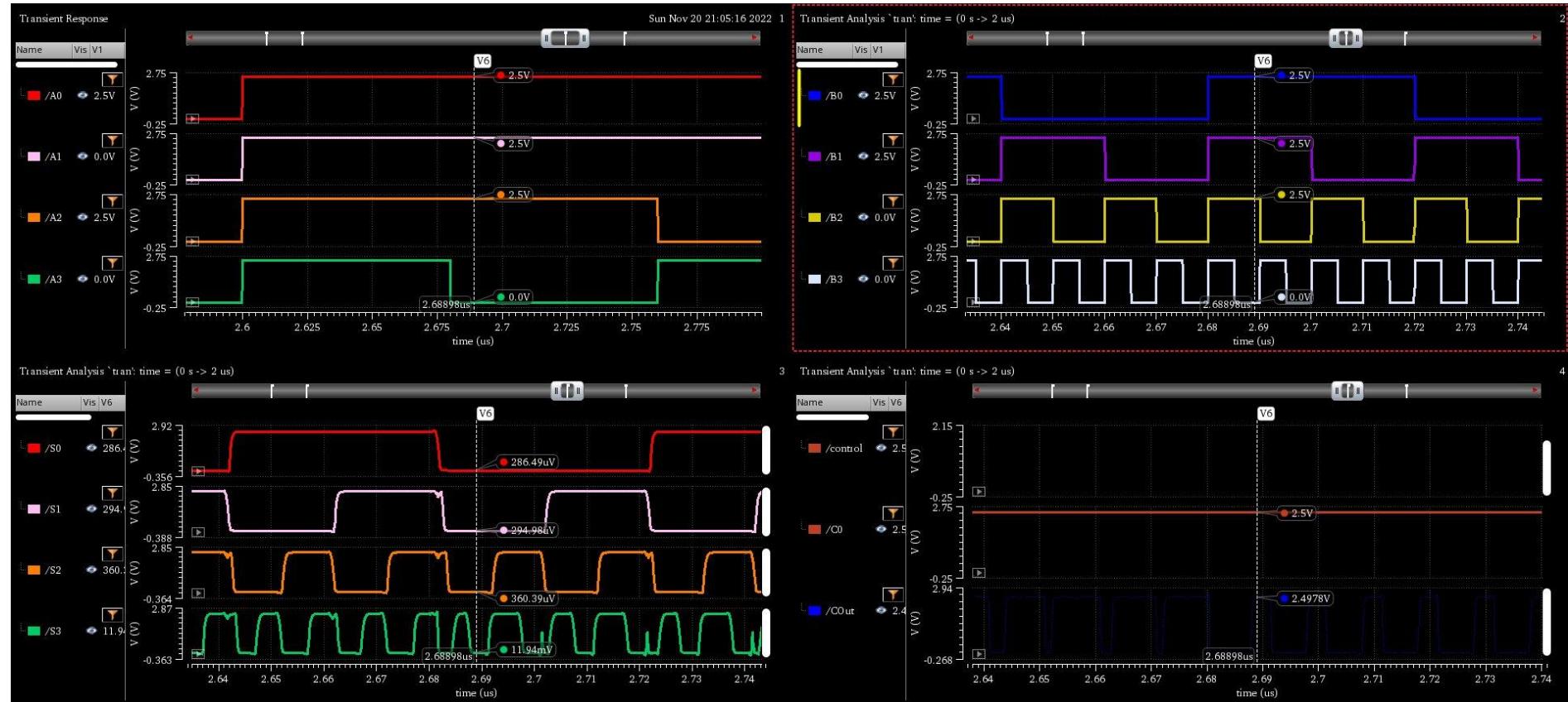


Fig 28. $7-7 = 0$ simulation (layout)

$9-6 = 3$:

$$1001 - 0110 = 0011 \text{ Cout} = 1$$

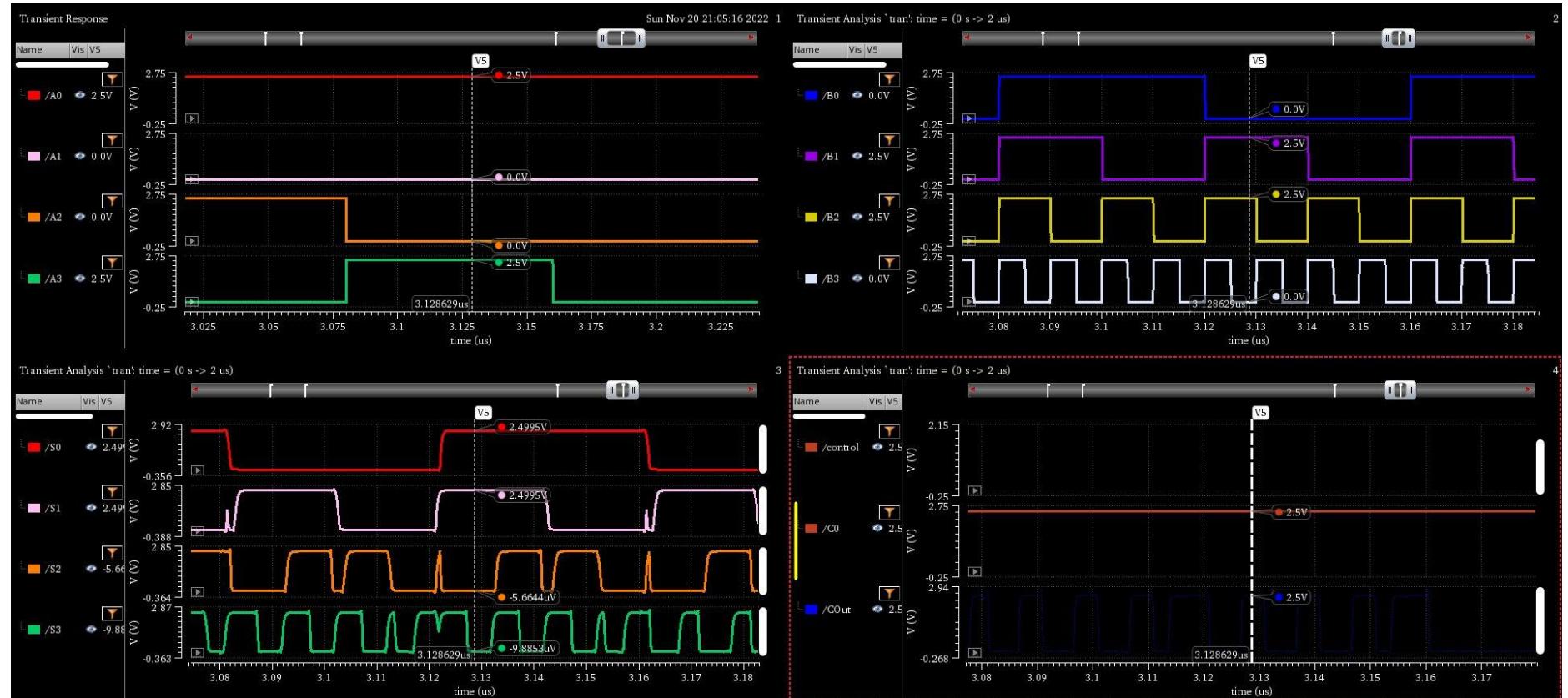


Fig 29. $9-6 = 3$ simulation (layout)

$$15+1 = 16:$$

$$1110 + 0001 = 1111 \text{ Cout} = 0$$

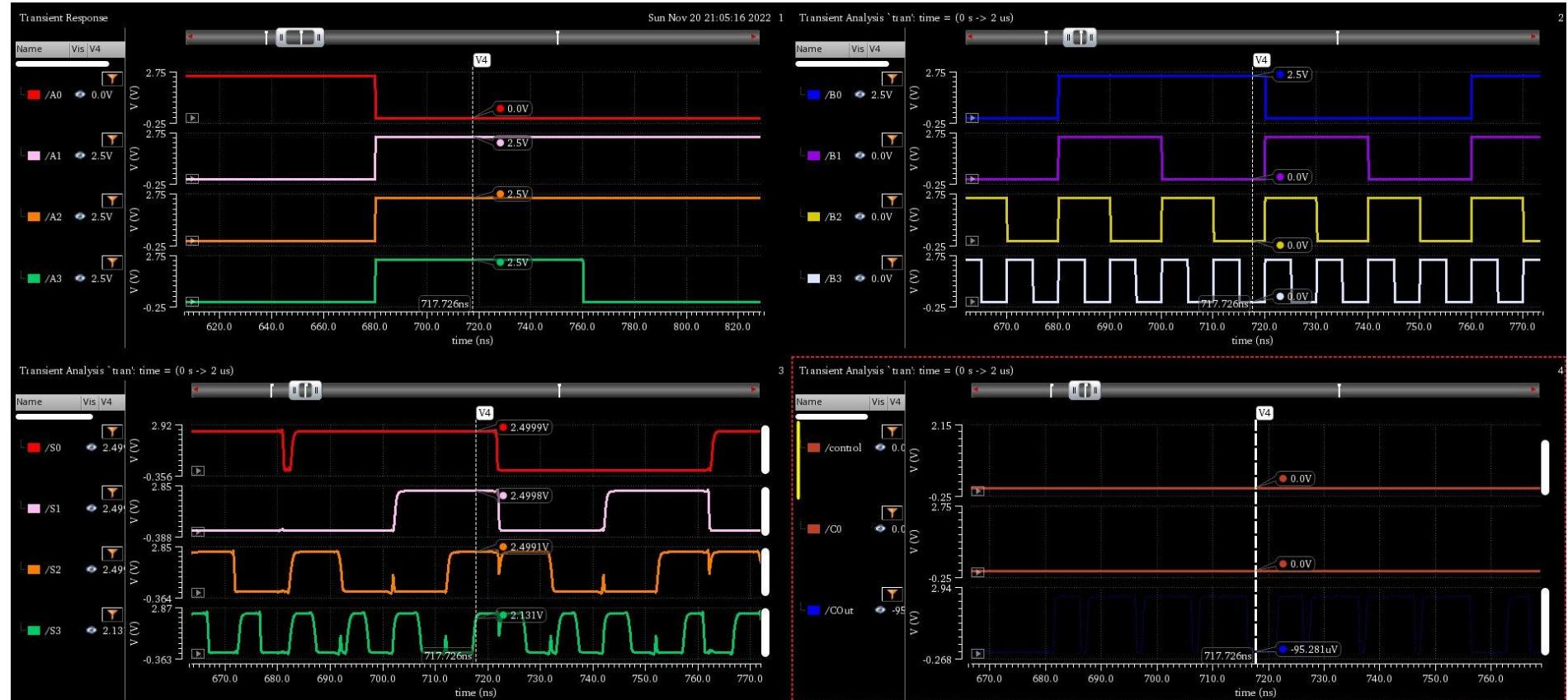


Fig 30. $15+1 = 16$ simulation (layout)

$$15+15 = 30:$$

$$1110 + 1110 = 0011 \text{ Cout} = 1$$

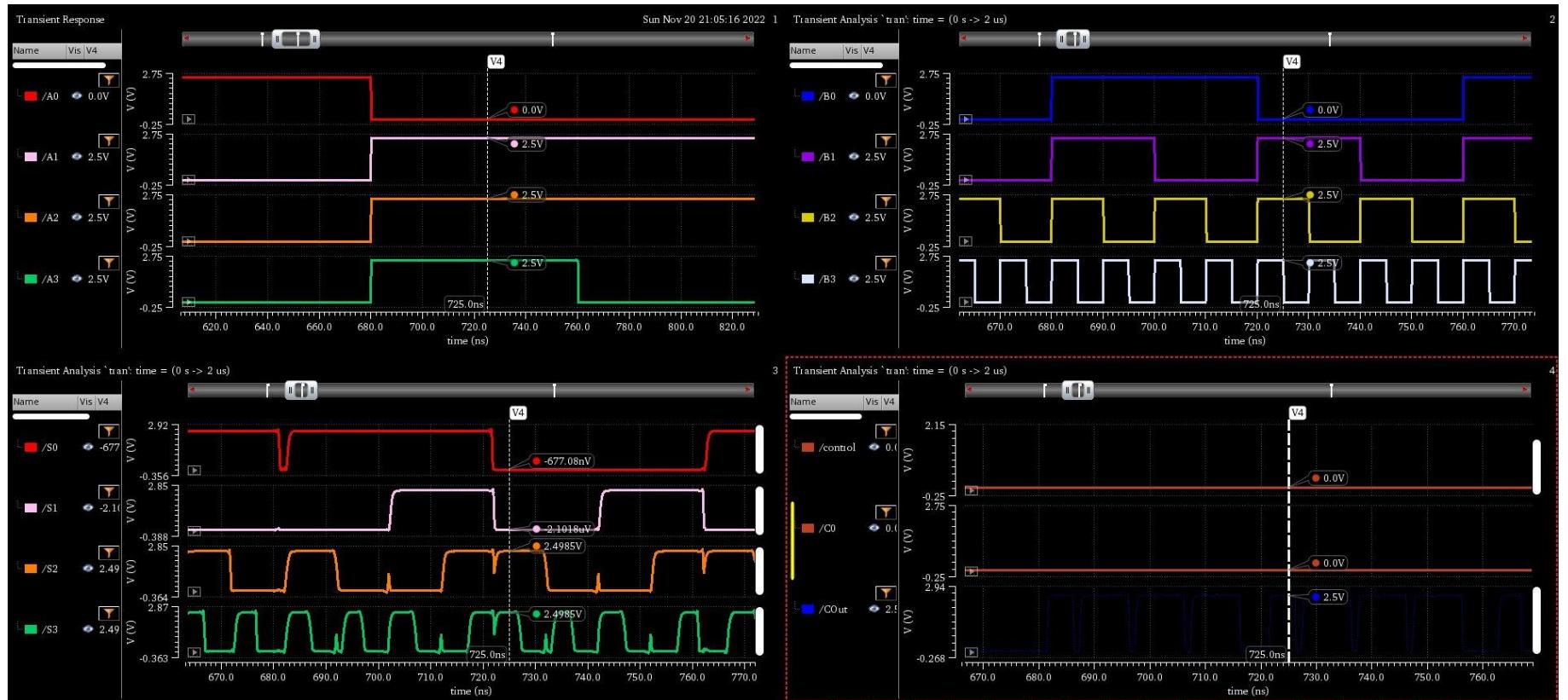


Fig 31. $15+15 = 30$ simulation (layout)

$$15-9 = 6:$$

$$1110 - 1001 = 0110 \text{ Cout} = 1$$

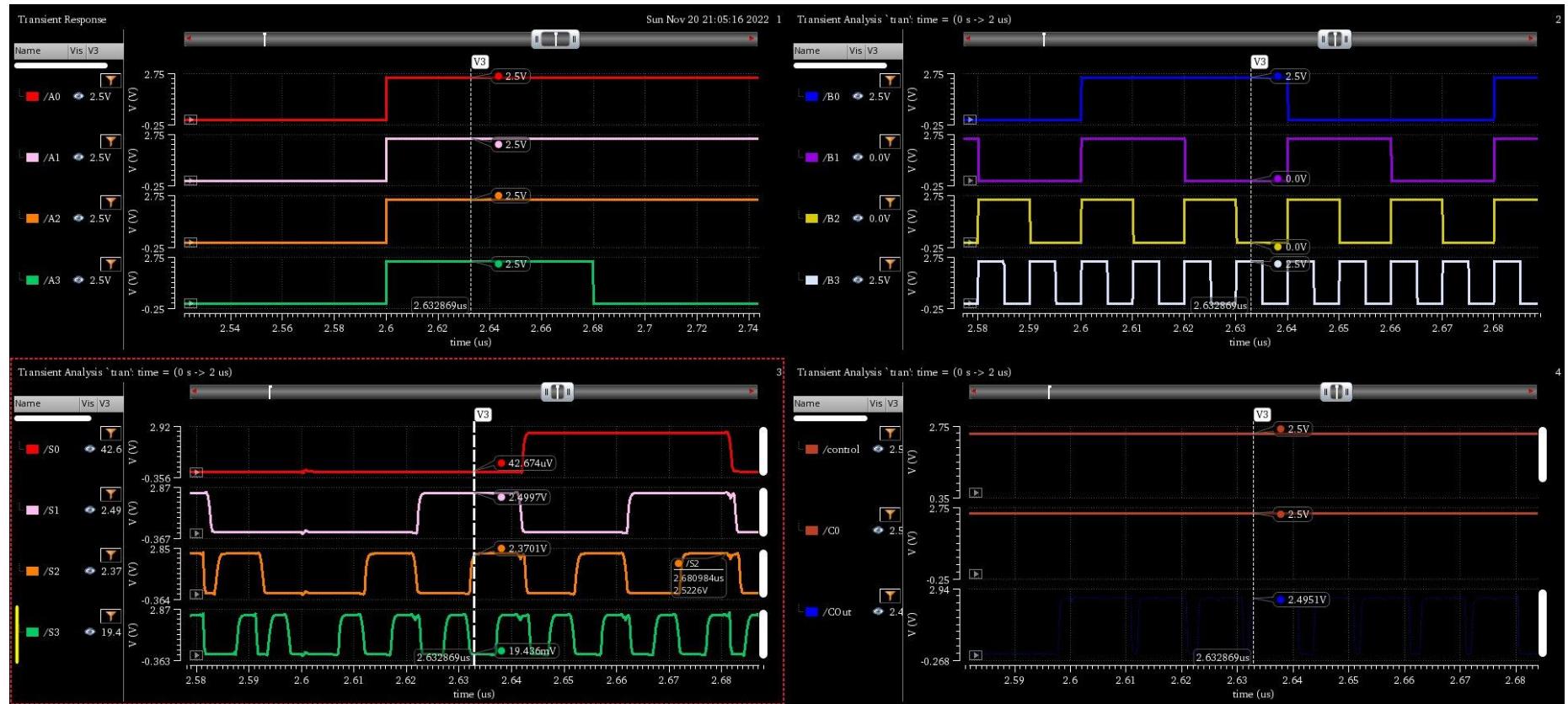


Fig 32. $15-9 = 6$ simulation (layout)

The reason we chose to display the results like this rather than using the print function is that this way we can display all the values in one image. In all four sections, the vertical line is at the exact same time stamp, so we know that is the correct correlating result of the inputs and outputs.

Conclusion:

In this lab, the schematic layout for an XOR and NAND gate were used to make a one-bit adder/subtractor's schematic and layout. The one-bit adder/subtractor schematic and layout and the XOR schematic and layout were then used to make the 4-bit adder/subtractor layout. In the design of the 4-bit adder/subtractor, we used XOR gates at the input of B and an additional control signal to create a two's complement for subtraction. The most difficult part of this lab was getting the layouts and the schematics to match in LVS, however, once the gates passed LVS, combining their layouts was simpler than we initially thought it would be. The 4-bit adder/subtractor was tested against the values provided for testing. For the 4-bit adder/subtractor layout, the simulator is slightly noisier due to the extracted capacitances. These steps were built on from lecture notes [1], the lab given to us [4], and this guide from GeeksforGeeks [3].

Bibliography:

- [1] Maqsood A. Chaudhry (2022), “Dynamic CMOS”
- [2] [Cadence Layout Tips](#)
- [3] [4-bit Binary Adder/Subtractor](#)
- [4] [1-bit Adder Lab Given](#)