UCI Fall 2022

EECS 119

Project # 1

CMOS Inverter and Oscillator

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Introduction:

There are five steps to this project:

- Calculating the DC transfer characteristic waveform (Vout vs Vin) from a CMOS inverter schematic that is generated at varying PMOS widths
- Create an inverter to where NMH=NML and VM= VDD/2
- Calculating noise margins and propagation delay time of the layout of the CMOS
- Generate the transient waveforms of Vin and Vout for three different pulse frequencies of both the schematic and layout
- Design an oscillator using 5 CMOS inverters

The goal of this project is to visualize and better understand how the ratio between the width and length ratio of the transistors of a CMOS inverter. Additionally, this project will compare the frequency of the designed oscillator's signal to the expected frequency from the propagation delay of the CMOS inverter calculated in the third step.

Theory:

A CMOS inverted is meant to output V_{DD} at $V_{in} = 0$ and 0 at $V_{in} = V_{DD}$. It is made up of a PMOS and an NMOS. By manipulating the width and length ratio between the two transistors, we can affect the performance of CMOS. If we optimize the ratio, we maximize the noise margins and obtain symmetrical characteristics.[1] The propagation delay is also looked at in this lab. This is affected by the internal capacitance of the CMOS, C_L. Reducing C_L would reduce propagation delay.[1] We started with an NMOS width of 720 nm because part d) calls for setting the PMOS width to half of the NMOS width. The minimum width can be is 360 nm.

We then build an oscillator with the inverters we made. An odd-number oscillator can be used to understand how the number of inverters in series can affect the frequency of the circuit.[2]

$F = 1/((t_{pLH} + t_{pHL}) * n)$, n being the number of inverters

We followed the steps shown in the discussion to build all the circuits and layouts in this lab. If there were things we couldn't find in the course material, we found it online. Mostly just how to use Cadence to find certain values and setting up ADE L for simulating the layouts. [4]

Design:

CMOS Inverter Schematic:

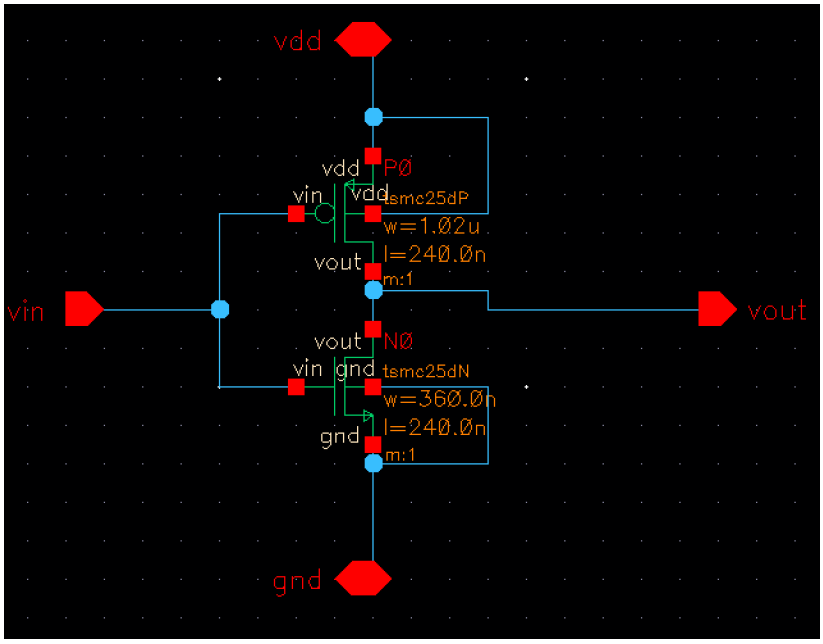


Figure 1: CMOS inverter schematic
NMOS width = 360nm, length = 240nm
PMOS width = 1.02um, length = 240nm

Inverter circuit with inverter symbol:

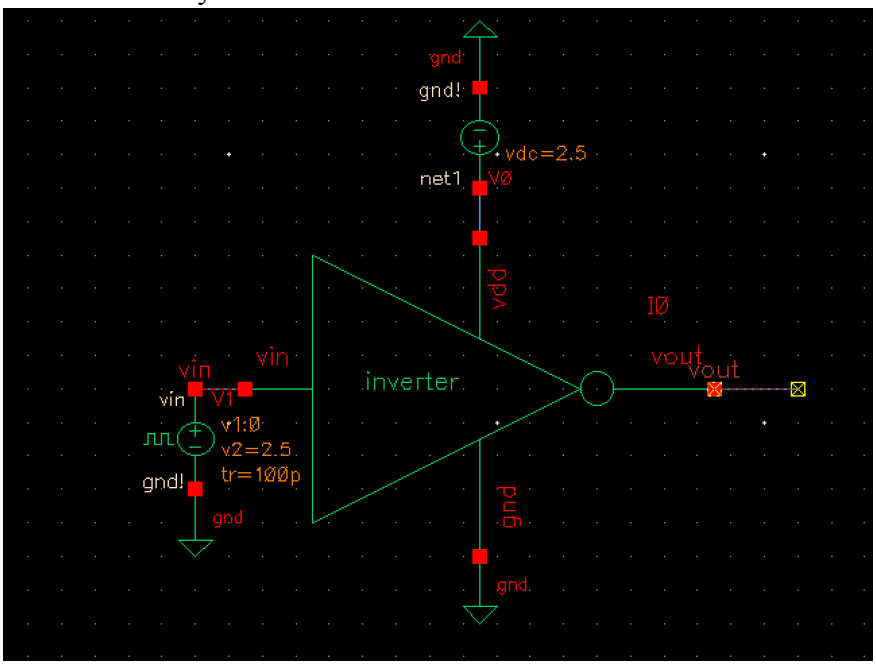


Figure 2: CMOS inverter circuit

Inverter Oscillator (schematic):

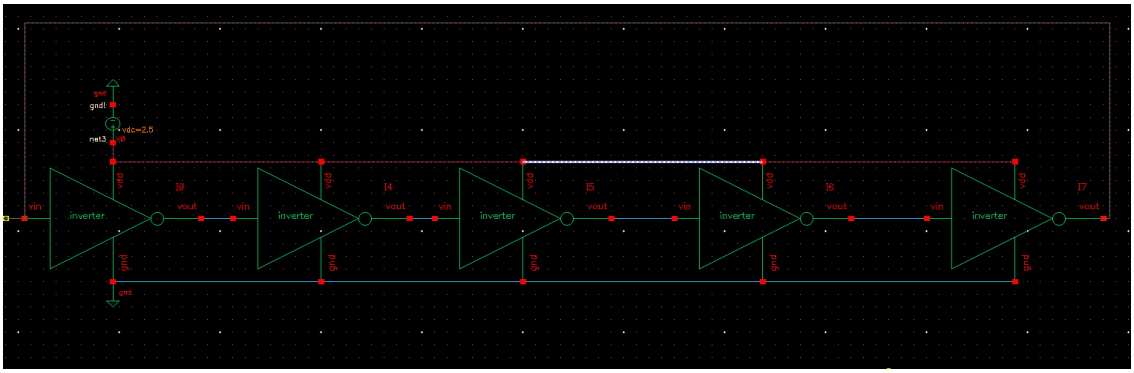


Figure 3: CMOS inverter oscillator circuit (schematic)

Inverter Oscillator (layout):

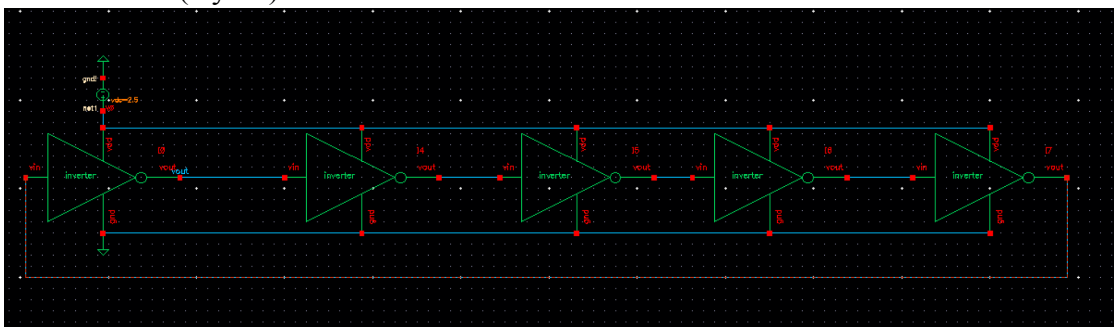


Figure 4: CMOS inverter oscillator circuit (layout)

Results:

1. Width Factor
   Width Factor ($Width_{NMOS}$ = 720nm)
   a. $Width_{PMOS}$ = $Width_{NMOS}$ = 720 nm:

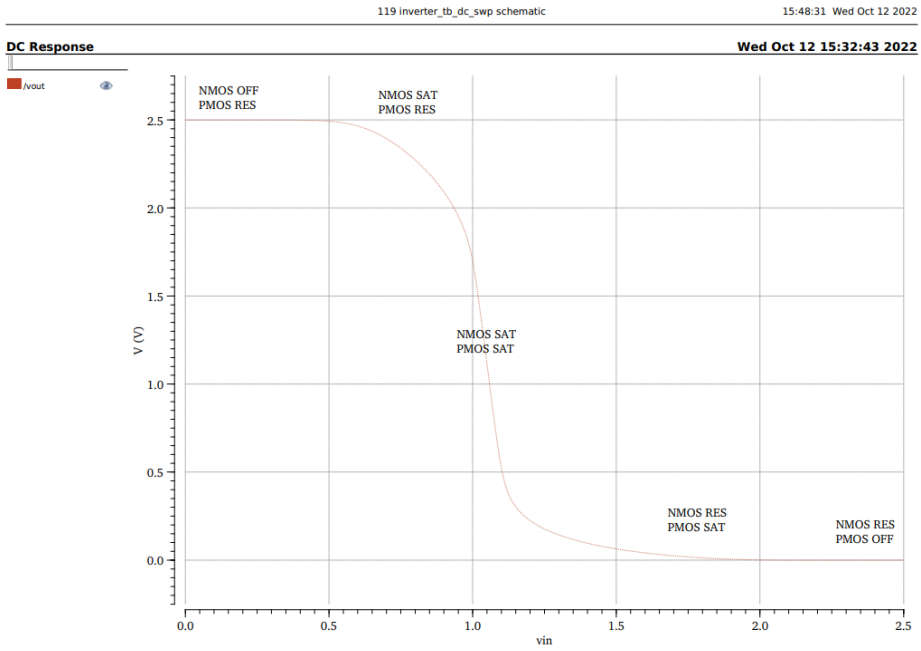


Figure 5: CMOS inverter $Width_{PMOS}$ = $Width_{NMOS}$ = 720 nm VTC plot with operating regions of the transistors

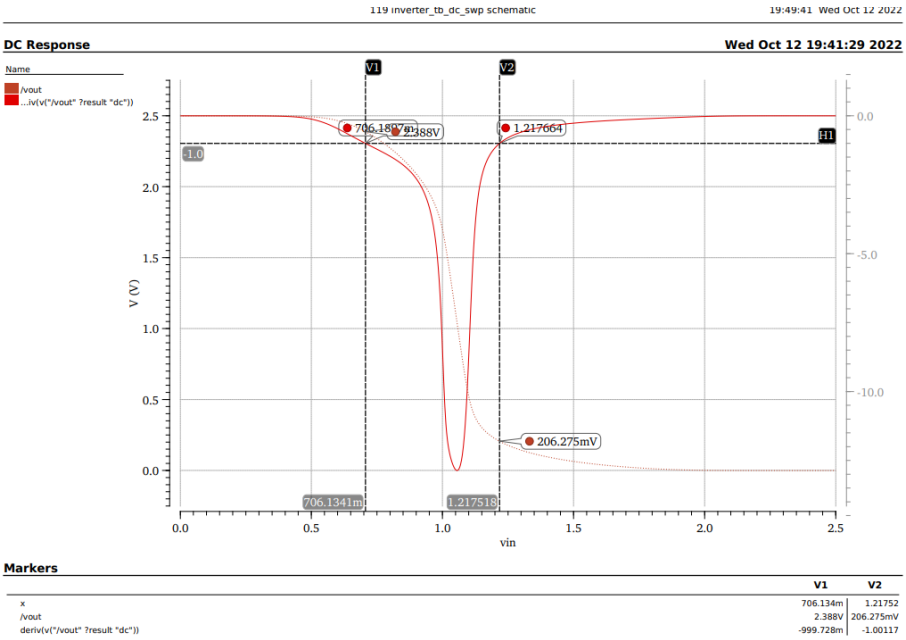


Figure 6: CMOS inverter $Width_{PMOS}$ = $Width_{NMOS}$ = 720 nm VTC plot with

derivative calculation
V_{IL} = 706.134 mV, V_{IH} = 1.22 V found at dV_{out}/dV_{in} = -1
$NM_H = V_{DD} - V_{IH}$ = 2.5 - 1.22 V = 1.28 V
$NM_L = V_{IL}$ - GND = 706.134 mV

b. $Width_{PMOS} = 3 * Width_{NMOS}$ = 2160 nm = 2.16 um:

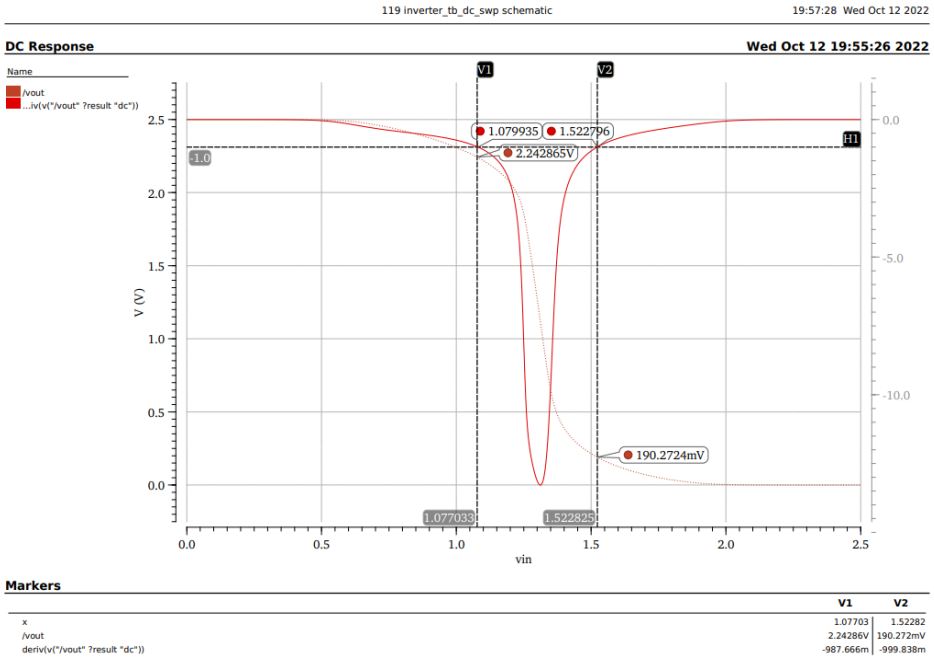


Figure 7: CMOS inverter $Width_{PMOS} = 3 * Width_{NMOS}$ = 2160 nm = 2.16 um VTC plot with derivative calculation
V_{IL} = 1.077 V, V_{IH} = 1.52 V
$NM_H = V_{DD} - V_{IH}$ = 2.5 - 1.52 = .98 V
$NM_L = V_{IL}$ - GND = 1.077 V

c. $Width_{PMOS} = 5 * Width_{NMOS} = 3600$ nm = 3.6 um:

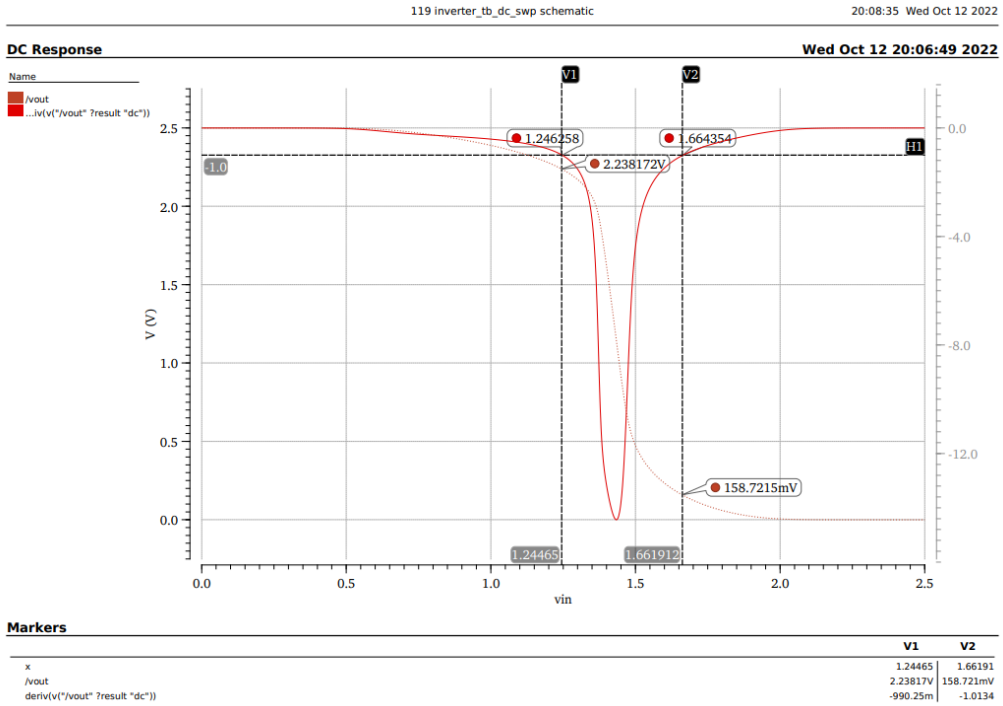


Figure 8: CMOS inverter $Width_{PMOS} = 5 * Width_{NMOS} = 3600$ nm = 3.6 um VTC plot with derivative calculation

$V_{IL} = 1.245$ V, $V_{IH} = 1.66$ V

$NM_H = V_{DD} - V_{IH} = 2.5 - 1.66 = .84$ V

$NM_L = V_{IL} - GND = 1.245$ V

d. $Width_{PMOS} = 0.5 * Width_{NMOS} = 360$ nm:

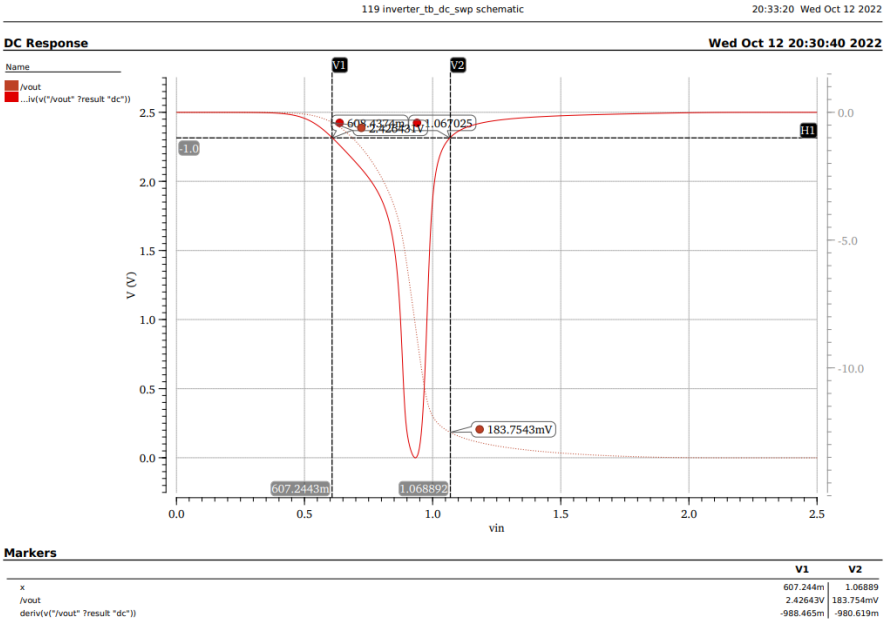


Figure 9: CMOS inverter $Width_{PMOS} = 0.5 * Width_{NMOS} = 360$nm VTC plot with derivative calculation

V_{IL} = 607.244 mV, V_{IH} = 1.07 V
$NM_H = V_{DD} - V_{IH} = 2.5 - 1.07 = 1.43$ V
$NM_L = V_{IL} - GND = 607.244$ mV

2. LVS:
   a.

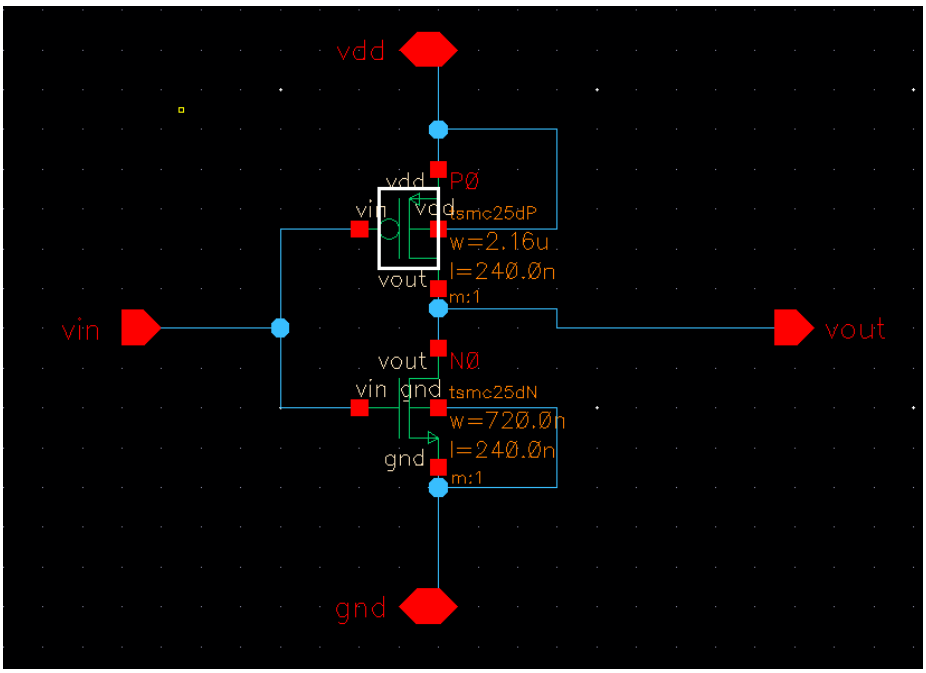


Figure 10: Schematic for an inverter with NM_L closest to NM_H, $Width_{PMOS}$ = 3 * $Width_{NMOS}$ = 2160 nm = 2.16 um, NMH = VDD - VIH = 2.5 - 1.52 = .98 V
NML = VIL - GND = 1.077 V

b.

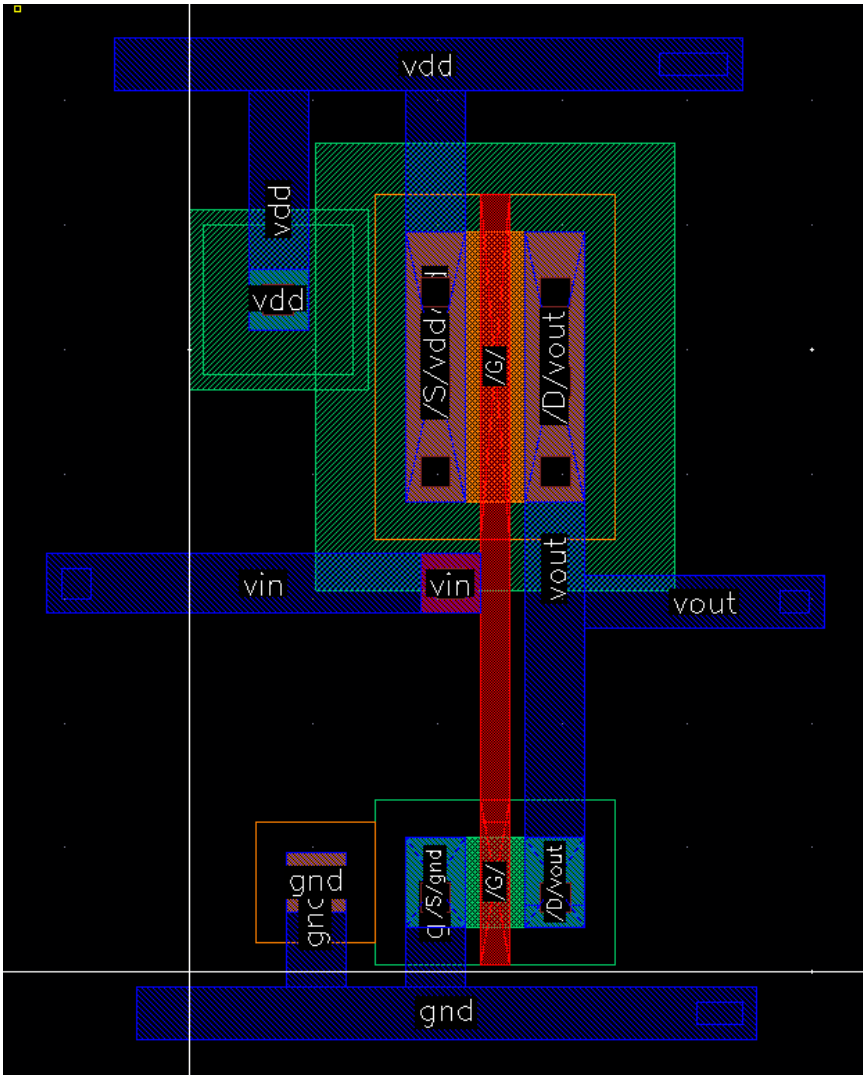


Figure 11: Layout for an inverter with NM_L closest to NM_H, $Width_{PMOS}$ = 3 * $Width_{NMOS}$ = 2160 nm = 2.16 um, NMH = VDD - VIH = 2.5 - 1.52 = .98 V
NML = VIL - GND = 1.077 V

c.

```
@(#)$CDS: LVS version 6.1.8-64b 09/22/2020 18:59 (sjfhw316) $

Command line: /ecelib/eceware/cadence/ic618/tools.lnx86/dfII/bin/64bit/LVS -dir /users/ugrad/2020/spring/taleba/eecs119/Caden
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /users/ugrad/2020/spring/taleba/eecs119/Cadence6/LVS/layout/netlist
       count
         4               nets
         4               terminals
         1               pmos
         1               nmos

    Net-list summary for /users/ugrad/2020/spring/taleba/eecs119/Cadence6/LVS/schematic/netlist
       count
         4               nets
         4               terminals
         1               pmos
         1               nmos


    Terminal correspondence points
    N2          N1          gnd
    N0          N3          vdd
    N3          N0          vin
    N1          N2          vout

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  2       2
        total                   2       2

                                  nets
        un-matched              0       0
```

The net-lists match.

	layout instances	schematic instances
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	4	4
total	4	4
	terminals	
un-matched	0	0
matched but different type	2	2
total	4	4

Figure 12: LVS Report for Layout and schematic for an inverter with NM_L closest to NM_H, it shows that the net lists match

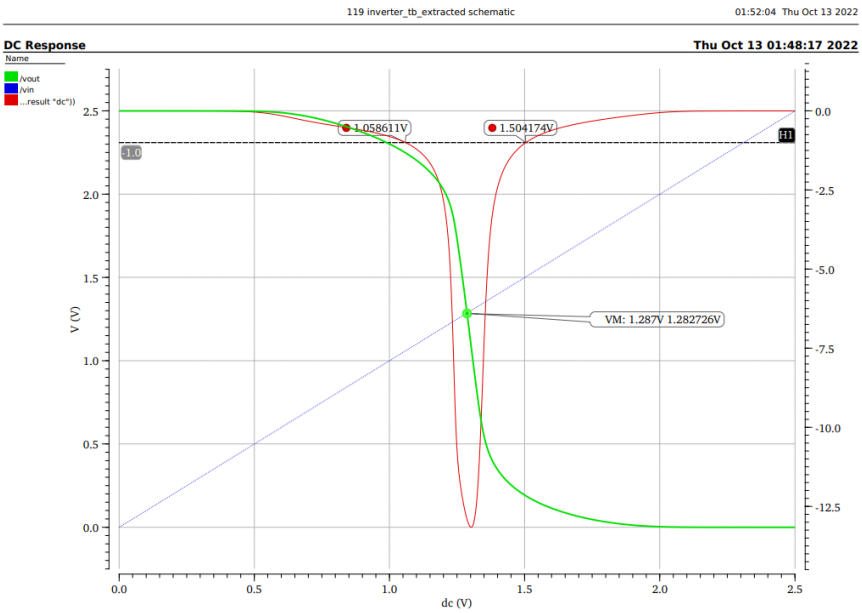


Figure 13: VTC plot of the layout

3. Noise Margin and Propagation Delay
   V_{IL} = 1.077 V, V_{IH} = 1.52 V
   $NM_H = V_{DD} - V_{IH} = 2.5 - 1.52 = .98$ V
   $NM_L = V_{IL} - GND = 1.077$ V

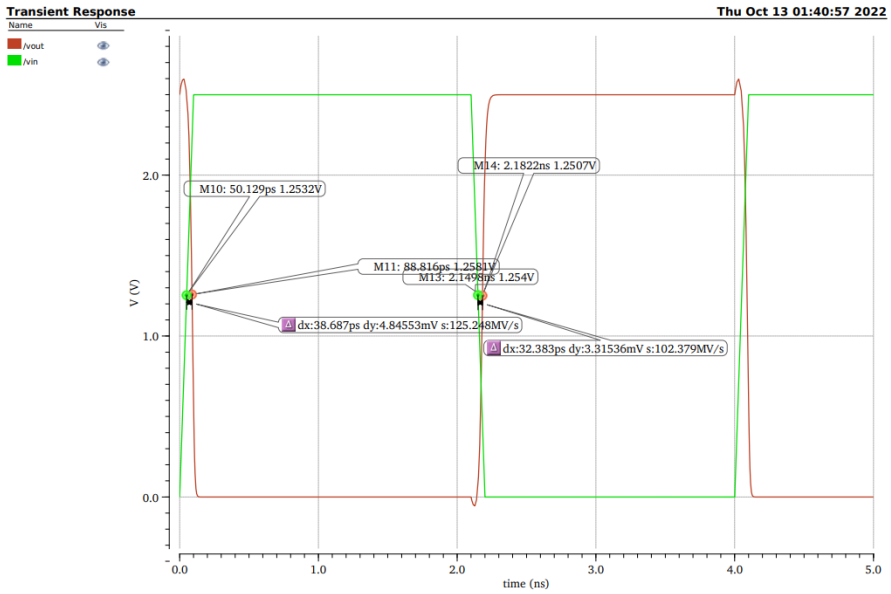


Figure 14: Transient Response of the layout of the inverter, showing the t_p calculated graphically by finding the difference between the rising and falling edges at Vdd/2,
t_p = (38.687ps + 32.383ps)/2 = 35.535ps

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	vout		☑	☐	allv
2	vin		☑	☐	allv
3	tphl	32.21p	☑	☐	
4	tplh	38.95p	☑	☐	

Figure 15: Transient Response of the layout of the inverter, found by using the calculator in ADE L
$t_P = (t_{phl} + t_{plh})/2 = (32.21ps + 38.95ps)/2 = 35.58ps$
$F = 1/((t_{phl} + t_{plh}) * n) = 1/(71.16ps * 1 \text{ inverter}) = 14.05$ GHz

4. Transient
   a.

i. 500 MHz:

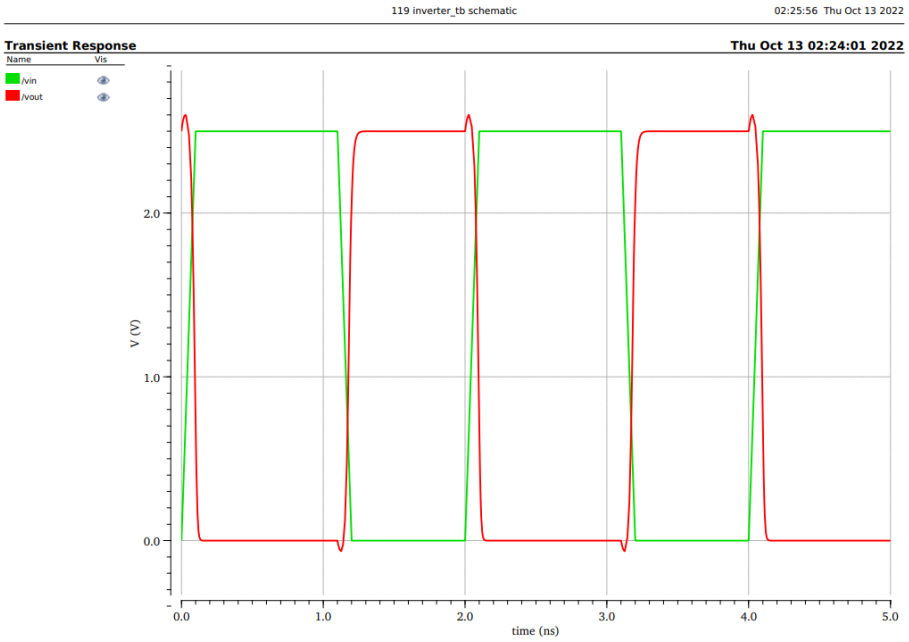


Figure 16: Schematic transient response at 500 MHz

ii. 5 GHz:

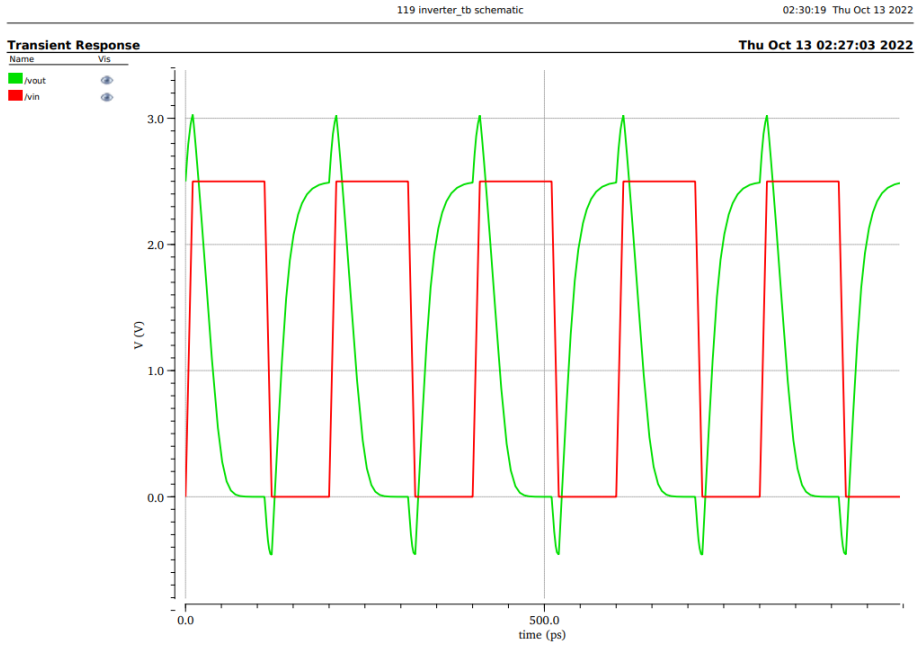


Figure 17: Schematic transient response at 5 GHz

iii. 50 GHz:

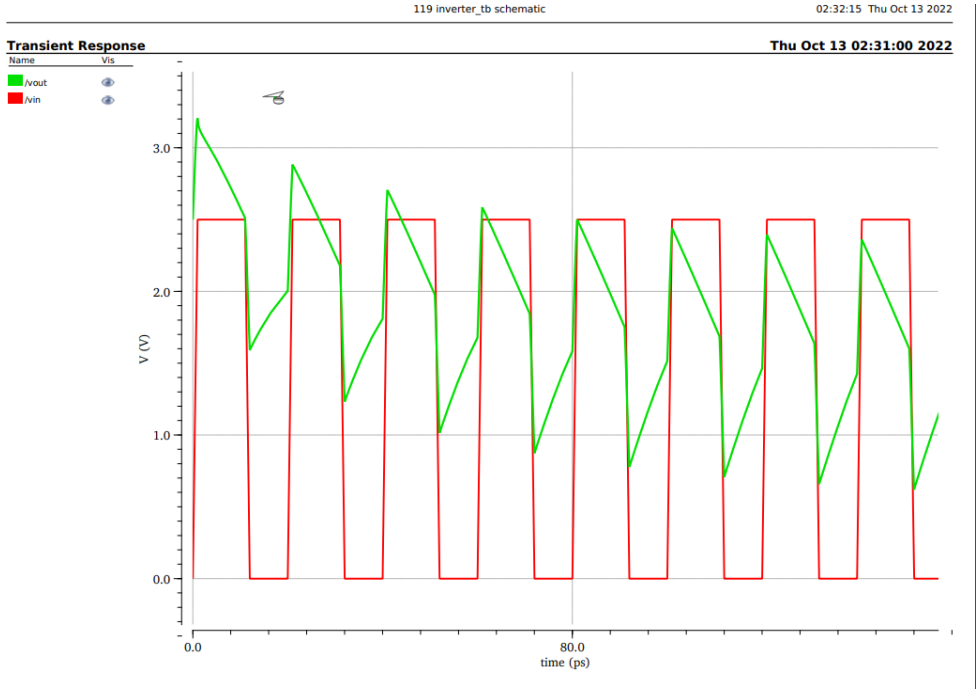


Figure 18: Schematic transient response at 50 GHz

b.

i. 500 MHz:

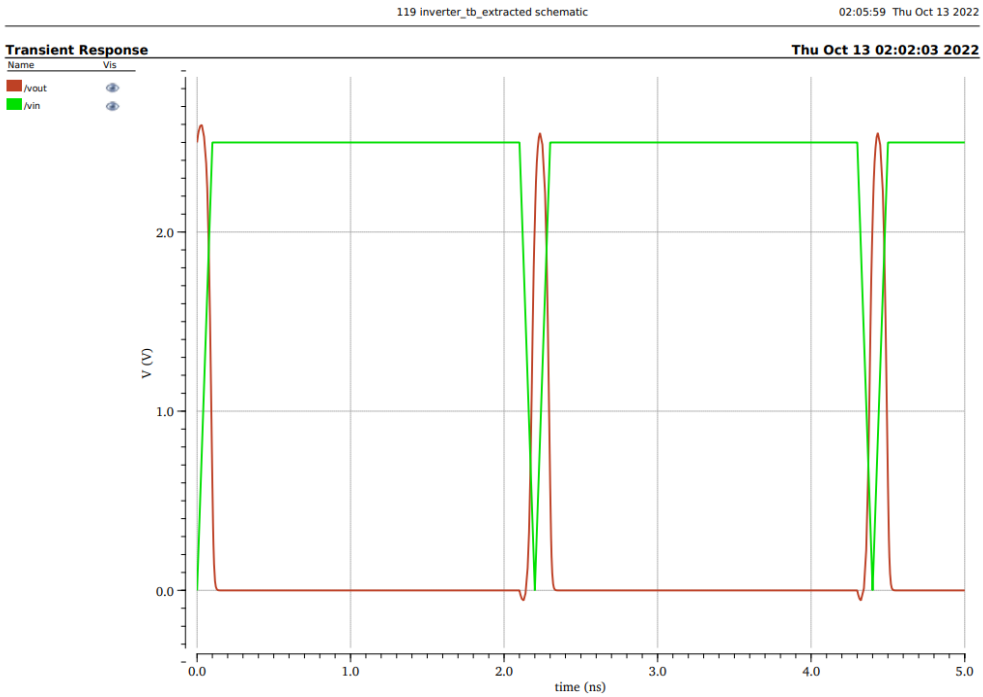


Figure 19: Layout transient response at 500 MHz

ii. 5 GHz:

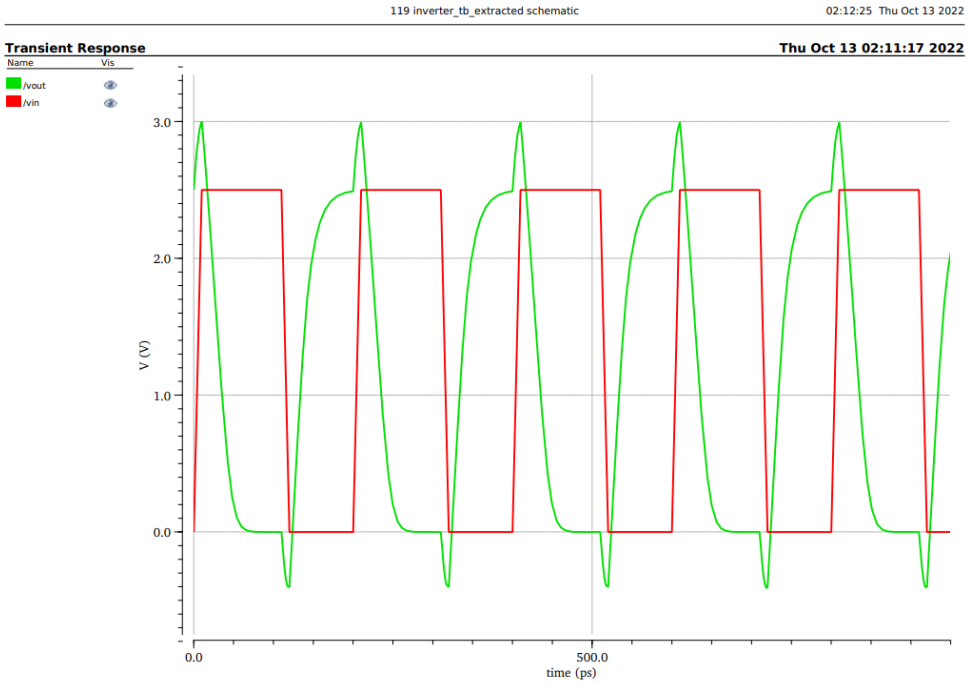


Figure 20: Layout transient response at 5 GHz

iii. 50 GHz:

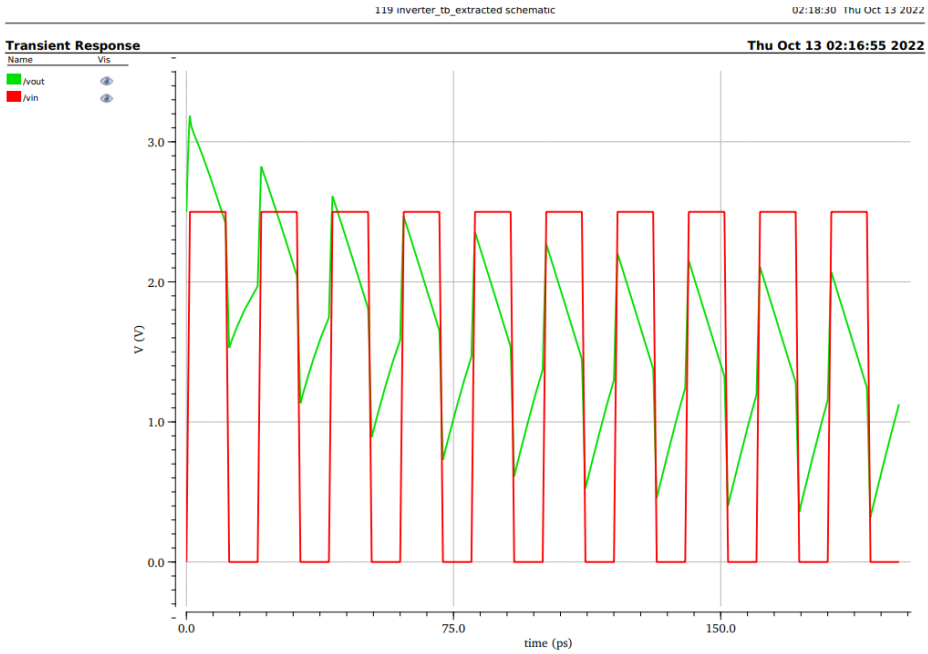


Figure 21: Layout transient response at 50 GHz
As the frequency increases, the wavelength of the Vout decreases, and the slew rate of the output is skewed.

5. Oscillator
   a. Schematic:

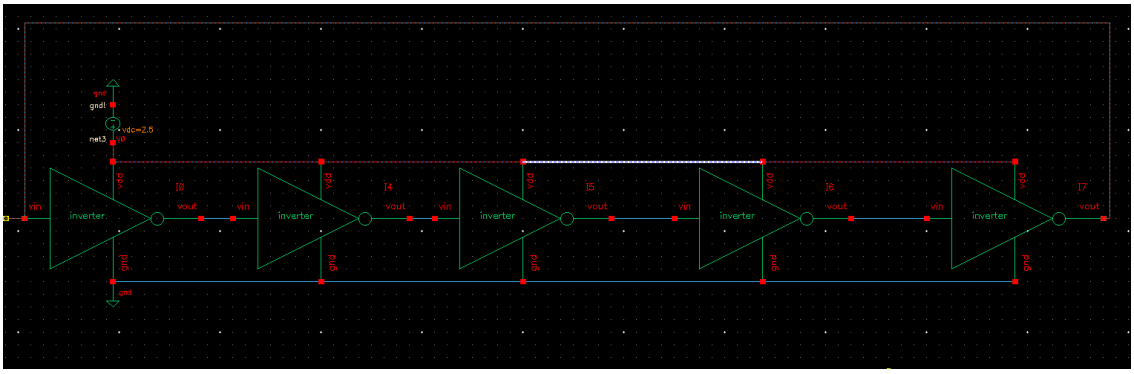


Figure 22: CMOS inverter oscillator circuit (schematic)
Waveform:

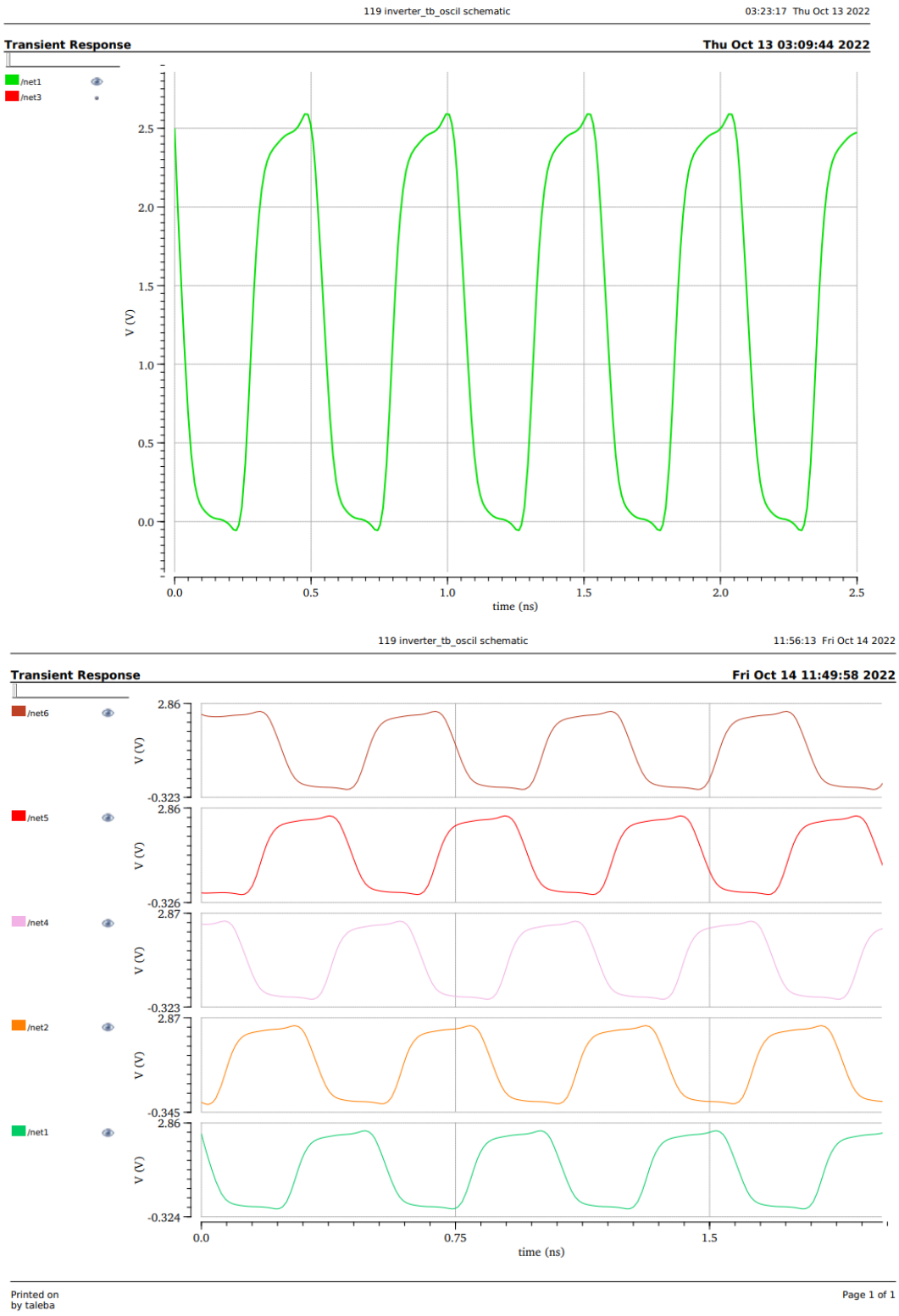


Figure 23: CMOS inverter oscillator transient response and each node's output

freq(v("/net1" ?result "tran") "rising...

	time (s)	req(v("/...0.0) (Hz
1	283.7E-12	1.931E9
2	801.5E-12	1.931E9
3	1.319E-9	1.931E9
4	1.837E-9	1.931E9

Figure 24: CMOS inverter oscillator frequency, measured using the calculator in ADE L

b. Layout

i. Schematic:

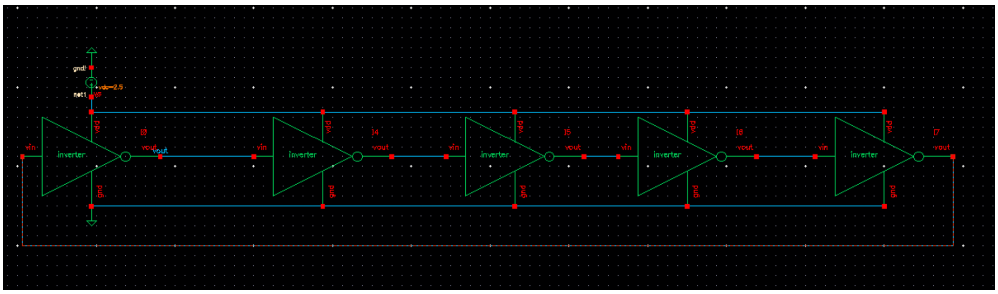
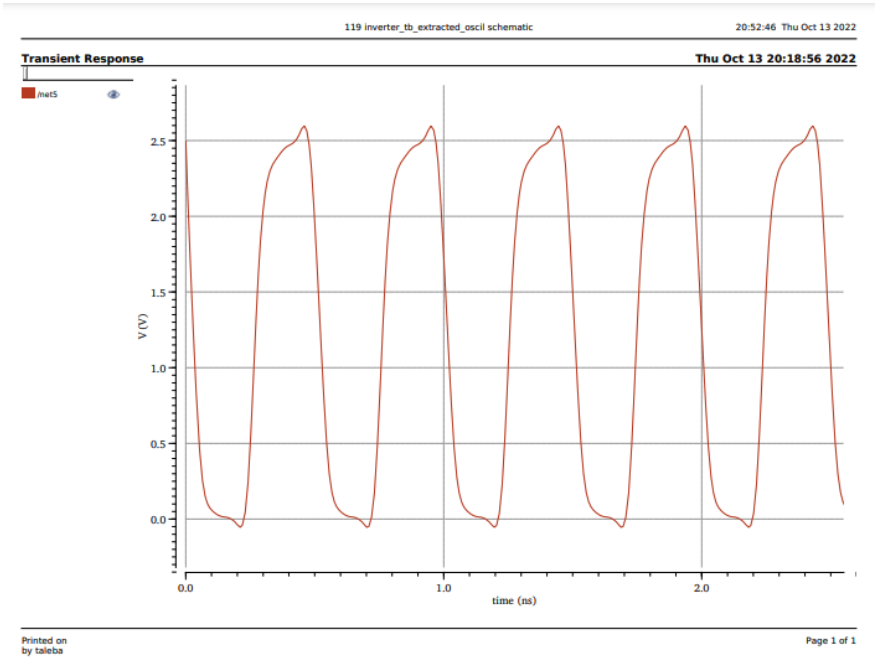


Figure 25: CMOS inverter oscillator circuit (layout)

ii. Waveform:



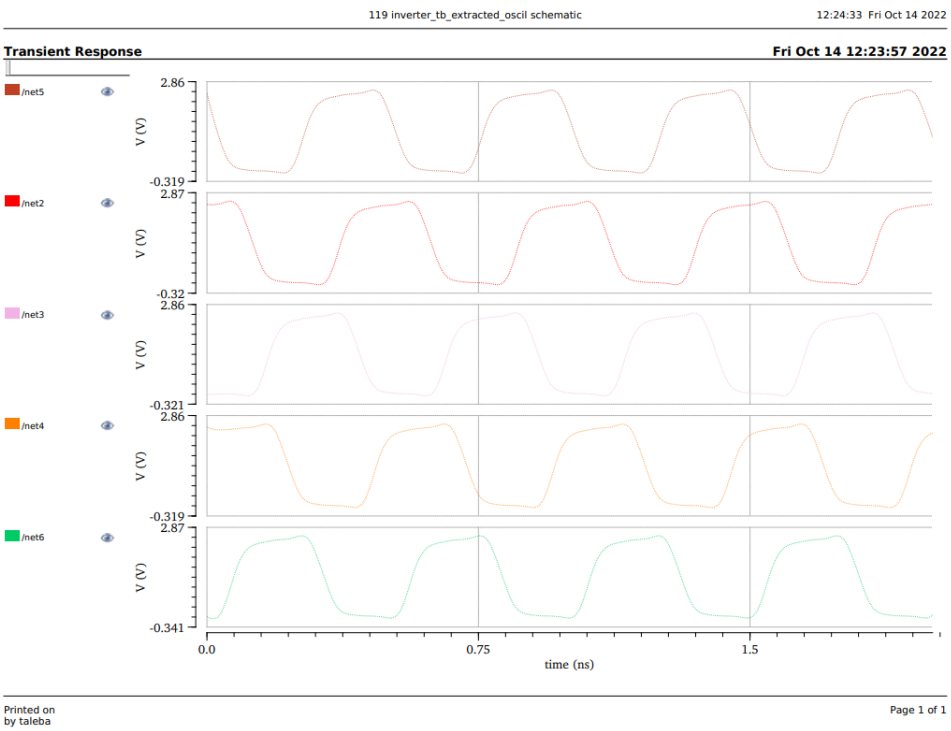


Figure 26: CMOS inverter oscillator (layout) transient response and each node's output

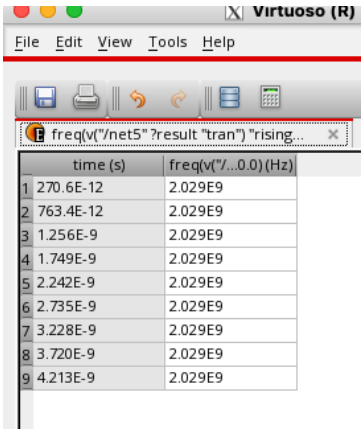


Figure 26: CMOS inverter oscillator (layout) frequency measured using the calculator in ADE L

$$F = \frac{1}{\left(tp_{LH} + tp_{HL}\right) \times n}$$

Frequency is inversely proportional to the number of stages and the propagation delay times. If we look at the period, which is about 2.2 ns, of the transient response in part three, we can find that the frequency is 14.05 GHz. From part 3 we can see that the expected frequency is F = $1/((t_{phl} + t_{plh}) * n)$ = 1/(71.16ps * 5 inverters) = 2.81 GHz, about what we got.

Conclusion:

In this lab, we got an overview of Cadence by making and manipulating a CMOS inverter in different ways and with different circuits. We show how changing the width of the PMOS affects the output of the CMOS inverter. By looking at the transient response of the inverter with NM_H and NM_L close we were able to calculate the propagation delay of the inverter. After analyzing the inverter at different higher frequencies we find that as the frequency increases the wavelength of the Vout decreases, and the slew rate of the output is skewed. This delay helped us understand the performance of the inverter as we put more in series to create an oscillator. The more inverters in series the slower the frequency would be.

Bibliography:

[1] Maqsood A. Chaudhry (2022), "CMOS Inverter"

[2] "Wiki." *Activity: CMOS Inverter Ring Oscillator [Analog Devices Wiki]*, https://wiki.analog.com/university/courses/alm1k/alm-lab-ring-osc.

[3] "Propagation Delay of CMOS Inverter." *VLSI System Design*, https://www.vlsisystemdesign.com/propagation-delay-of-cmos-inverter/.

[4] "Post Layout Simulation." *University of Texas at El Paso - Ece Dept. - VLSI Cadence: Post Layout Simulation*, University of Texas at El Paso, http://www.ece.utep.edu/courses/vlsi/Fall/cadence/pls.html.

[5] Mohammad Wahiduzzaman Khan "Cadence Setup"