UNITED INTERNATIONAL UNIVERSITY

Department of Electrical and Electronic Engineering

EEE 4122: VLSI Design Lab

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Project Report

Submitted by

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Submitted To

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Design of a 4-bit Arithmetic Logic Unit (ALU) with inputs A, B (4-bits each) and SEL (2-bits). The inputs are loaded into registers first and the output is saved into 4-bit registers.

Abstract

This project report presents the design of a 4-bit Arithmetic Logic Unit (ALU) on Cadence platform using Virtuoso tool. An essential part of digital systems, the ALU can carry out a wide range of arithmetic and logical operations. Two 4-bit inputs, A and B, and a 2-bit selection input (SEL), which chooses the precise operation to be carried out, are used in the ALU design. The final 4-bit result is kept in an output register after the inputs have first been loaded into registers. The Cadence Virtuoso environment is used for the ALU's design, simulation, and validation, guaranteeing accurate transistor-level behavior modeling. The project's primary goal is to develop a fully functional and effective ALU design that can be incorporated into bigger digital systems, such as microprocessors.

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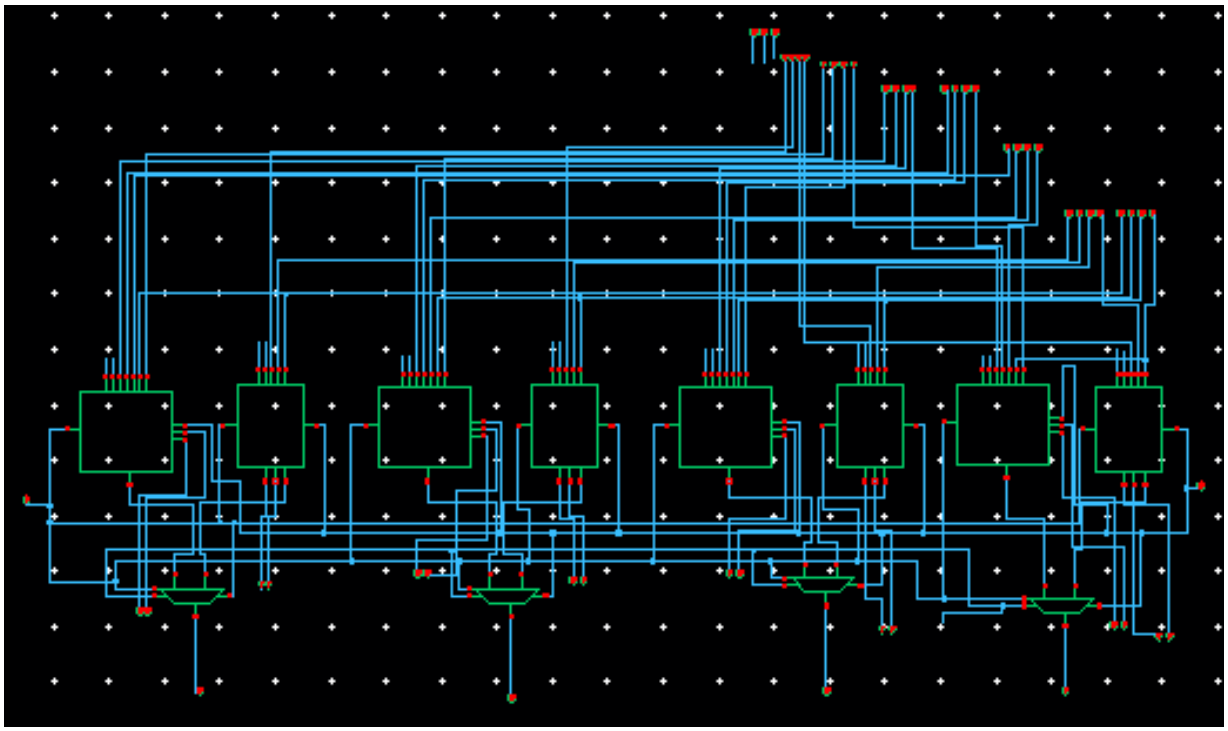
1. Introduction

An Arithmetic Logic Unit (ALU) is a critical building block in digital VLSI design sector, responsible for executing a wide range of arithmetic and logical functions. ALUs are used in processors to perform operations such as addition, subtraction, logical AND, OR, and XOR, among others. The design of an efficient and reliable ALU is essential for the performance of digital systems.

In this project, a 4-bit ALU is designed using the Cadence Virtuoso tool, a widely used platform for integrated circuit design and simulation. The ALU accepts two 4-bit inputs (A and B) and a 2-bit selection input (SEL) that dictates which operation is performed on the inputs. The operations include basic arithmetic (such as addition and subtraction) as well as logical operations. To enhance modularity and control, the inputs are first loaded into registers, and the output is stored in a 4-bit register.

This project aims to demonstrate the entire design process, from the conceptual design and implementation to simulation and verification. This report contains Schematics, outputs compared with the truth table and layouts.

2. 4bit ALU final diagram

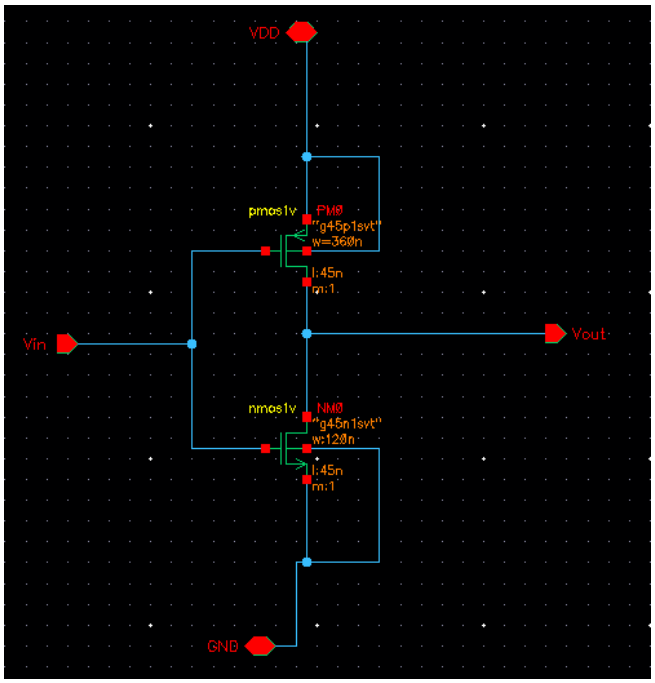


3. Necessary Gates

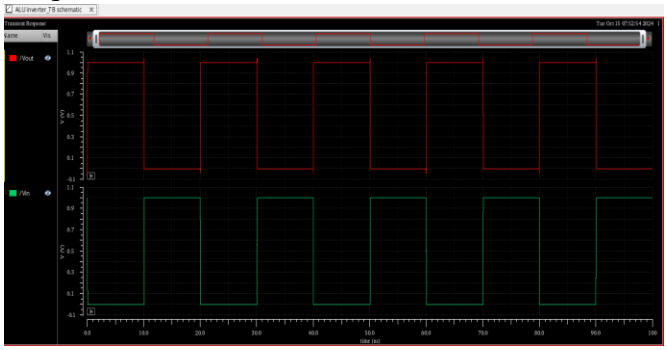
Chap-1

i. Inverter

- ✓ Schematic



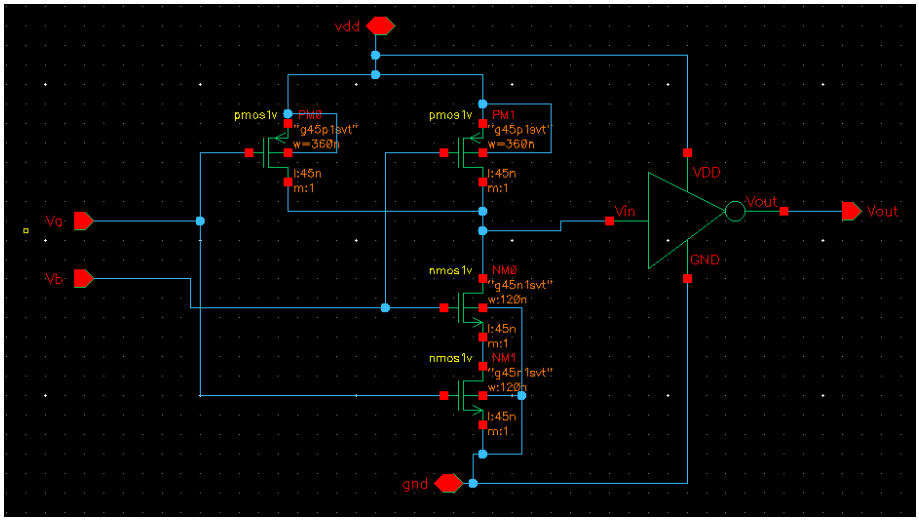
- ✓ Output



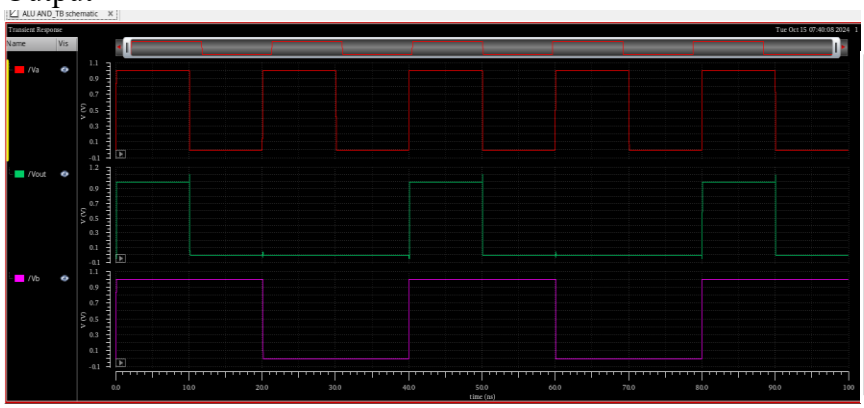
Input	Output
0	1
1	0

ii. AND

✓ Schematic

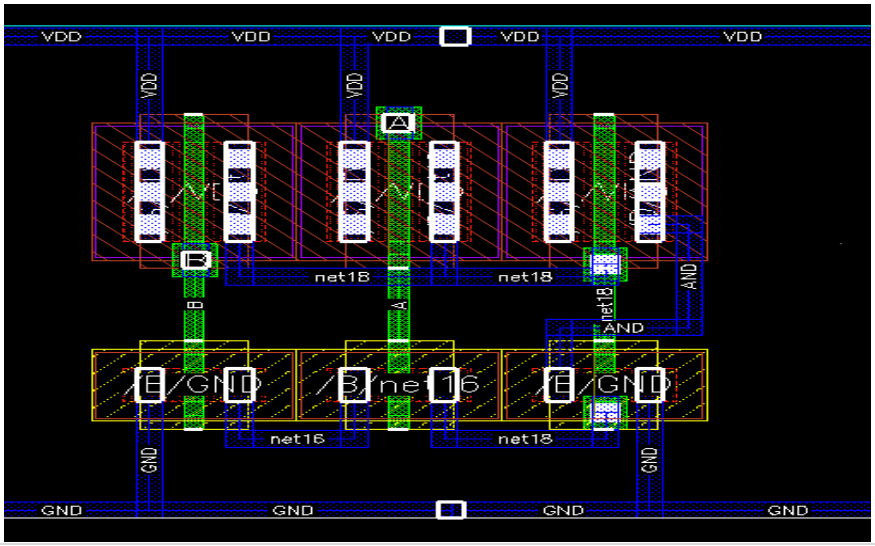


✓ Output



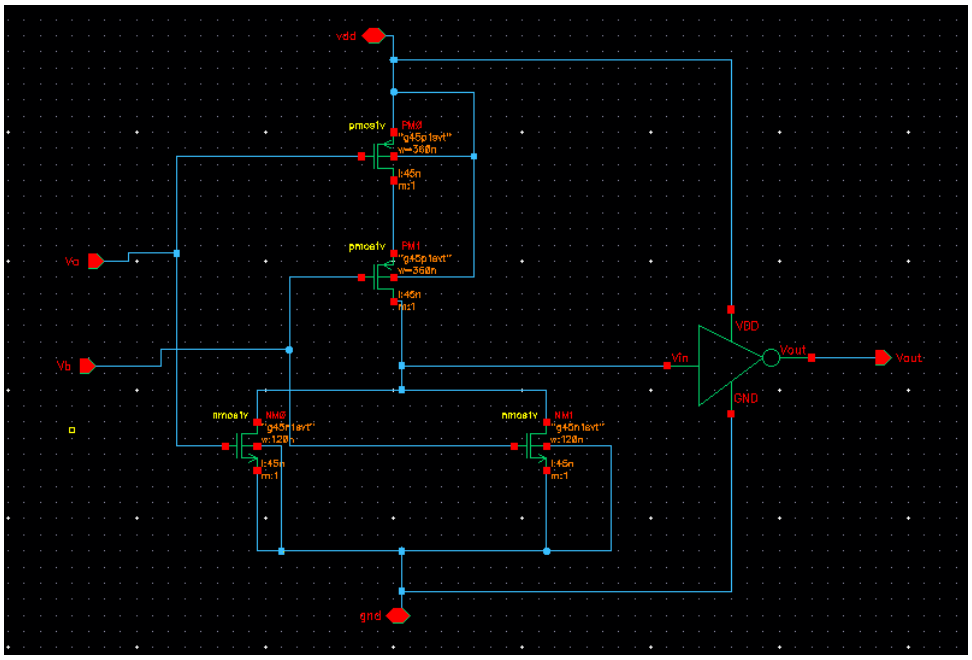
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

✓ Layout



iii. OR

✓ Schematic



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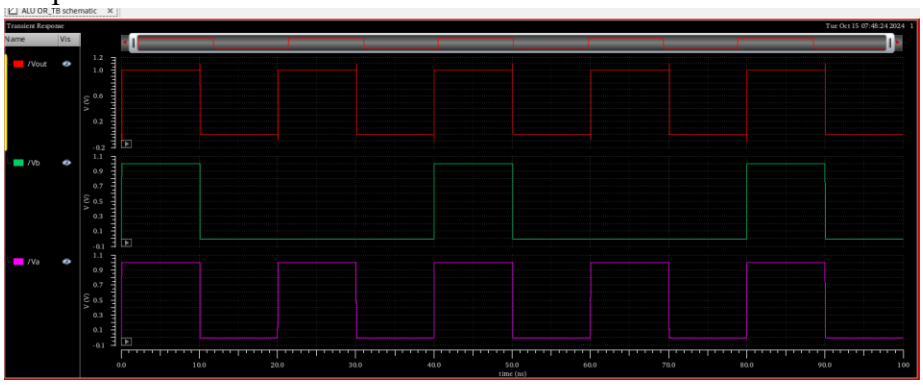
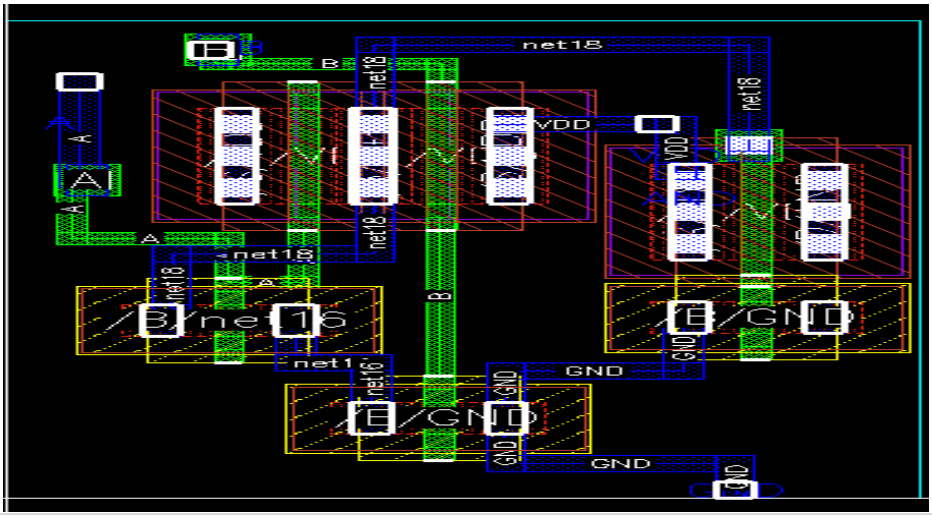


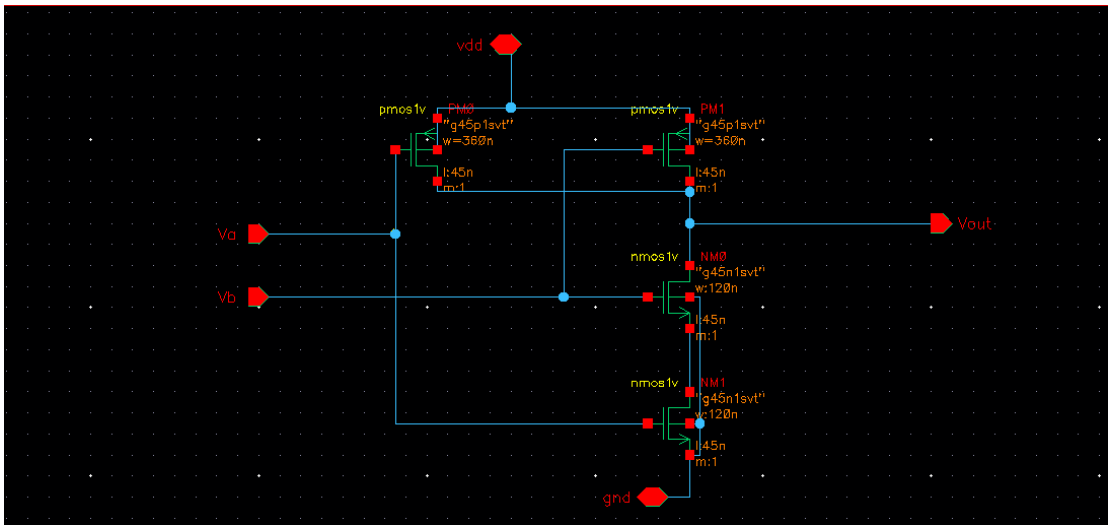
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

✓ Layout



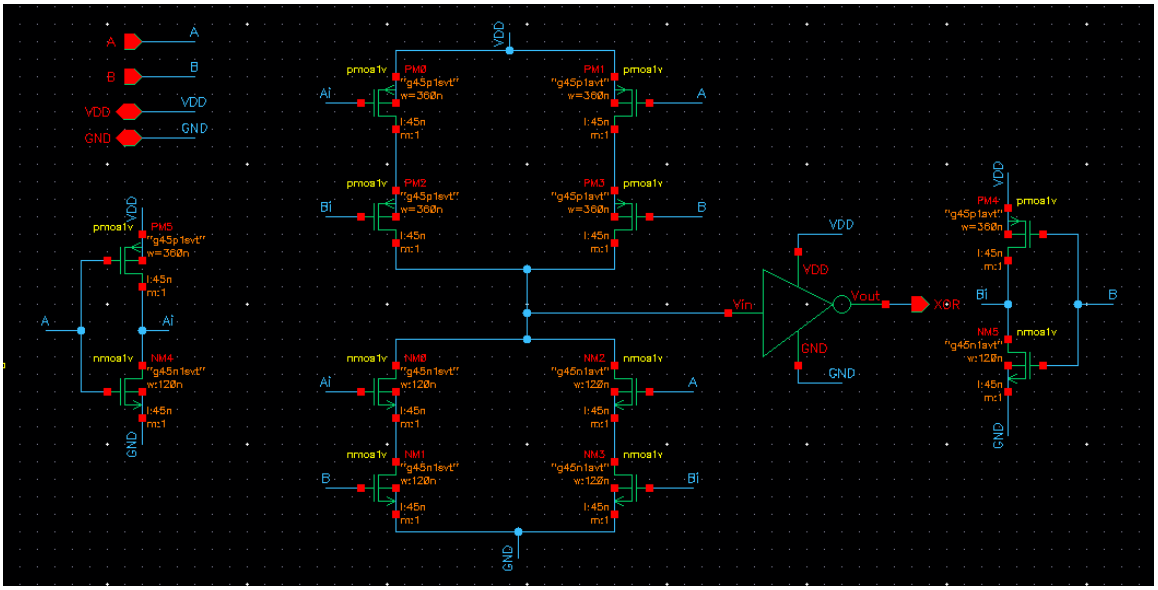
iv. NAND

✓ Schematic



v. XOR

✓ Schematic



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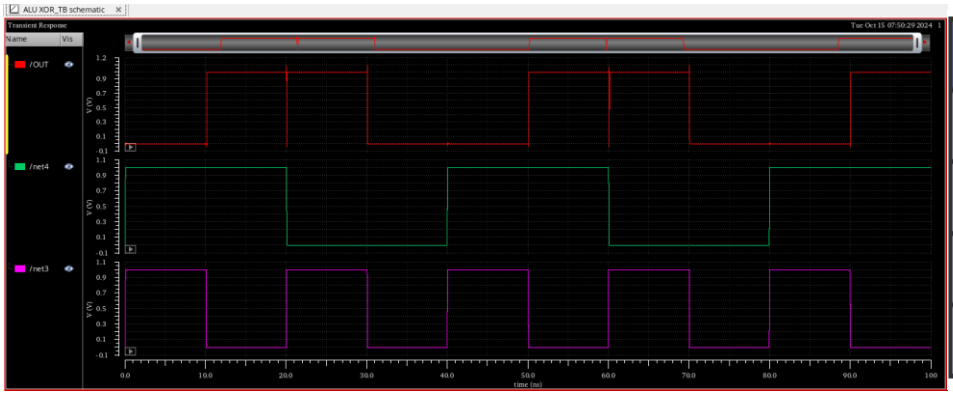
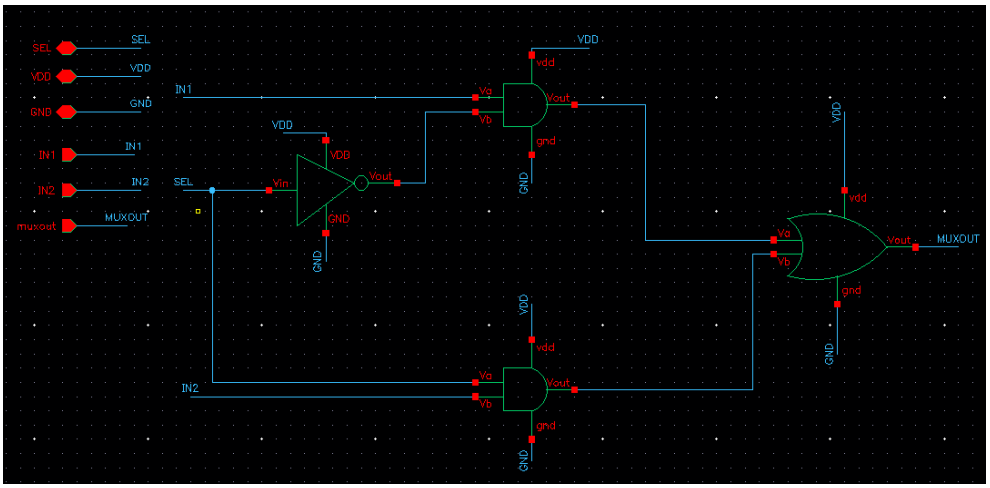


A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Chap-2

vi. MUX 2:1

✓ Schematic



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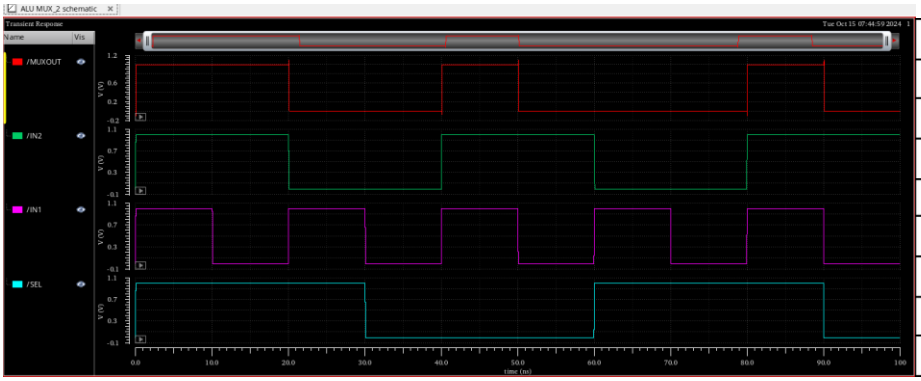
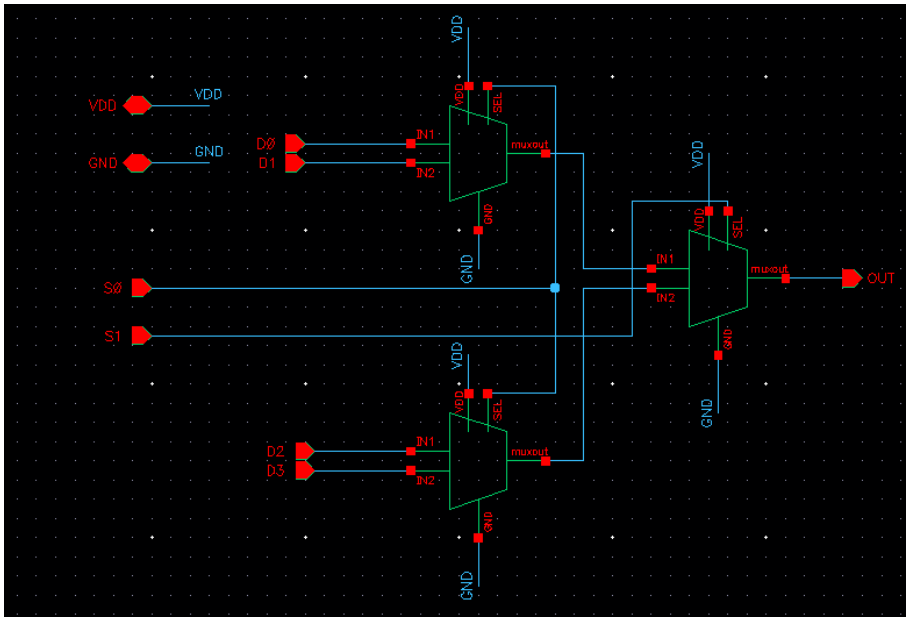


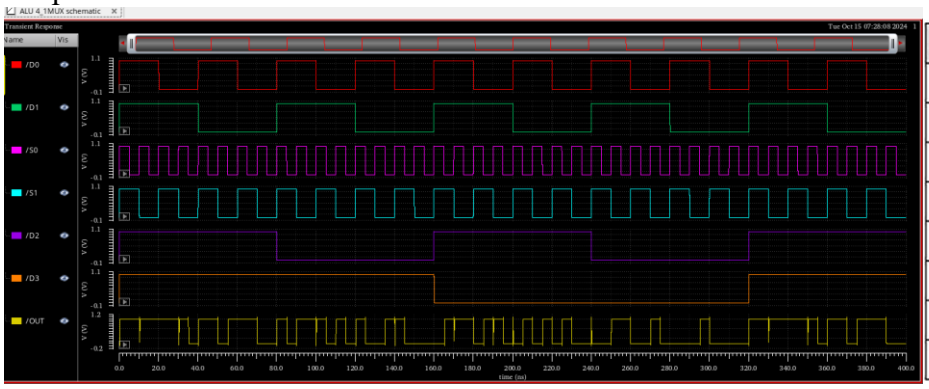
S	A	B	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

vii. MUX 4:1

✓ Schematic



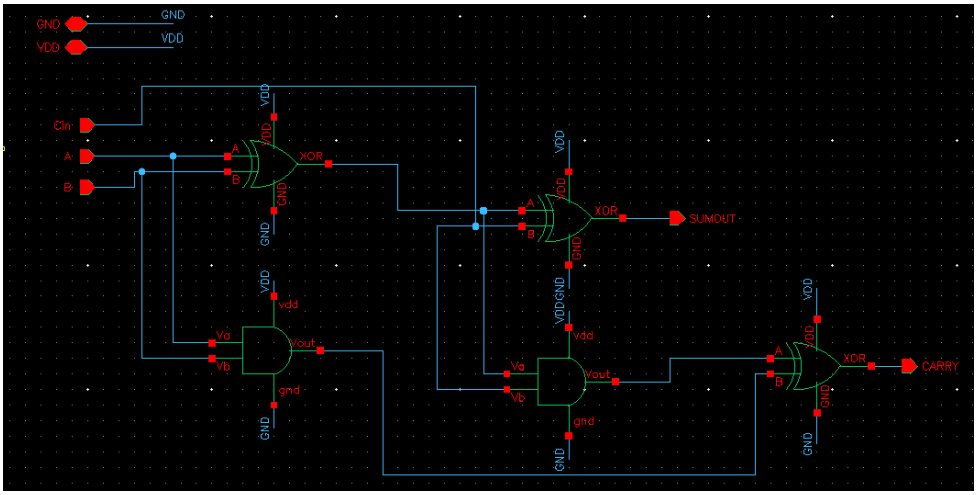
✓ Output



A	B	S	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

viii. 1bit Full Adder

✓ Schematic



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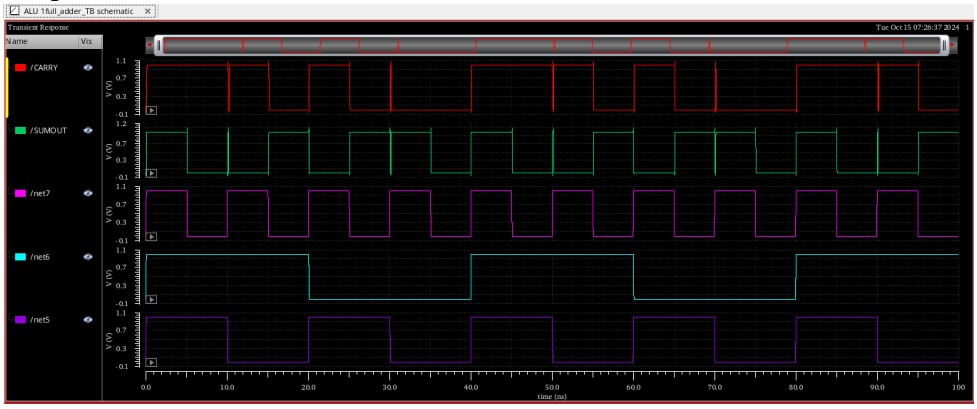
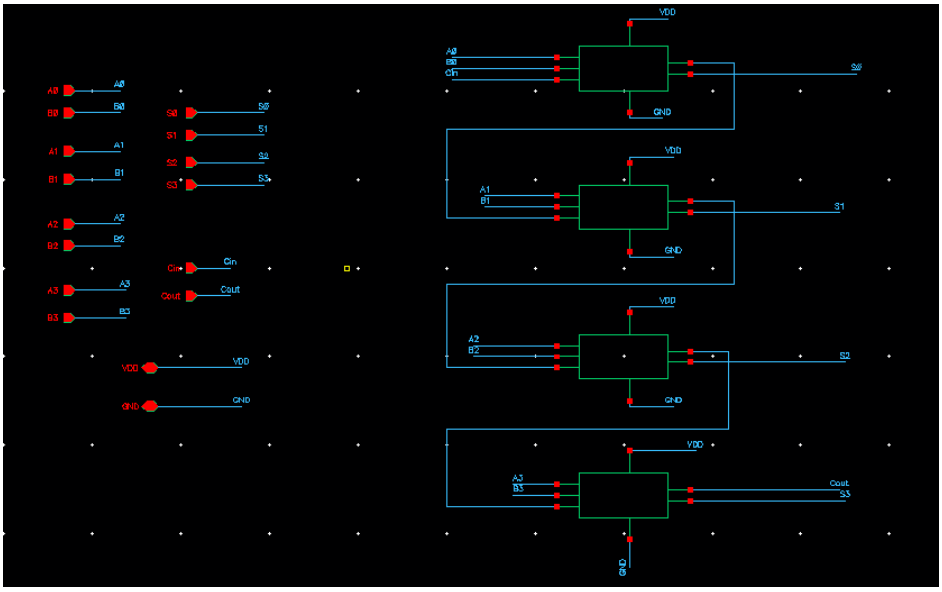


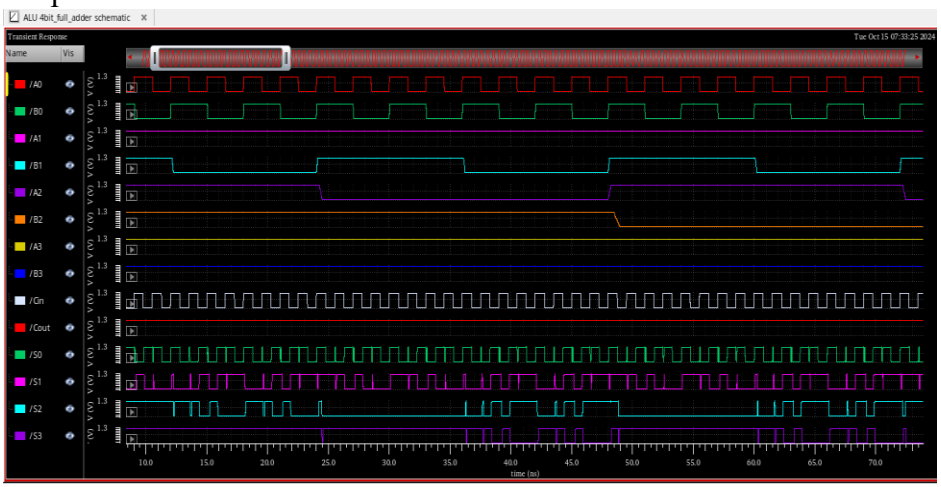
Inputs			Outputs	
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

ix. 4bit Full Adder

✓ Schematic

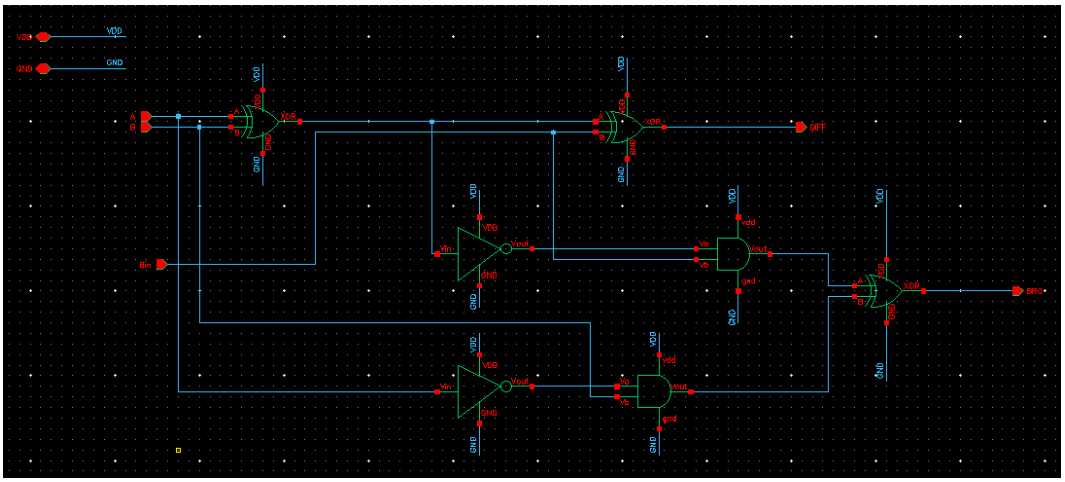


✓ Output



x. Subtractor

✓ Schematic



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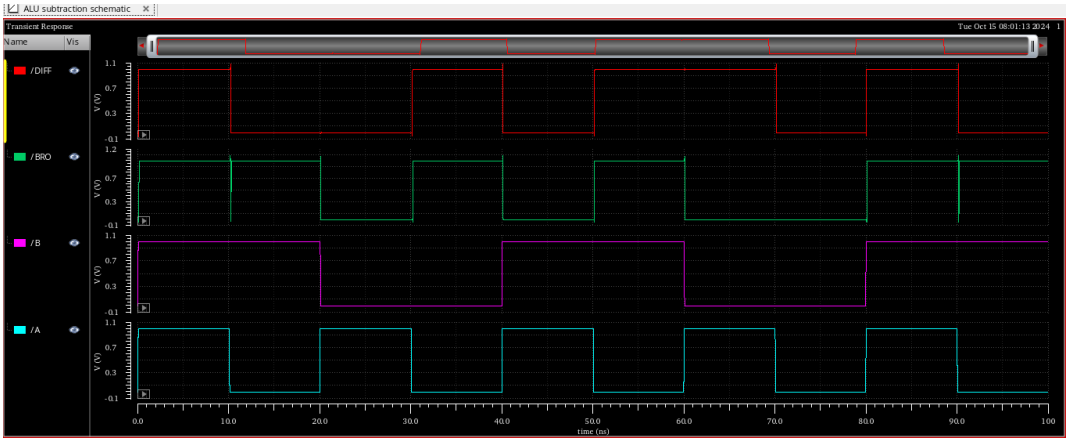
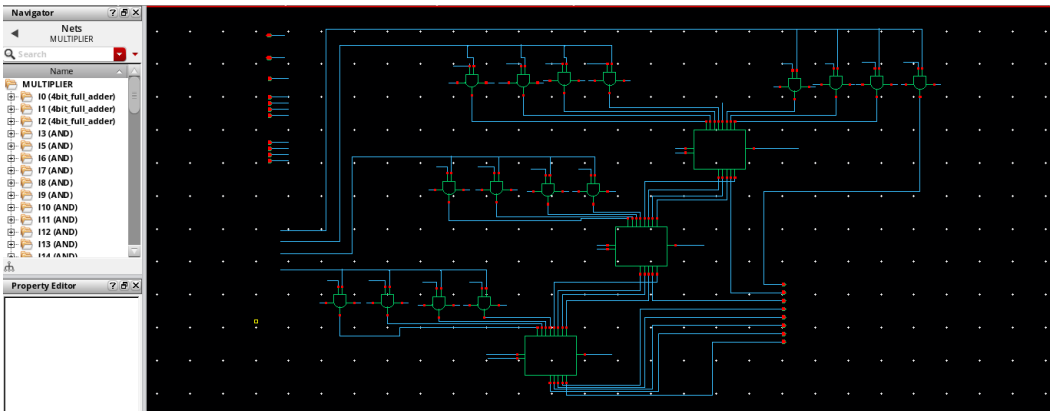


xi. Multiplier

✓ Schematic



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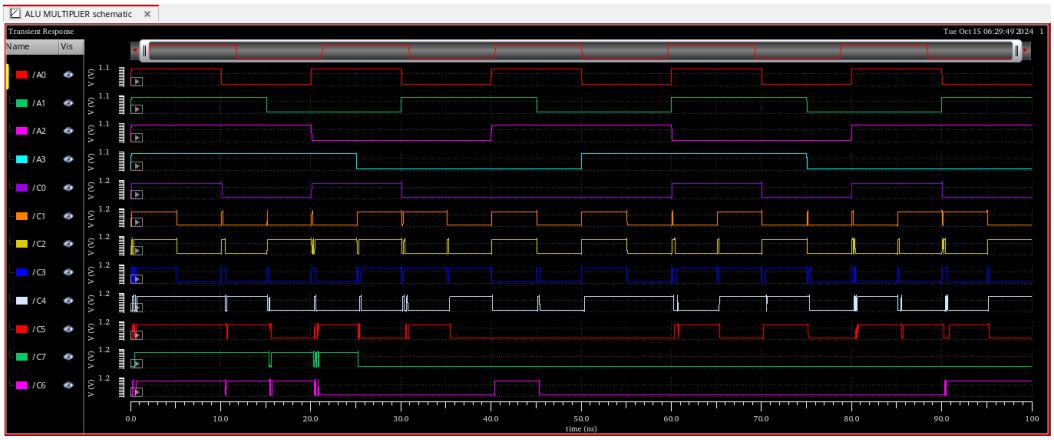
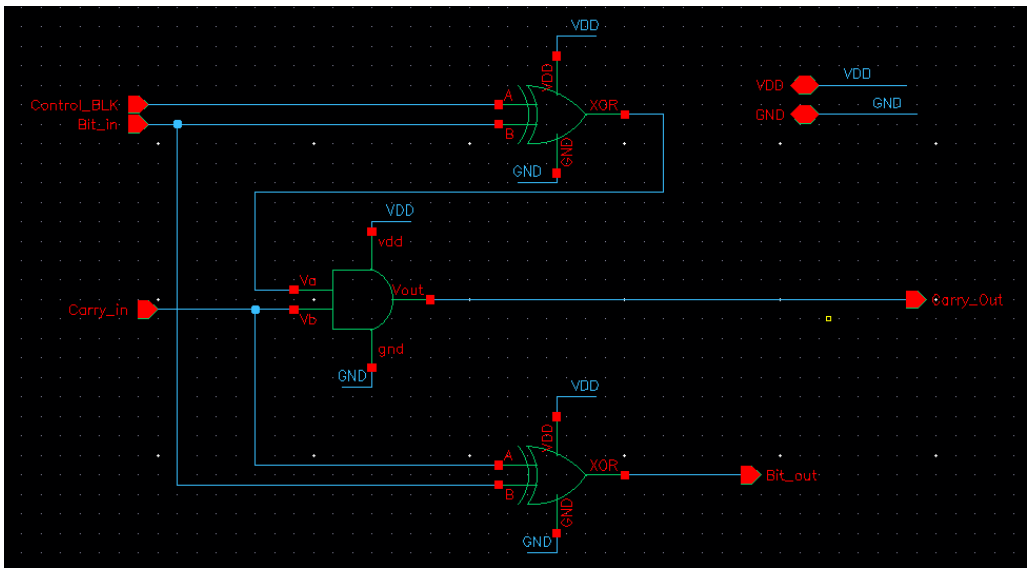


xii. Increment Decrement

✓ Schematic



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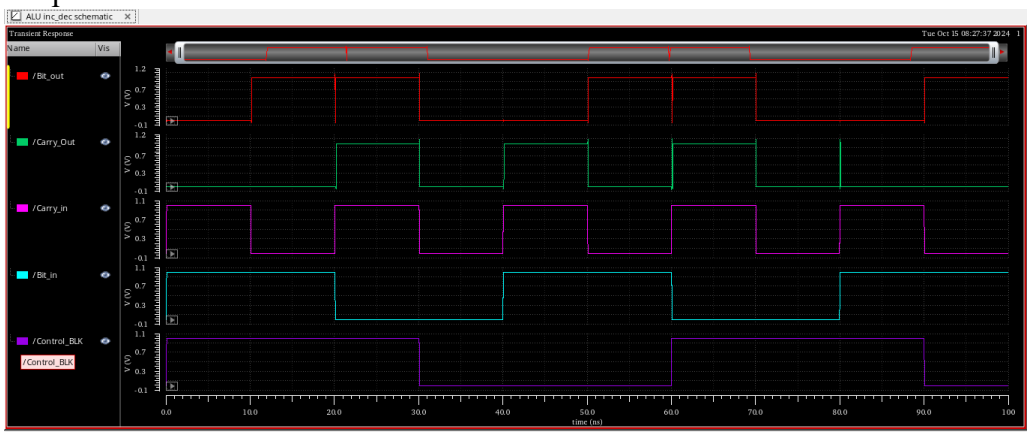
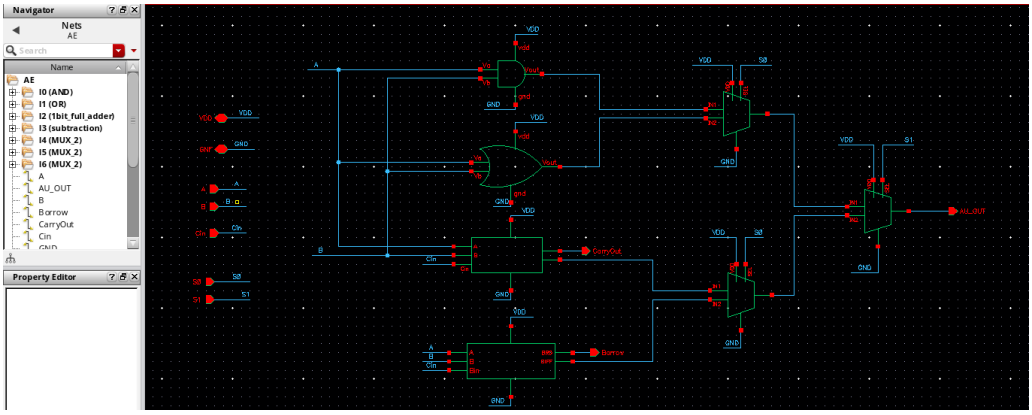


4. ALU

i. Arithmetic Unit

✓ Schematic



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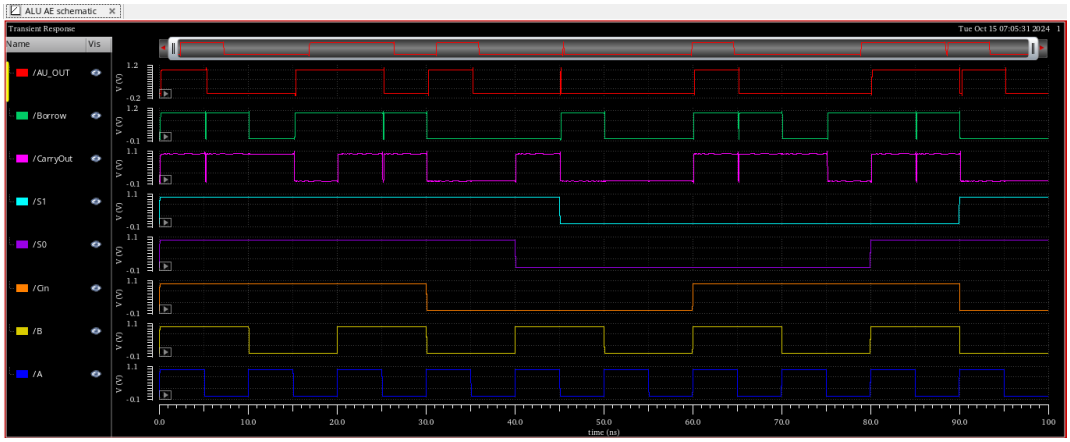
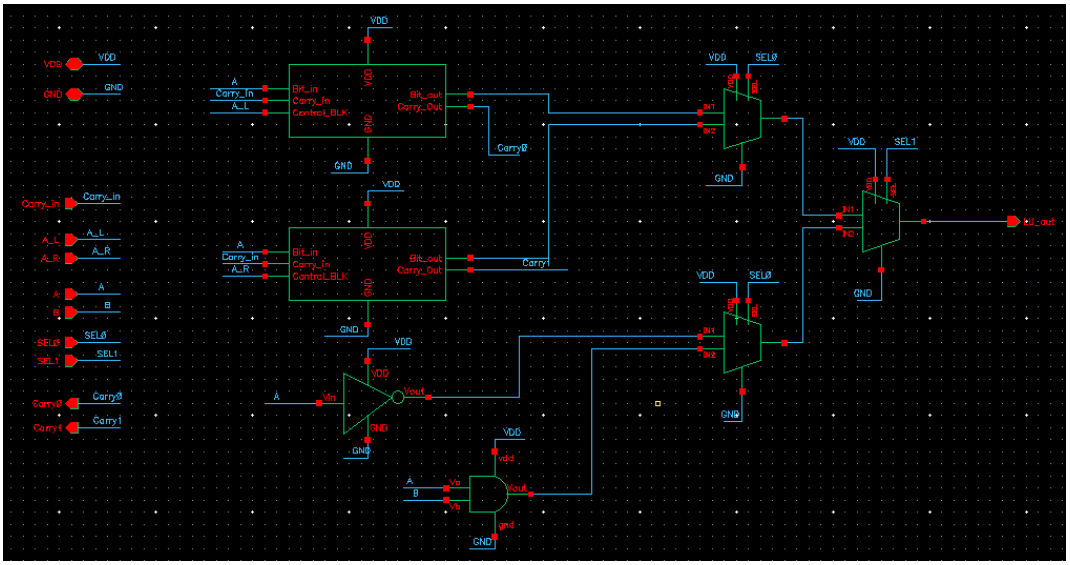


ii. Logic Unit

✓ Schematic



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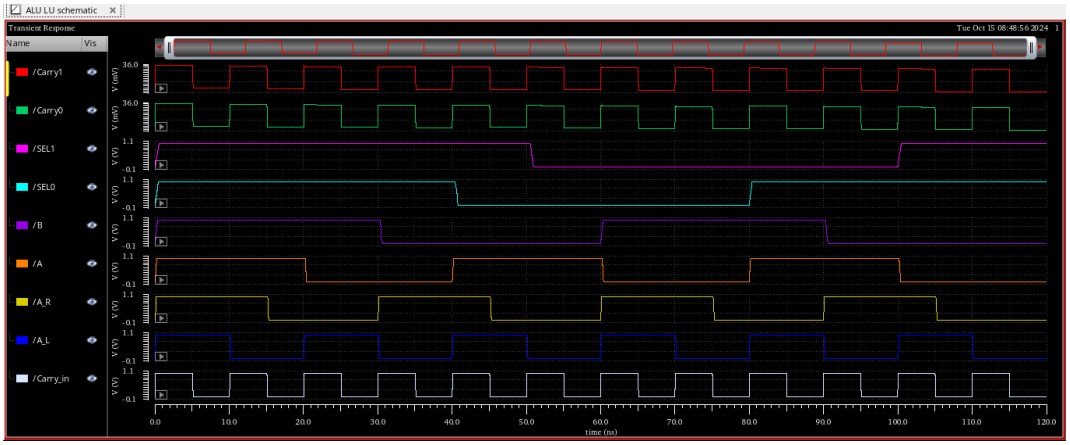
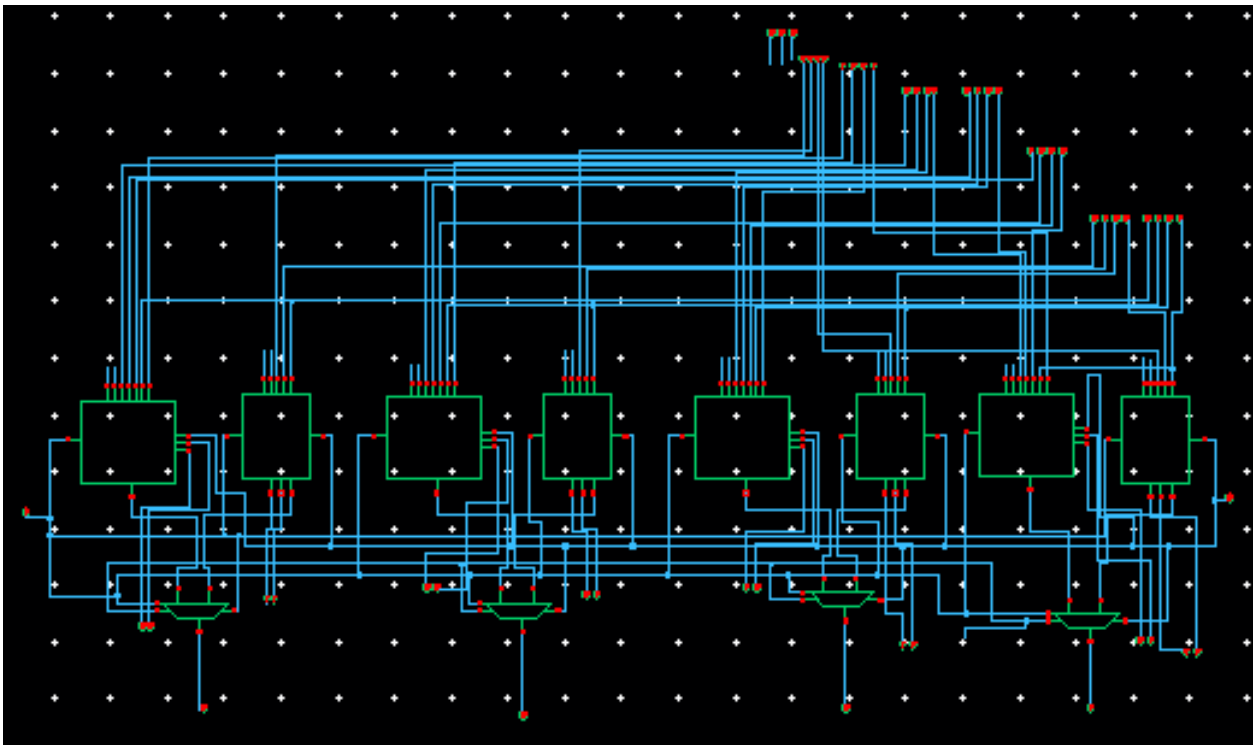


Final Diagram



5. Conclusion

In conclusion, the design of a 4-bit Arithmetic Logic Unit (ALU) using Cadence Virtuoso successfully demonstrates key digital design principles. An array of arithmetic and logical operations is efficiently carried out by the ALU using the integration of 4-bit registers for inputs A and B and a 2-bit select (SEL) input.

This project gives important practical experience with industry-standard technologies and emphasizes the significance of extensive design, simulation, and verification processes. Future research might concentrate on improving the ALU's performance or extending its range of applications for incorporation into more complex systems.