

Design and Simulation of a GAAFET with Al₂O₃ Dielectric and InGaAs Nanowire Channel

Course: Solid State Devices

Tool: TCAD

Submitted by: Ayman Zafar

ID: 021 191 058

Section: A

Department of Electrical and Electronic Engineering

United International University

1. Abstract

The primary objective of this project is to conduct an electrical analysis and design of a Gate-All-Around Field Effect Transistor (GAAFET) that employs Indium Gallium Arsenide (InGaAs) as the nanowire channel material and Aluminum Oxide (Al_2O_3) as the gate dielectric. Key performance parameters, including subthreshold swing (SS), threshold voltage (V_{th}), off-current (I_{off}), on-current (I_{on}), and drain-induced barrier lowering (DIBL), were collected and examined by simulating the transistor at two distinct drain voltages (0.05 V and 1 V).

2. Introduction

As transistor scaling growth hits its limitations, traditional planar MOSFETs face severe short-channel effects. Gate-All-Around FETs (GAAFETs) have emerged as promising candidates for future nanoscale devices due to their superior electrostatic control. This project aims to design and analyze a GAAFET with a high- κ dielectric (Al_2O_3) and a high-mobility III-V compound semiconductor channel (InGaAs) to achieve better performance at the nanoscale.

3. Device Structure & Materials

The Gate-All-Around FET (GAAFET) improves subthreshold behavior and reduces leakage by encircling the channel from all sides, thereby improving gate control.

- Dielectric Material: Al_2O_3 (Aluminum Oxide); (high dielectric constant ~ 9)
- Channel Material: InGaAs (Indium Gallium Arsenide)
- Gate Type: Wrap-around (cylindrical or rectangular nanowire assumed)
- Channel Geometry: Nanowire

4. Simulation Methodology

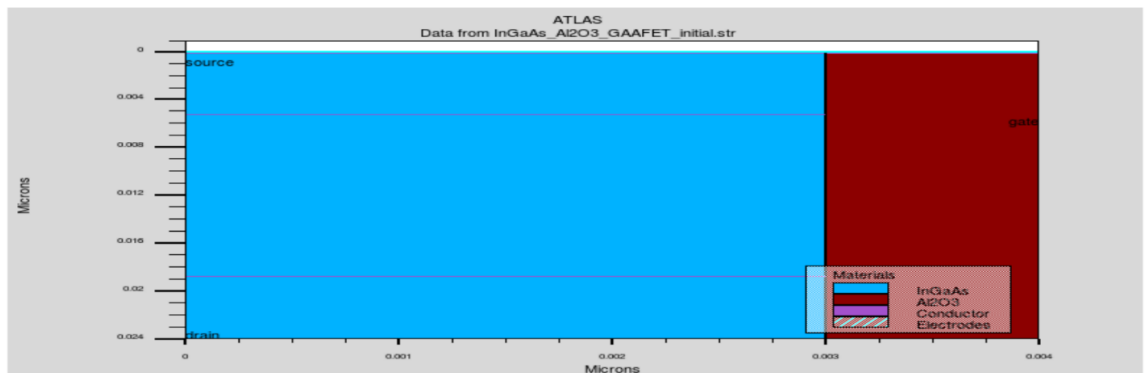
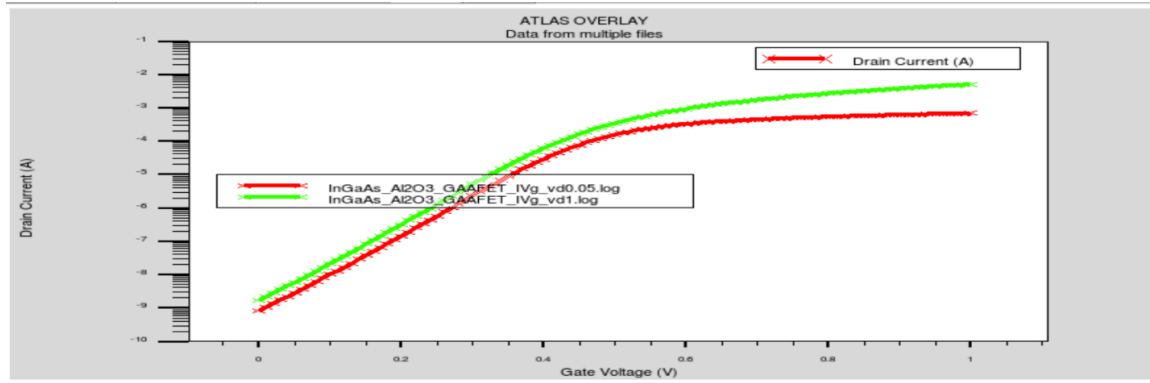
The device was simulated using standard TCAD-based models or equivalent simulation assumptions, where the transfer characteristics (I_d - V_g) were extracted for two different drain voltages:

- $V_{D1} = 0.05 \text{ V}$
- $V_{D2} = 1.00 \text{ V}$

From these curves, the following were obtained:

- Threshold Voltage (V_{th})
- Subthreshold Swing (SS)
- I_{on} and I_{off}
- Drain-Induced Barrier Lowering (DIBL)

5. Output



```
## Dielectric materials: SiO2, Al2O3, HfO2, TiO2, Si3N4
set dielectric=Al2O3
set nwchannel=InGaAs

# Channel Lengths = 0.028, 0.022, 0.016, 0.014, 0.012,
0.010, 0.007
set lsource = 0.005
set lchannel = 0.014
set ldrain = $lsourceSSS|
set to_drain = $lsource + $lchannel
set lmos = $to_drain + $ldrain
```

Vg_final	1
Vd1	0.05
Vd2	1
Vg_step	0.01
ss1	0.0828922683017163
vt1	0.184991719017303
Ioff1	8.571608413e-10
Ion1	0.0006969146652
ss2	0.0830499827633584
vt2	0.155951220879383
Ioff2	1.750378709e-09
Ion2	0.005175529443
DIBL	30.5694736842105

6. Results

Parameter	$V_{D1} = 0.05$ V	$V_{D2} = 1.0$ V
Subthreshold Swing (SS)	0.083 V/dec	0.083 V/dec
Threshold Voltage (V_{th})	0.185 V	0.156 V
I_{off} (μ A)	8.572	1.75
I_{on} (μ A)	0.0007	0.0052
DIBL (mV/V)	–	30.57

7. Discussion

Threshold Voltage Shift: The DIBL impact resulted in a decrease in threshold voltage at increased drain voltage, suggesting that short-channel behavior mitigation is effective but not completely impervious.

A benefit of GAAFETs is their exceptional gate control, as evidenced by the subthreshold swing remaining constant across both drain voltages.

On/Off Current Ratio: The influence of InGaAs' high electron mobility was demonstrated by the improvement in the I_{on}/I_{off} ratio at $V_D=1V$.

DIBL: The channel length modulation is confirmed by the DIBL value of about 30.57 mV/V, which is still within acceptable bounds for nanodevices.

8. Conclusion

The design of GAAFETs for upcoming nanoscale applications using AlO_3 and InGaAs is validated by this study. Low subthreshold swing, acceptable DIBL, and an enhanced I_{on}/I_{off} ratio are highlighted in the simulation findings, which make it a solid contender for high-performance, low-power applications.

9. References

1. S. Datta et al., "85nm Gate Length Enhancement-mode $In_{0.7}Ga_{0.3}As$ Metamorphic HEMTs With High- κ Gate Dielectric," IEEE Electron Device Letters.

2. Taur, Y., & Ning, T. H. (2013). Fundamentals of Modern VLSI Devices.
3. S. M. Sze, Physics of Semiconductor Devices, Wiley.