GOVERNMENT COLLEGE OF ENGINEERING & CERAMIC TECHNOLOGY
AN AUTONOMOUS INSTITUTE
AFFILIATED TO MAKAUT (FORMELY KNOWN AS WBUT)

Theory / B. Tech / CSE / SEM - III / Code – CS 302 / 2016-17

Paper Name: Digital Logic

Full Marks: 75 **Time Allotted: 3 hours**

The figures in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
[MCQ Type Questions][Compulsory]

1. Choose the correct alternative of the following questions. Answer all questions. **10 x 1 = 10**

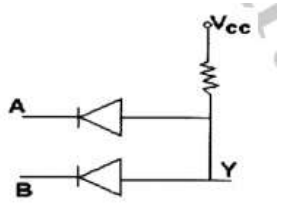
i) The OR operation can be produced using
   a) two NOR gates b) three NAND gates
   c) four NAND gates d) both (a) and (b)

ii) The race around condition does not occur in Flip Flop
   a) J-K b) T
   c) Master slave d) none

iii) A three variable Karnaugh-MAP has
   a) 16 minterms b) 8 minterms
   c) 24 minterms d) none

iv) Identify the carry expression of full adder circuit
   a) X'Y+ZX' b) XY+XZ+ZX
   c) X'Y+XZ'+ZX d) X'Y'+X'Z+ZX

v) Identify the operation of the circuit



vi) In which code the successive codes differ in only position
   a) Gray b) Excess 3
   c) 8421 d) Hamming code

vii) The fastest logic family is
   a) ECL b) CMOS
   c) TTL d) RTL

viii) The memory which is electrically erasable is
   a) EEROM b) EPROM
   c) PROM d) None of these

ix) Assign the proper odd parity bit to the code 111001
   a) 1111011 b) 1111001
   c) 0111111 d) 0011111

x) The hexadecimal equivalent of the decimal number 115 is
   a) 72 b) 73
   c) 70 d) None of these

GROUP – B
[Short Answer Type Questions]
Answer any *four* of the following

4 x 5 = 20

2. Reduce the following Boolean expression to three literals.
   $(x'y'+z)'+z+xy+wz$ [5]

3. Find the simplified expression of sum and carry output of a full adder using Karnaugh Map. Draw the circuit diagram of a full adder using half adders and logic gates. [5]

4. Implement a 4X16 decoder two 3X8 decoders and explain. Use block diagram only. [5]

5. What is don't care condition? Simplify the following Boolean function F, together with the don't-care conditions $F(x, y, z) = \sum (0, 1, 4, 5, 6)$ $d(x, y, z) = \sum (2, 3, 7)$. [5]

6. Simplify the following Boolean function into product-of-sums form:
$F(A, B, C, D) = \sum(0, 1, 2, 5, 8, 9, 10)$. [5]

7. Draw the circuit diagram of a S R flip flop using NAND gate. Do the following conversions:
i) SR to D flip flop ii) JK to T flip flop [5]

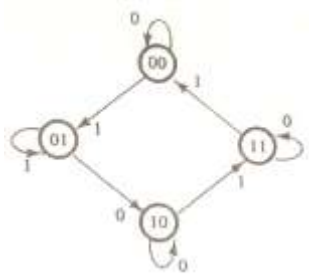
GROUP – C
[Long Answer Type Questions]
Answer any *three* of the following

3 x 15 = 45

8. a) A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is zero otherwise. Design a 3-input majority circuit by finding its truth table.
b) Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output one is greater than the input. When the binary input is 4, 5, 6, or 7, the binary output two is less than the input. [5+10]

9. a) Explain the function of ROM. What are the different types of ROM available?
b) A circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. Design the combinational circuit using a ROM. [5+10]

10. Design the clocked sequential circuit whose state diagram is given in the following figure. The type of flip flop to be used is JK flip flop. [15]



11. a) What is the difference between asynchronous and synchronous sequential circuit? Explain the principle of operation of a MOD 16 ripple counter with a suitable block diagram and draw the timing diagram. [10+5]
b) What are the different types of hazards that may cause a sequential circuit to malfunction?

12. a) Implement a combinational circuit having a truth table given below with a 4X2 ROM and logic gates.

A_1(input)	A_2(input)	F_1(output)	F_2(output)
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	0

b) Draw a neat diagram of PLA and explain function of each component. [5+10]

13. Write short notes on any three of the following: [3 × 5 = 15]
a) Transistor-transistor logic
b) Priority encoder
c) Propagation Delay
d) Shift register

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