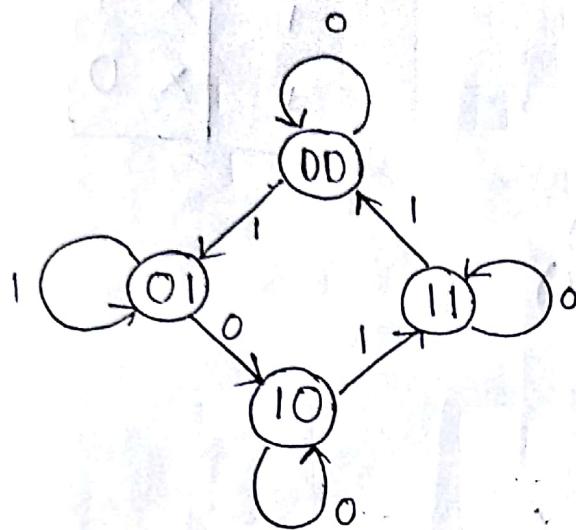


sequential circuit design

Date: 29.8.18



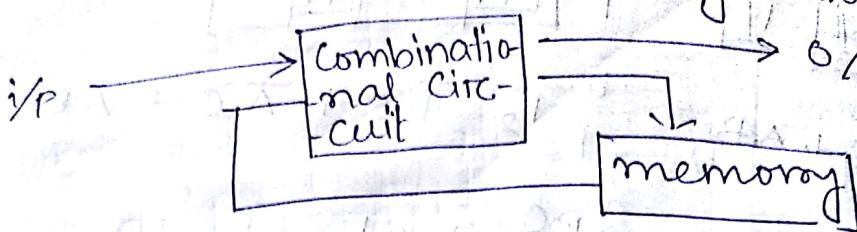
Design a seq. ckt.
State diagram is given.
Given: Can only use J-K F.F.

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

State Table :

Present state		Next state		Input of comb. ckt		Next state		Q/P of comb ckt		F.F I/Ps	
A	B	X=0	X=1	Present state A	Input X	A	B	JA KA	JB KB		
0	0	0	0	0	0	0	0	0	X	0	X
0	1	1	0	0	1	0	1	0	X	1	X
1	0	1	0	1	1	1	0	1	X	0	1
1	1	1	1	1	0	1	1	1	0	X	0

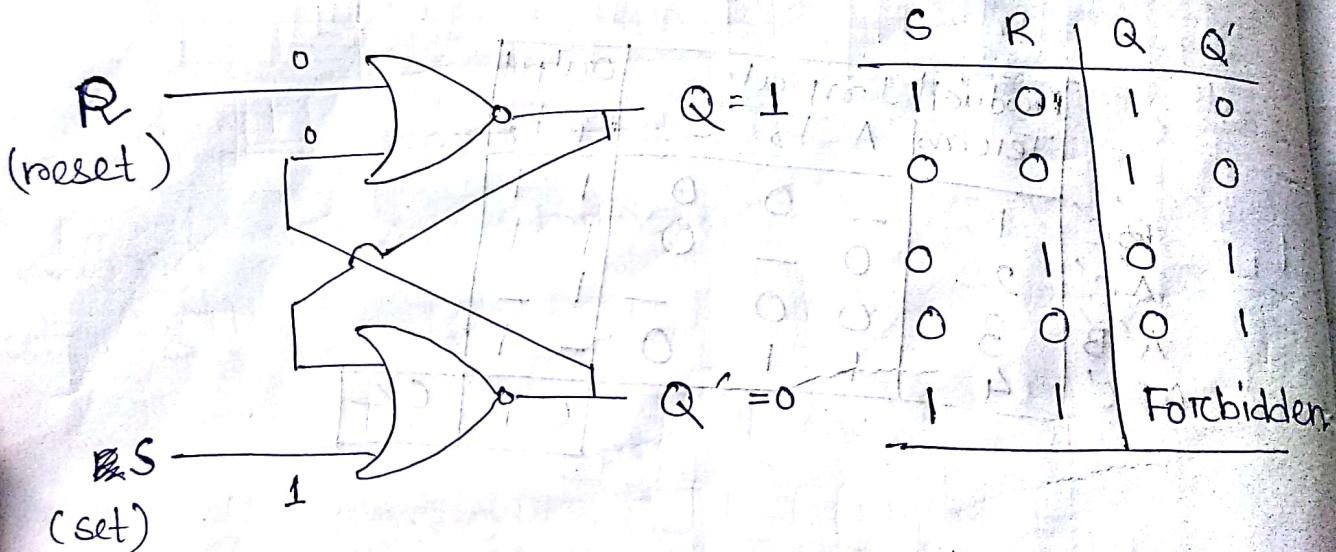
Sequential Circuit



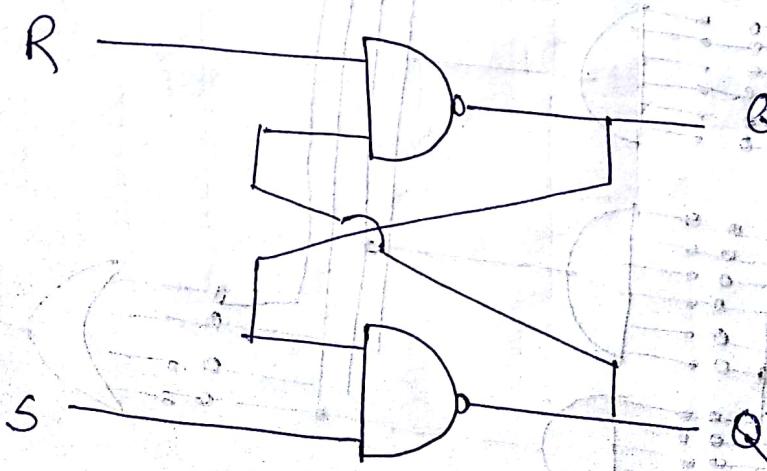
Date: 16.1.17
 ↳ Synchronous (Clock)
 ↳ Asynchronous

Flip-Flop:
 One bit memory element

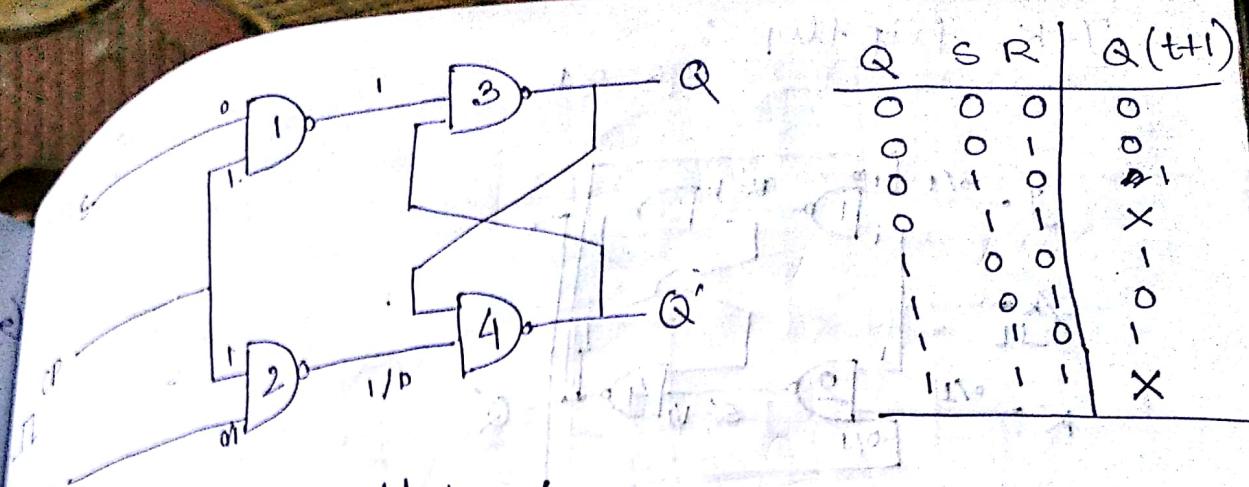
Latch \rightarrow without clock-pulse, a flip-flop.



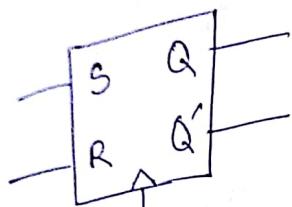
S-R Latch



S	R	Q	Q'
0	1	0	1
0	1	0	1
1	0	1	0
1	0	1	0
0	0	Forbid	Forbid



triggered
RS flip-flop



CP edge

SR	00	01	10	11
Q	0	0	X	1
	1	0	X	1

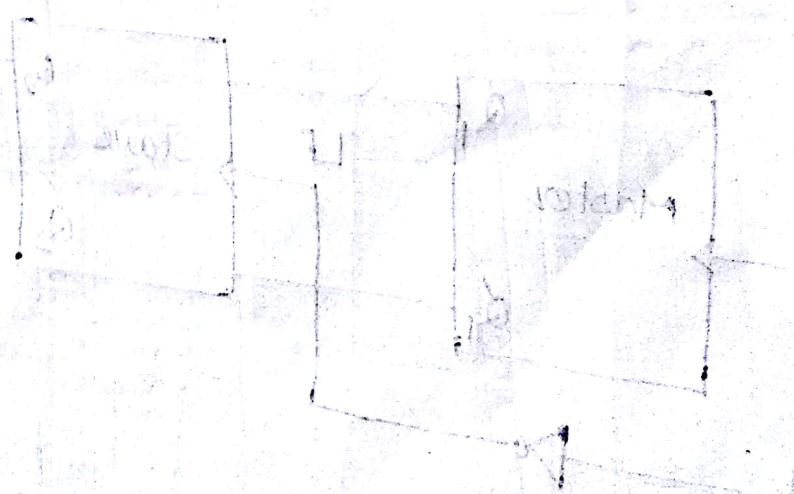
$$Q(t+1) = \cancel{S} + \cancel{Q}R'$$

initial condition

new values set via feedback until

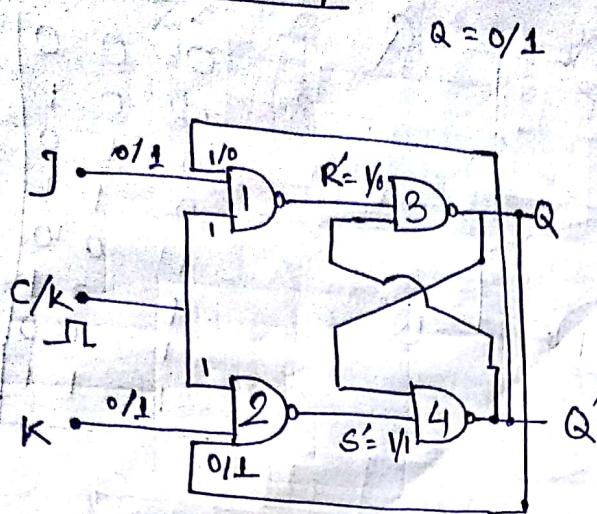
equilibrium is reached

for all AND-gates



rotates

J-K flipflop :



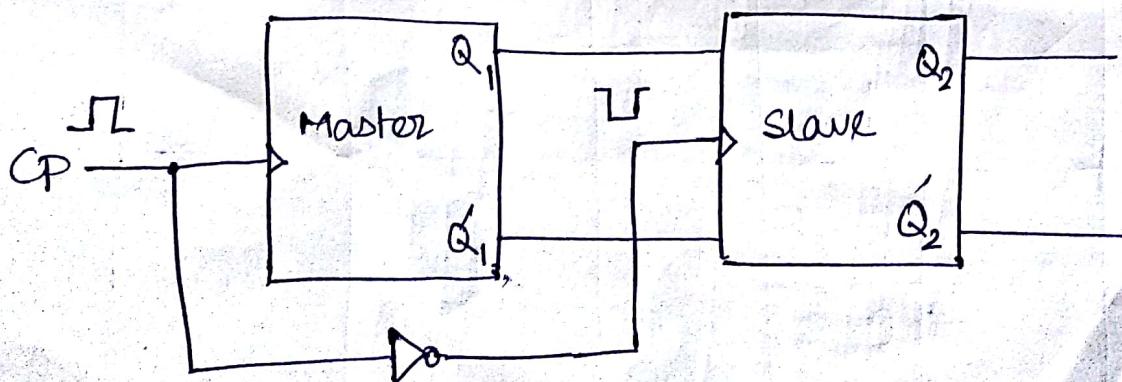
Inputs		Output
J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	01
1	0	1
1	1	\bar{Q}_n

← toggle

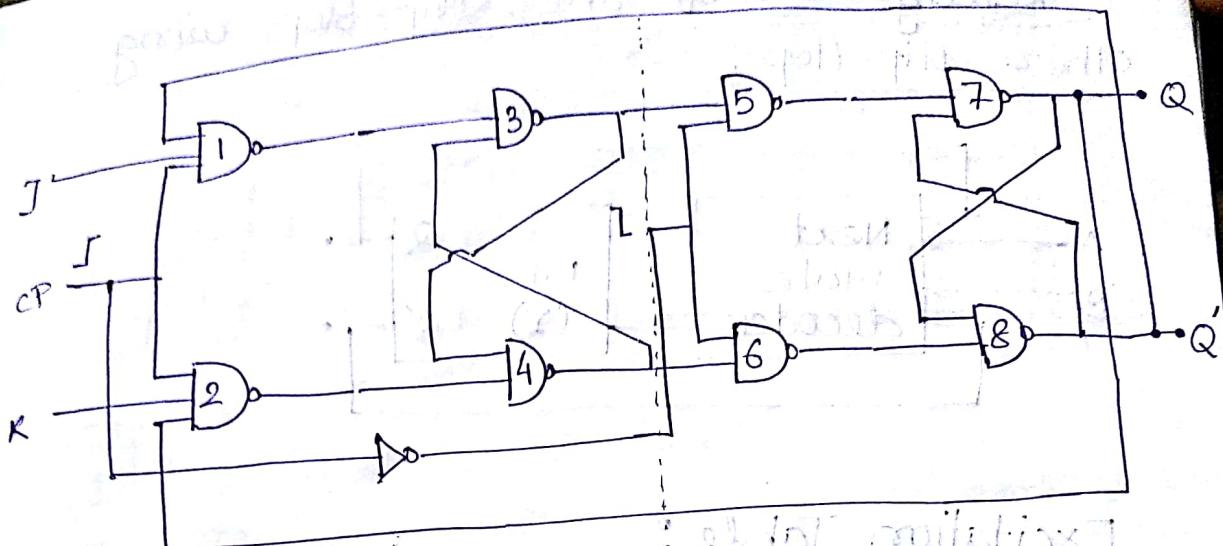
Race-around Condition

This problem can be solved using another type of flipflop.

Master-Slave J-k FF



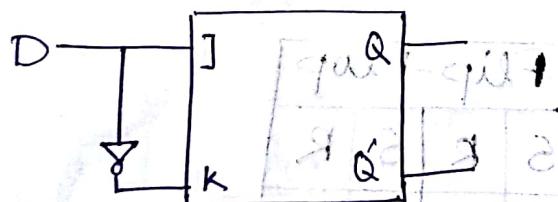
Date : 20.8.19



what is the limitation of JK FF? How it

is solved?

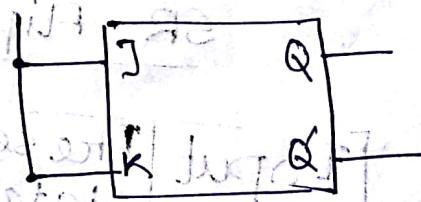
D Flip flop
(Delay)



Input D | Output

0	0 0
1	0 1

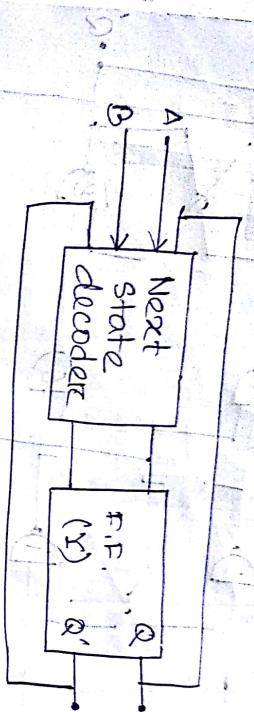
T Flip flop
(Toggle)



Diagram

T	Q _{n+1}
0	Q _n
1	Q' _n

Realization of one flip-flop using other flip-flop:



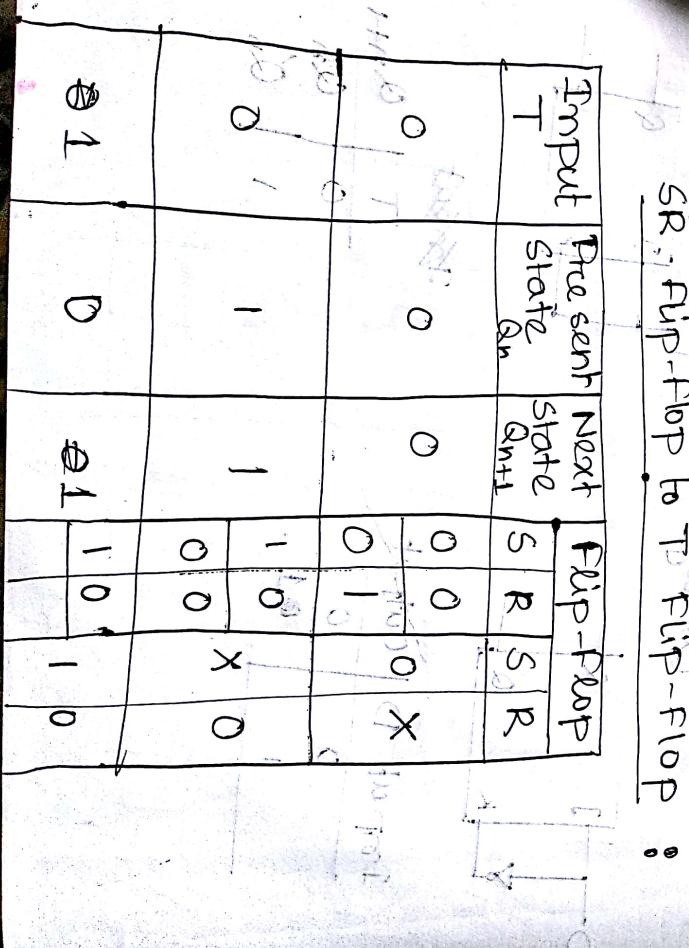
Excitation Table:

Flip-Flop conversion:

Excitation Table:

SR : flip-flop to T flip-flop :

Input	Present State Q_n	Next State Q_{n+1}	flip-flop			
			S	R	S	R
0	0	0	0	0	0	0
0	1	1	0	1	X	0
1	0	1	1	0	0	0
1	1	0	X	0	0	1

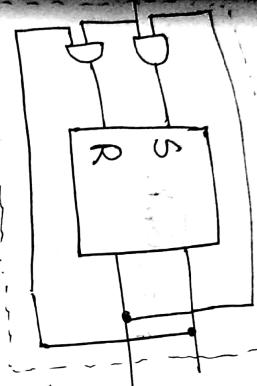


$S =$

$R =$

-	-	-	0	0	0	J		
-	0	0	-	-	0	K		
-	0	1	0	1	0			
-	1	-	-	0	0			
0	0	0	0	0	0			
0	0	0	0	0	0			
X	0	X	0	X	0			
0	X	X	0	X	0			
0	1	-	0	0	X			
1	0	0	0	1	0			

SR flip-flop to JK flip-flop :



$$S = TQ_n$$

Q_n	T	S	Q_{n+1}
0	0	0	0
0	1	X	1
1	0	0	1
1	1	X	0

Q_n	R	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$R = Q_n T$$

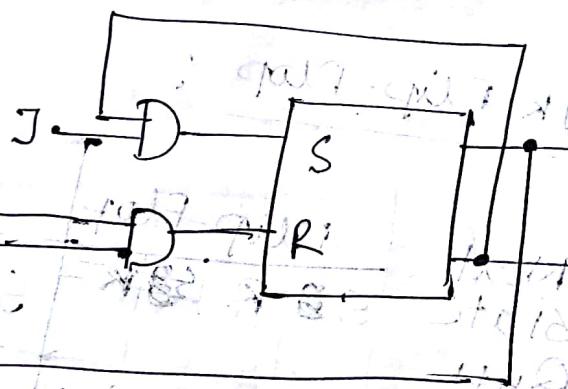
and
also

	JK	00	01	11	10	
Q _n	0	X	0	1	0	
J	1	0	X	0	1	
K	0	1	0	1	0	
Q _{n+1}	1	0	0	1	0	

	JK	00	01	11	10	
Q _n	0	X	0	1	0	
J	1	0	X	0	1	
K	0	1	0	1	0	
Q _{n+1}	1	0	0	1	0	

$$S = J \bar{Q}_n$$

$$R = Q_n K$$



	JK	00	01	11	10	
Q _n	0	X	0	0	0	
J	1	0	X	0	0	
K	0	1	0	1	0	
Q _{n+1}	1	0	0	1	0	

	JK	00	01	11	10	
Q _n	0	X	0	0	0	
J	1	0	X	0	0	
K	0	1	0	1	0	
Q _{n+1}	1	0	0	1	0	

Input	Present state		Next state		Flip Flop		Q _n Q _{n+1}		S R	
	J	K	Q _n	Q _{n+1}	S	R	0	0	0 X	1 0
0 0	0	0	0	0	0	X	1	0	0 1	1 0
0 1	0	0	0	1	1	0	1	1	X 0	0 1
0 0	1	0	1	0	1	0	0	1	1 X 0	X 0
1 1	1	0	0	1	1	0	0	0	0 0	0 0
1 1	0	1	1	1	X	0	0	1	0 1	0 1
0 0	0	1	1	0	0	1	1	0	1 0	1 0
0 1	0	1	1	0	X	0	0	1	0 1	0 1
1 0	0	1	1	0	1	0	0	1	1 0	1 0
1 1	1	1	1	0	0	1	0	1	1 0	1 0

Q _n	JK	0	0	1	1
		X	0	0	X
0	0	0	0	1	1
1	1	1	1	0	0

JK	Q _n	X	X	0	0
		0	1	1	0
0	0	X	X	0	0
1	1	0	1	1	0

$$S = J \bar{Q}_n$$

$$R = Q K$$

Identify the type of FF

Date: 24/8/19

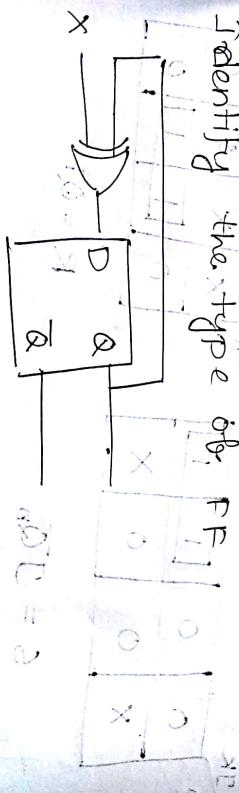
Page No.



- a) R-S
- b) D
- c) J-K
- d) T

Inputs	S.		R		Output Q_{n+1}
	X	$Q_n = X \oplus Q_n$	0	1	
0	0	0	0	1	0
0	1	1	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1

Identify the type of FF



when
either
both
dels

Inputs	D		Output	
	X	Q_n	D	Q_{n+1}
0	0	0	0	0
0	1	1	1	0
1	0	1	1	1
1	1	1	0	0

4

Q
D
T

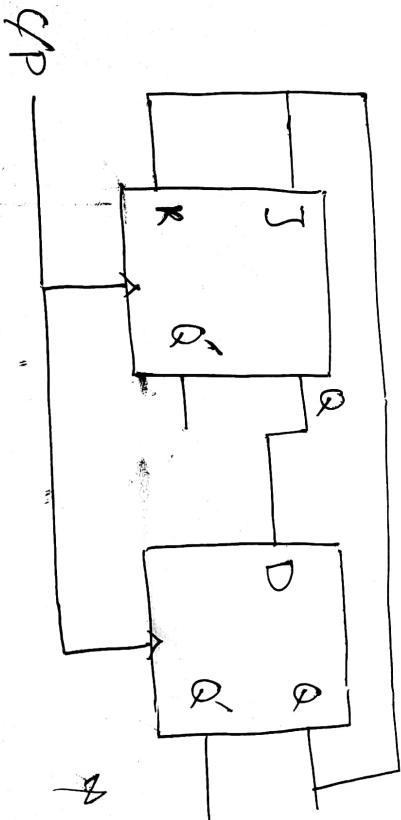
QUESTION

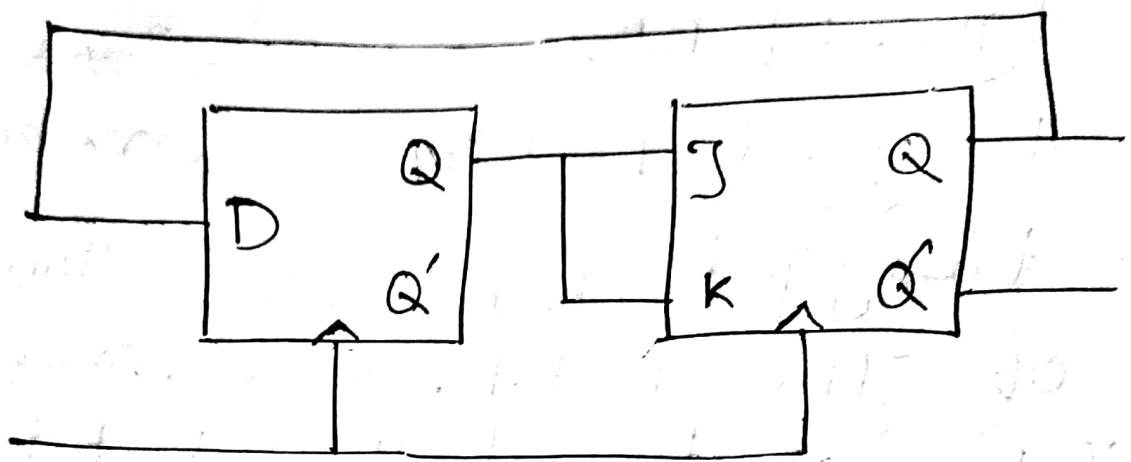
- A +ve edge triggered D F.F is connected to a +ve edge triggered J-K F.F as follows: The Q output of the D F.F. is connected to both the J-K inputs of the J-K F.F while the Q output of the J-K F.F is connected to the input of the D F.F.

Initially the D F.F is set to logic 1.

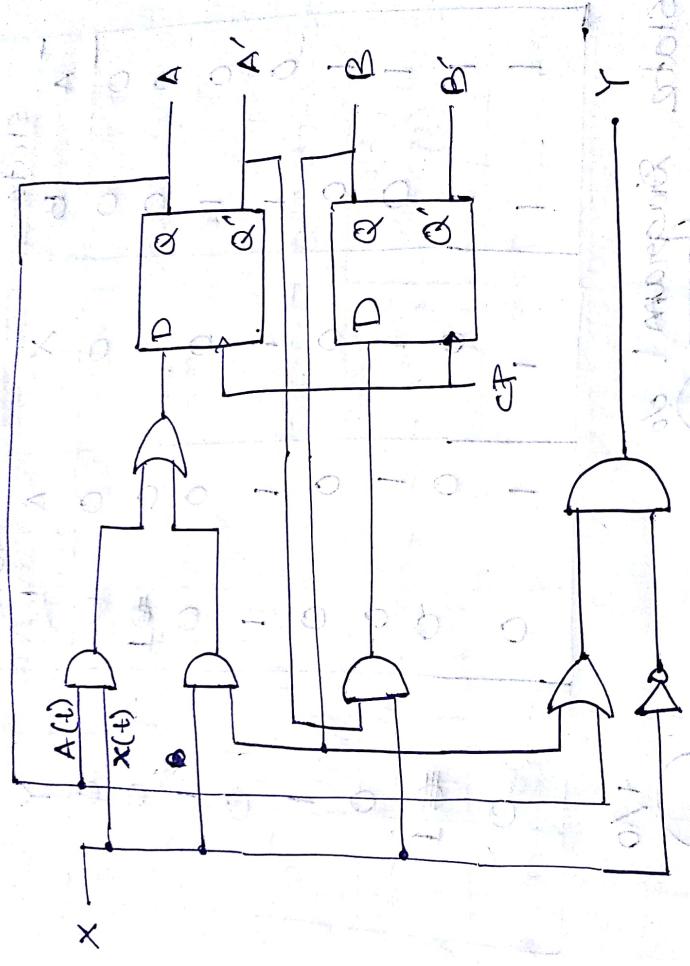
and the output of the J-K F.F is cleared which one of the following is the bit sequence at the Q output of the J-K F.F when the F.Fs are connected to a free running common clock. Assume the both the F.Fs have non zero propagation delay.

- a) 0110110 . . .
- b) 0100100 . . .
- c) 011101110 - - -
- d) 011001100 - - -





Analysis of Clocked Sequential Circuit Date: 27.8.18



$X \rightarrow$ External Input
 $Y \rightarrow$ Final Output

\Rightarrow Next State Characteristic Eqn

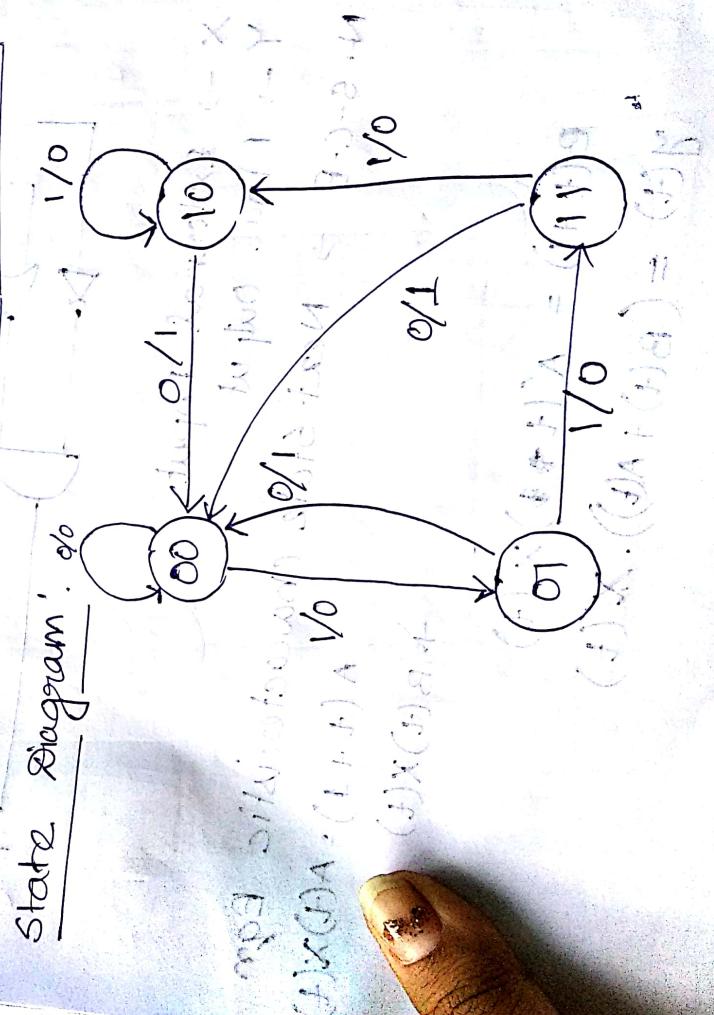
$$A(t+1) = A(t)x(t) + B(t)x(t)$$

$$B(t+1) = A'(t) \cdot x(t)$$
$$y(t) = (B(t) + A(t)) \cdot x'(t)$$

State table:

Present State	Input	Next State		Output
		A	B	
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	1	1	0

State Diagram:



Characteristic Table:

	J	K	Q(t-1)	Q(t)	Q(t+1)
A	0	0	0	0	0
	0	1	0	1	1
	1	0	1	0	0
	1	1	1	0	1

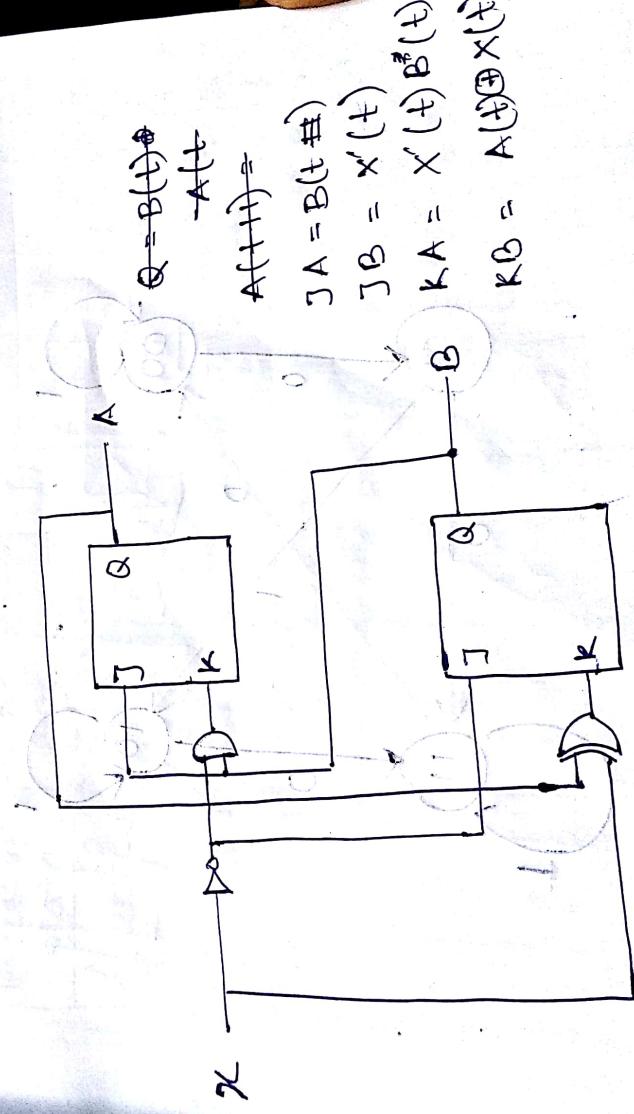
J-K F.F.

	D	Q(t-1)	Q(t)	Q(t+1)
0	0	0	0	0
1	1	0	1	1

D-F.F.

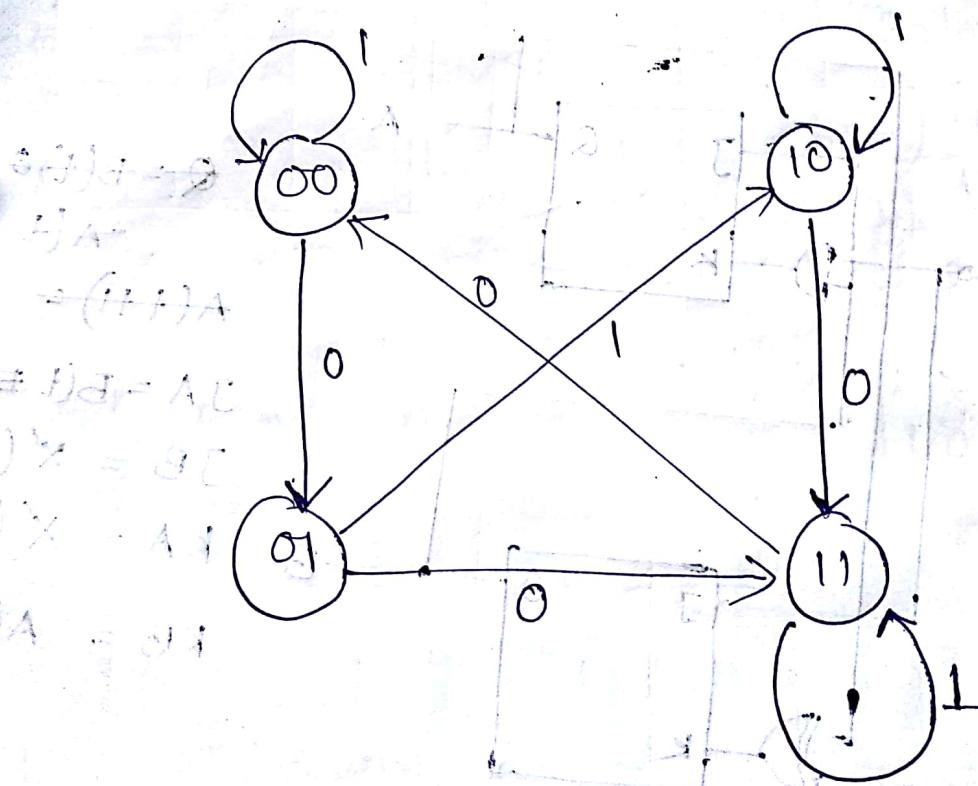
	T	Q(t-1)	Q(t)	Q(t+1)
0	0	0	0	0
1	1	0	1	1
	0	1	0	0

T-F.F.



State Table:

Present state A B	Input x^i	Next state 1				Next state A B	
		JA	KA	JB	KB	A	B
0 0	0	0	0	1	0	0	0
0 0	1	0	0	0	1	0	1
0 1	0	1	1	1	0	1	0
0 1	1	1	0	0	1	1	0
1 0	0	0	0	1	1	0	1
1 0	1	0	0	0	0	0	1
1 1	0	1	1	1	1	1	0
1 1	1	1	0	0	0	0	1

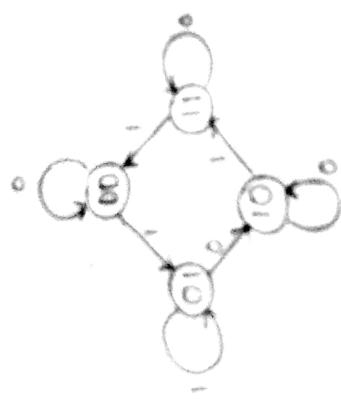


Date : 20/6/18

Sequential Circuit design

Design a seq. circuit

State diagram is given
Given can only use J-K

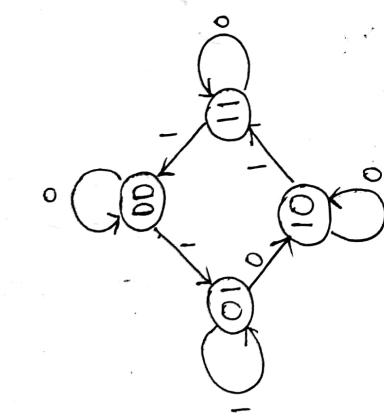


State Table :

Transition	Next State	Inputs	Outputs
S0 to S1	S1	J=0, K=0	Q1=1, Q2=0
S1 to S2	S2	J=1, K=0	Q1=0, Q2=1
S2 to S3	S3	J=0, K=1	Q1=1, Q2=1
S3 to S0	S0	J=1, K=1	Q1=0, Q2=0

Sequential circuit design

Date: 29.8.18

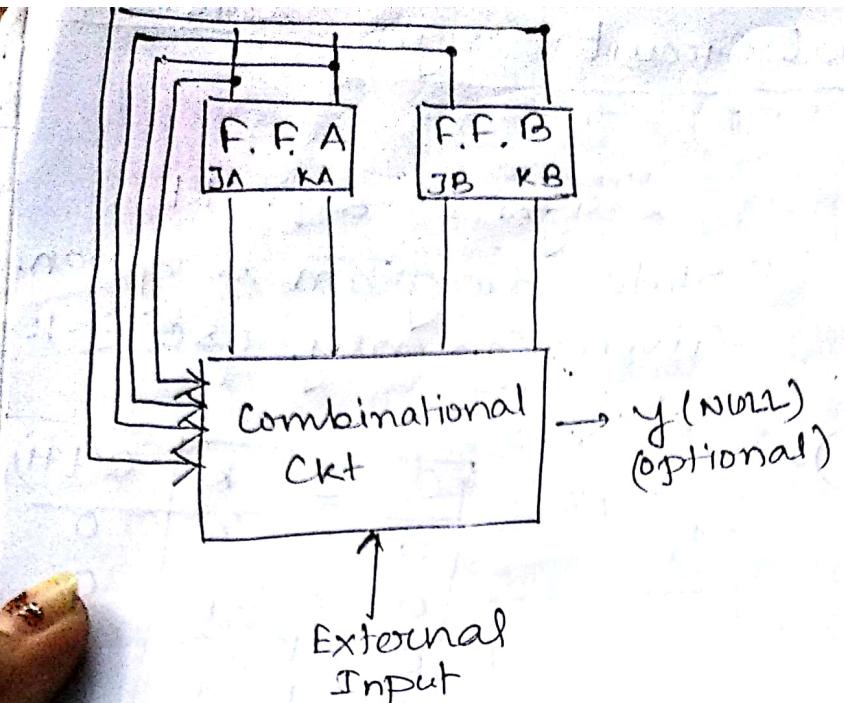


Design a seq. ckt.
State diagram is given.
Given: Can only use J-K F.F.

	Q	J	K	$Q(t+1)$
0	0	0	0	0
0	0	-	-	0
0	-	0	0	0
0	-	0	0	0
0	0	-	-	0
0	0	0	-	0
0	0	-	-	0

State Table :

Present State	Next State $X = \begin{cases} 0 & A \\ 1 & B \end{cases}$	Input of comb. ckt		Next state A B	Output $\begin{cases} X & \text{F.F. I/Ps} \\ JA & JK \\ KA & KB \end{cases}$
		Input present	Input of comb. ckt		
A	0	0 0 0 1	0 0 0 1	0 0	X - X - X - X
B	1	1 0 0 1	0 0 1 0	0 1	X X X X X X X X
A	0	1 0 1 1	0 1 0 1	0 1	- 0 0 0 0 0 0 0
B	1	0 1 1 1	1 0 1 0	1 0	- - - - 0 0 0 0
A	0	- - - -	- - - -	- -	- - - - - - - -
B	- - - -	- - - -	- - - -	- -	- - - - - - - -



$Q(0)$	J	K	$Q(1)$
0	0	X	0
0	1	X	1
1	X	1	0
1	X	0	1

BX	00	01	11	10
01	0	0	0	1
01	X	X	X	X

BX	00	01	11	10
01	X	X	X	X
01	0	0	1	0

$$J_A = BX$$

$$K_A = BX$$

BX	00	01	11	10
A	0	1	1	X
1	0	1	X	X

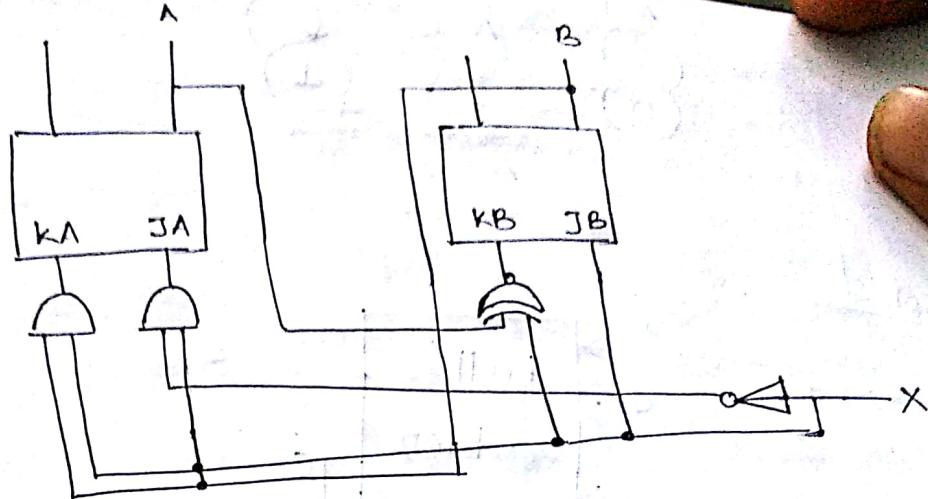
BX	00	01	11	10
10	X	X	0	10
1	X	X	1	0

$$J_B = X$$

$$K_B = (\cancel{A \oplus B})'$$

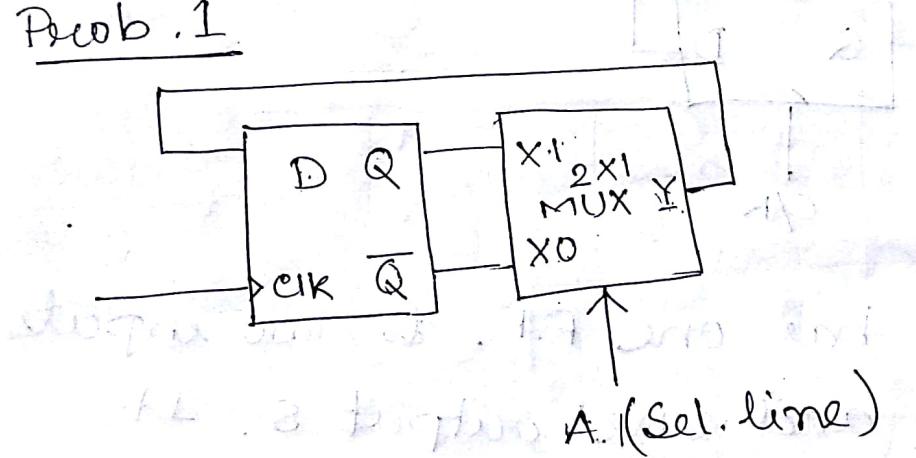
$$\bar{A}X + A'X'$$

$$K_B = (A \oplus X)'$$



Date: 30.8.18

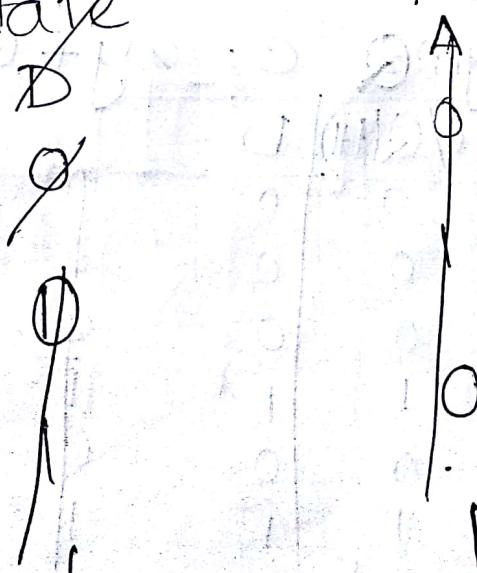
Prob. 1

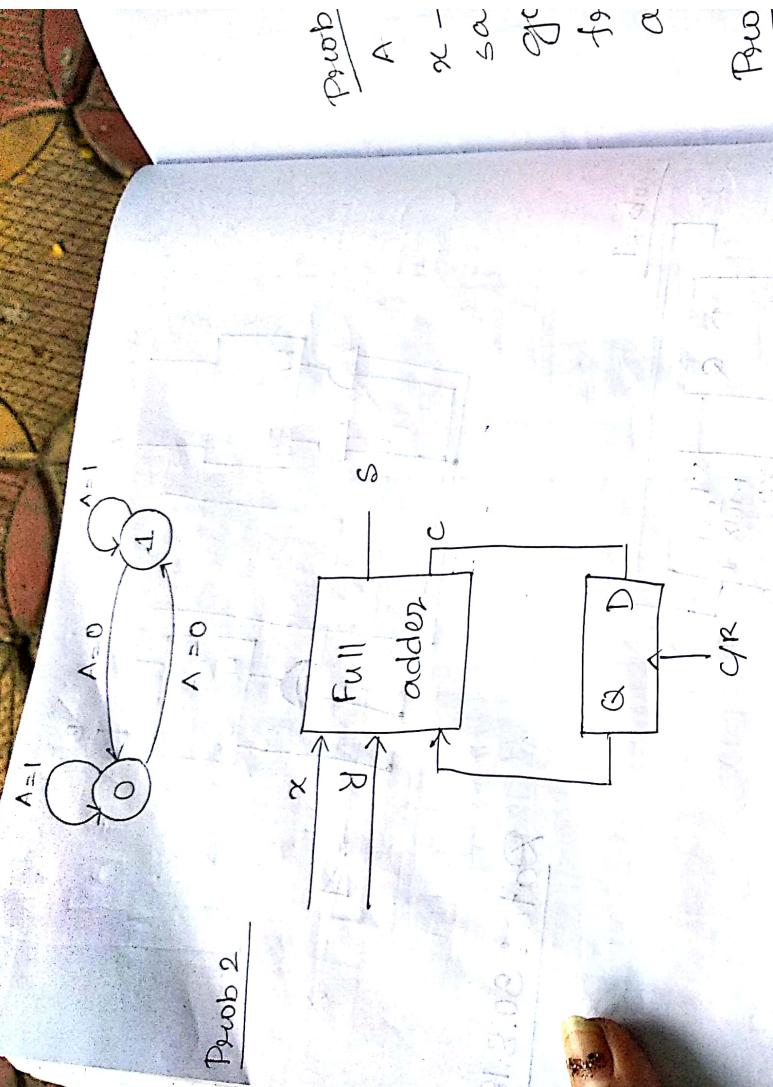


State Table

Present state
D

Input





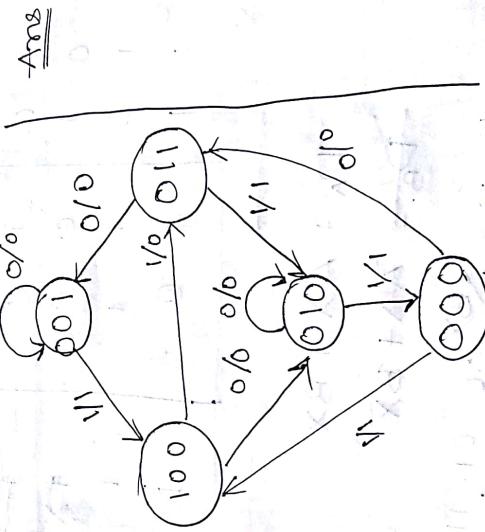
A seq. ckt has one I.F. & two inputs x and y . and one output s . It consists of a full adder ckt connected to a D.R.F. & state table, state

State Table

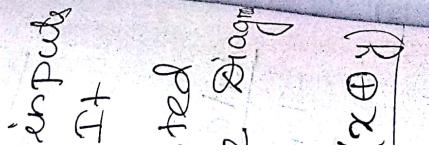
Input	x	y	$S = x \oplus y \oplus Q$	$C = xy + Qx \oplus y$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Prob 3 Design a seq. ckt with 2 D F.F.s A and B and one input x_{in} . When $x_{in} = 0$, the ckt remains in the same state, when $x_{in} = 1$, the ckt goes through the state transitions from 00 to 01, 01 to 11, 11 to 10, and 10 to 00. and repeats.



Prob 4



A seq. ckt has 3 F.F.s A, B, C, one input x and one output y . Design the ckt using D F.F. The ckt to be designed by treating unused states as don't care conditions.

$$D_A = \overline{A} \overline{B} X$$

$$D_B = A + BCX + \overline{C} \overline{X}$$

$$D_C = C \overline{X} + AX + \overline{A} \overline{B} \overline{X}$$

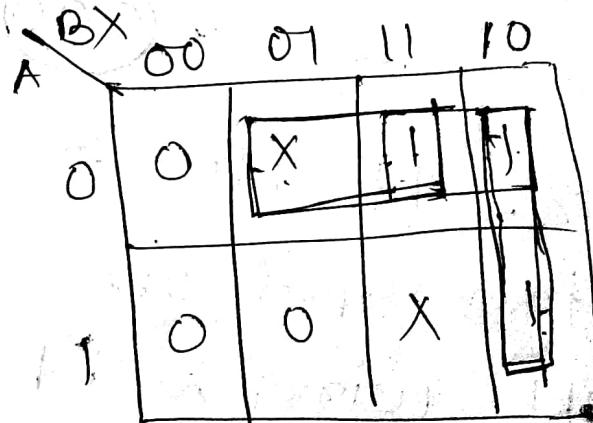
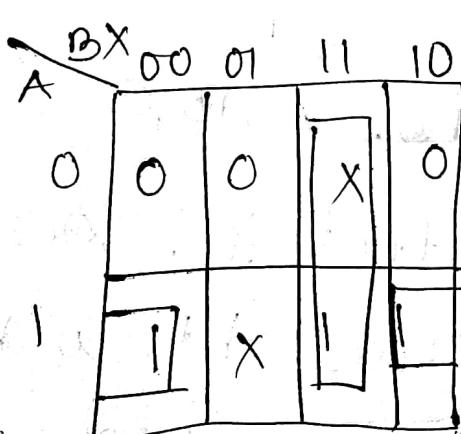
$$Y = \overline{A} X.$$

Prob3

R.S. / I/P.			N.S.	D _A	D _B
A	B	X	AB		
0	0	0	00	0	0
0	0	1	01	0	X
0	1	0	01	0	1
0	1	1	11	⊕X	1
1	0	0	10	1	0
1	0	1	00	⊕X	0
1	1	0	11	1	1
1	1	1	10	(01)	X

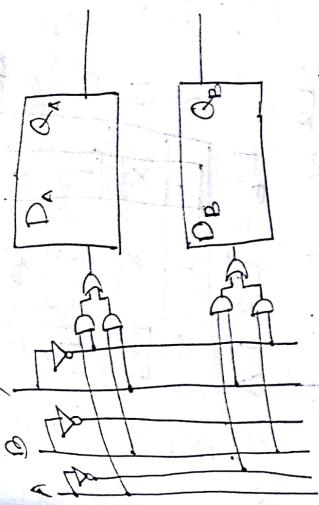
$$D_A = A \overline{X} + BX$$

$$D_B = \overline{A} X + BX$$



$$D_A = BX + A\overline{X}$$

$$D_B = \overline{A} X + BX$$



AB	Cx	00	01	11	10
00	0	1		1	0
01	0	0	0	0	0
11	x	x	x	x	x
10	0	0	x	x	x

$$D_A = \overline{A}\overline{B}x$$

AB	Cx	00	01	11	10
00	1	0	0	0	0
01	1	0	1	0	0
11	x	x	x	x	x
10	1	1	x	x	x

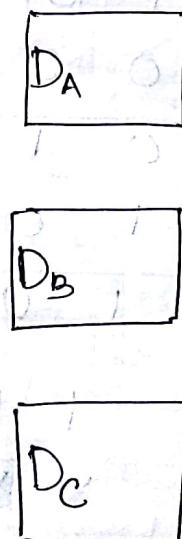
$$D_B = \overline{C}\overline{x} + A + BCx$$

AB	Cx	00	01	11	10
00	1	0	0	1	1
01	0	0	0	1	1
11	x	x	x	x	x
10	0	1	x	x	x

AB	Cx	00	01	11	10
00	0	1	1	0	0
01	0	1	1	0	0
11	x	x	x	x	x
10	0	0	x	x	x

$$D_C = BCx \quad C\overline{x} + Ax + \overline{AB}\overline{x}$$

$$Y = \overline{A}x$$

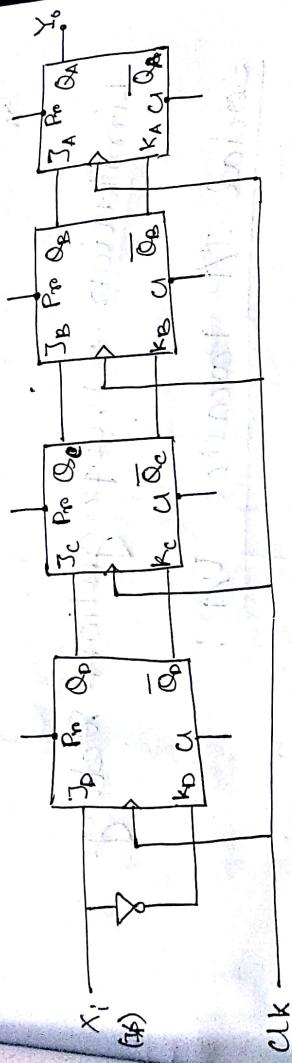


Shift Register

1. SISO \rightarrow Serial I/P Serial O/P
2. SIPO \rightarrow Serial I/P Parallel O/P
3. PI SO
4. PI PO

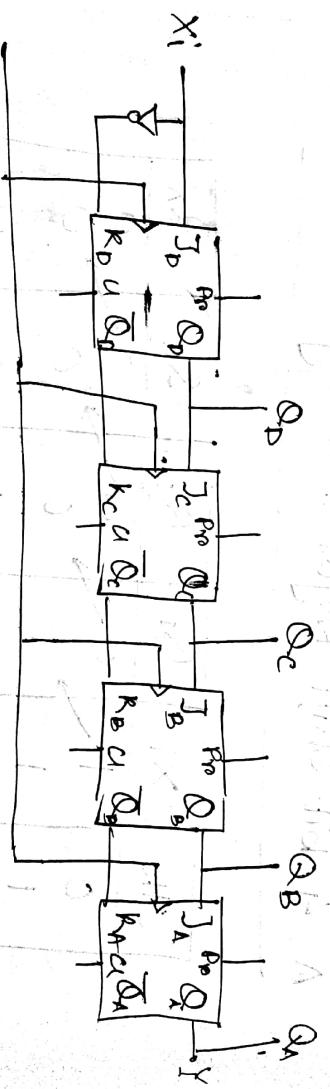
Date: 6.9.18

1. Serial I/P Serial O/P
-ve edge triggered JK F.F.



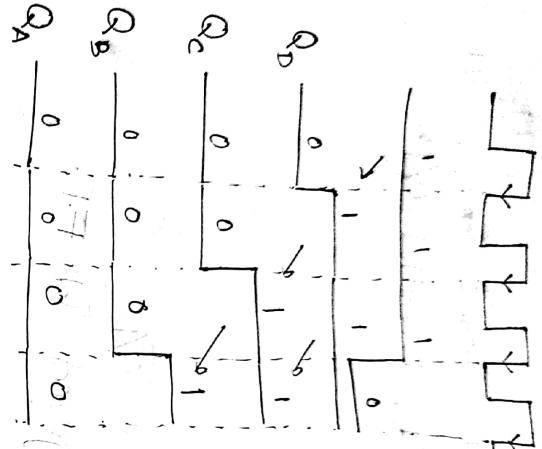
A 4 bit Shift Register using JK F.F.

Clk	X _i	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄
0	-	0	0	0	0	0
1	1	1	0	0	0	0
2	1	1	1	0	0	0
3	0	1	1	1	0	0
4	-	-	-	-	-	-

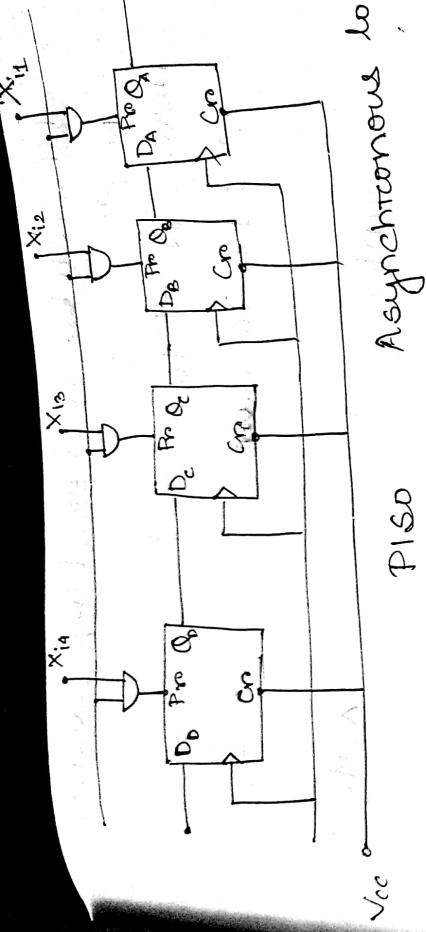


Social T/P Parallel D/P:

Limitation \rightarrow Propagation Delay



Prop \rightarrow Present
Cl \rightarrow Clear



PISO

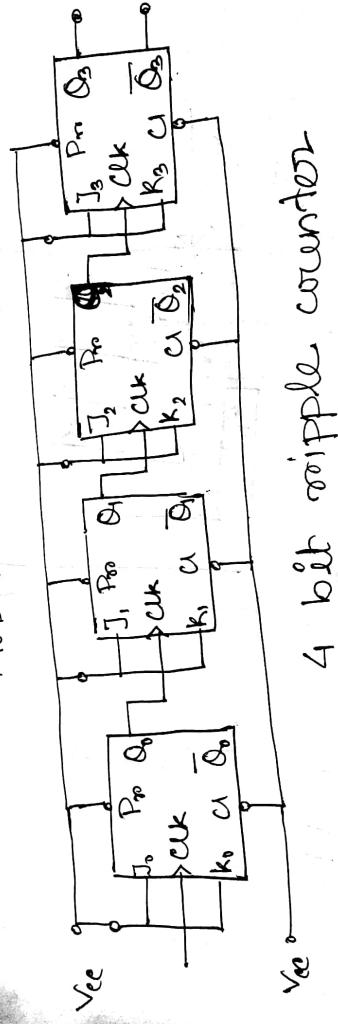
Asynchronous loading

If preset is 0, the output will be 1.

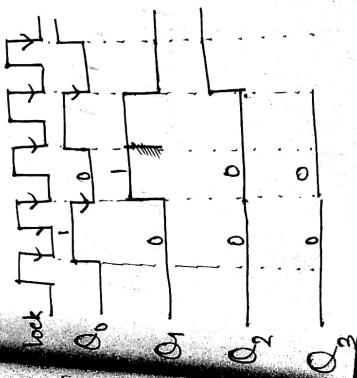
Rate: 12.918

Counter

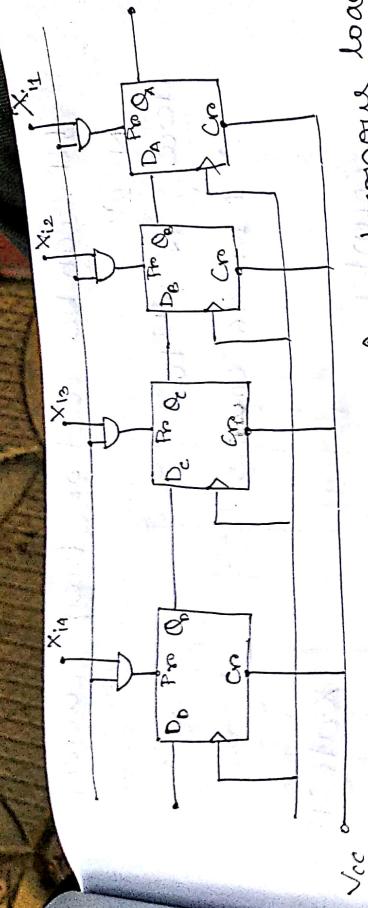
1. Asynchronous Counter / Ripple Counter
2. Synchronous Counter
MOD-N Counter



4 bit ripple counter



After 15 clock pulses all the F.F.s are reset.
will be set,
disadvantage:
Speed limitation, freq. lim.



Asynchronous loading

PISO

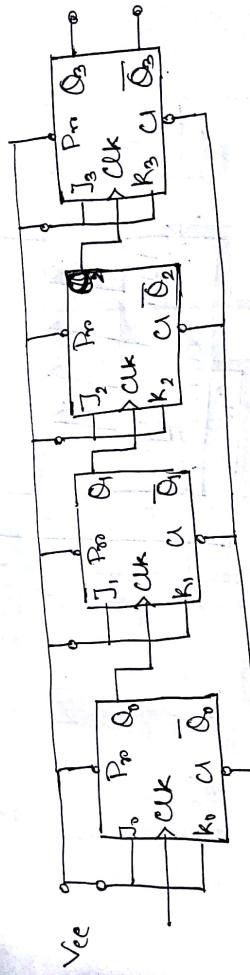
If preset is 0, the output will be 1.

Date: 12.9.18

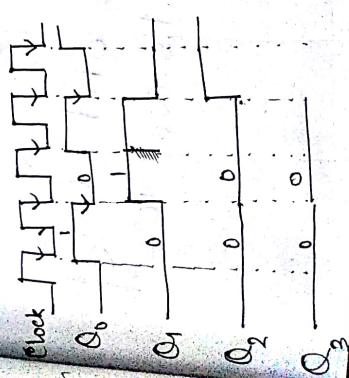
Counter

Counter / Ripple

1. Asynchronous Counter
2. Synchronous Counter
3. MOD-N Counter



4 bit ripple counter



After 15 clock pulses all
the F.F.s will preset.
will be 0000.

Disadvantage:
Speed limitation, freq. lim.

F.F. can be used as freq. division.

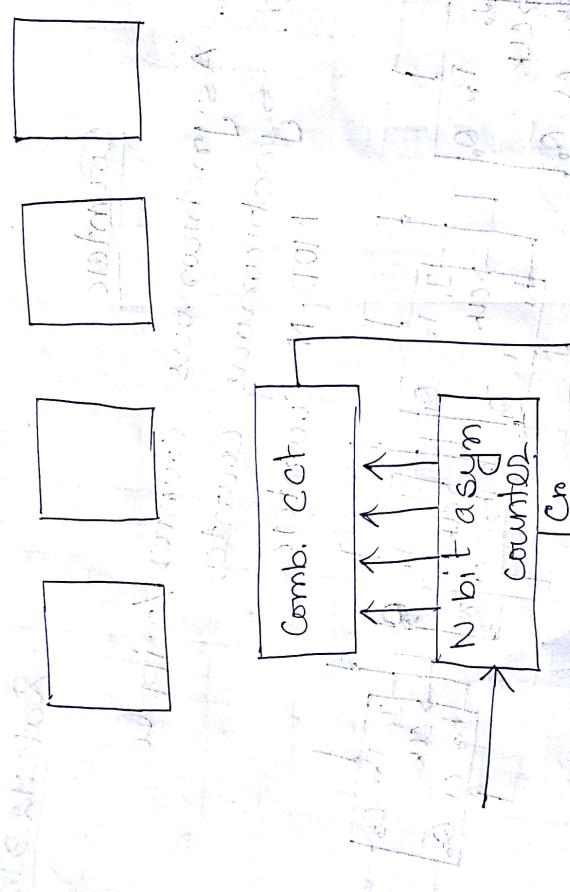
$$N = 2^n$$

Here, $N = 2^4 = 16$

MOD-16 counter

Counterclockwise

Up counter / down counter



Date: 13.9.14

Step 1: Find the min no of FFS required

Step 2: Prep. the sequence and design the comb. clk s.t. all the F.F.s. are reset after n clock pulses.

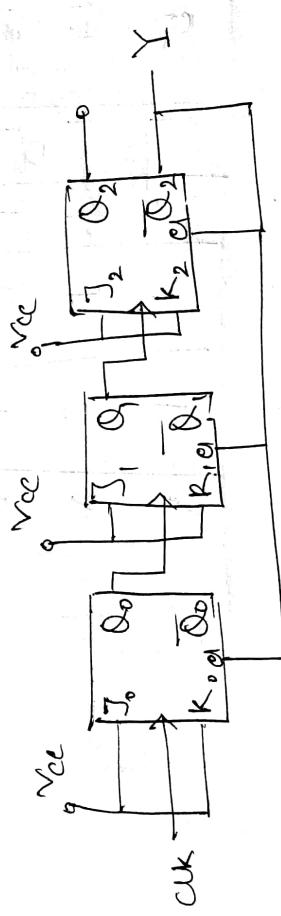
(a) Write down the TT of ripple counter, $Y = 1$ from valid state, $= 0$ for invalid.

clock	Q_2	Q_1	Q_0	Y
0	0	0	0	-
1	0	0	1	-
2	0	1	0	-
3	0	1	1	X
4	1	1	1	X
5	1	0	0	-
6	1	0	1	-
7	1	1	0	X

13.9.14

Q_2	Q_1	Q_0	on	off	10
0	1	1	X	X	1
1	0	1	X	X	0

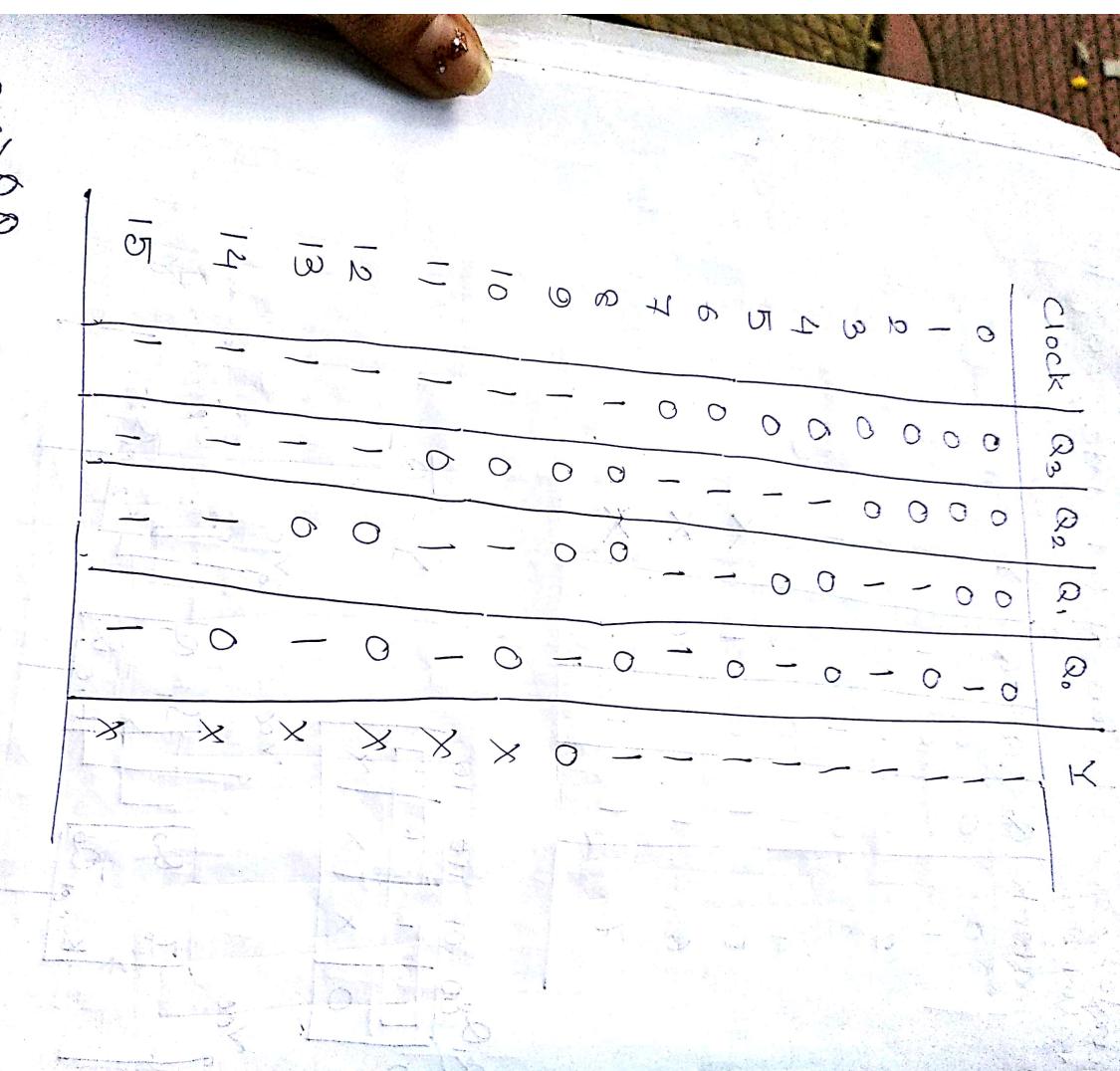
$$Y = \overline{Q_2}$$

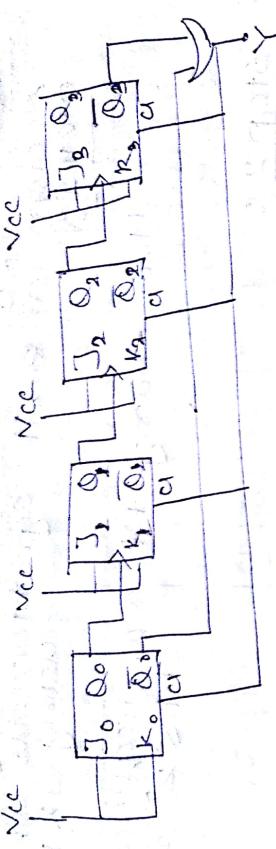


MOD-9

10	11	01	00	00	01	11	10
-	X	-	-	-	-	-	-
-	X	-	-	-	-	-	-
0	X	-	-	-	-	-	-
X	X	-	-	-	-	-	-
X	X	-	-	-	-	-	-

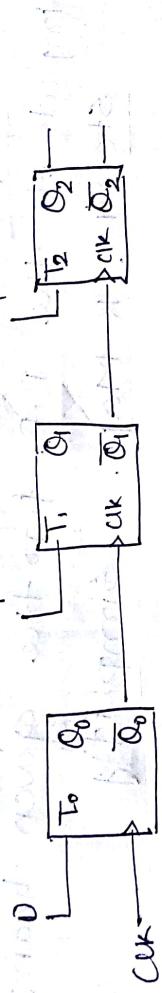
$$K = \frac{1}{\varrho + \varrho}$$





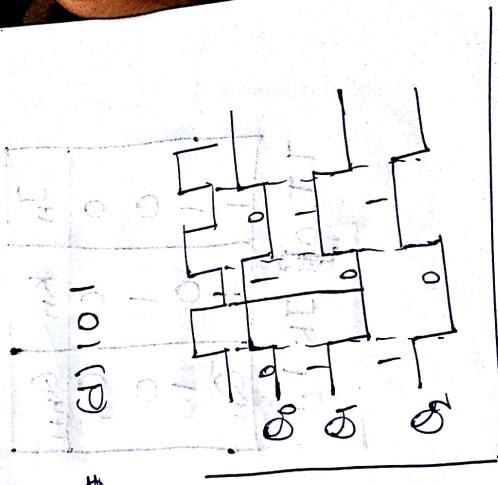
Rate: 14.918

Prob 1



Q_0, Q_1, Q_2

(a) 101 (b) 100 (c) 111 (d) 101



Procedure

Synchronous F.F. design
Design a 3 bit synchronous counter
Step 1:

How many F.F. are required
 $M \leq 2^n$ $n = P_R$

Step 2:

Write the sequence in the form of present state and next state.

Step 3: Excitation Table, find the inputs of the F.F. for the given transition

Step 4: K-Map, Simplify

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	0
1	1	Q_n

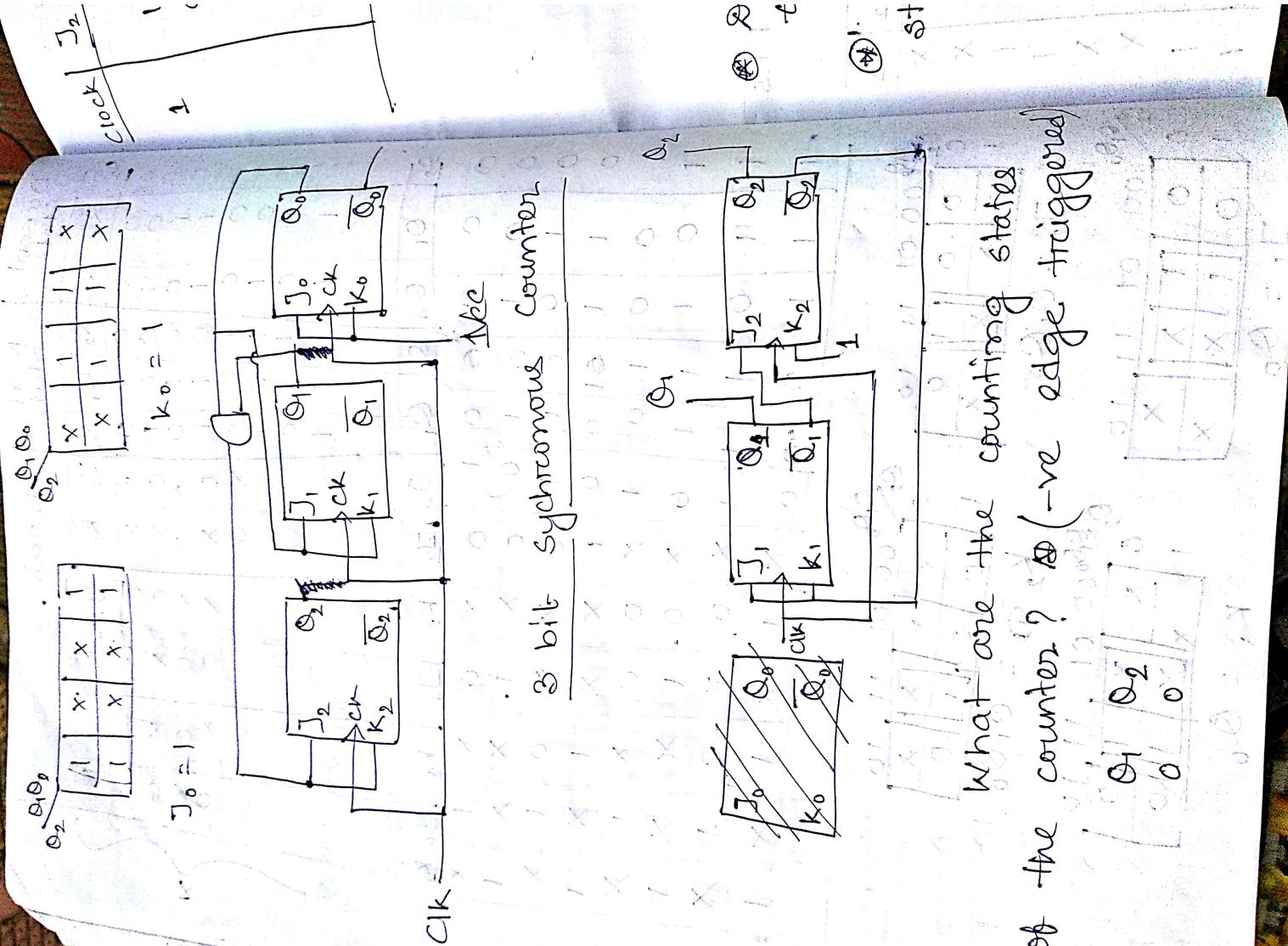
Present i/p Q_n	Next o/p Q_{n+1}	T/P	
		J_n	K_n
0	0	0	X
0	1	1	X
1	0	0	X
1	1	1	0

T.T. of JK F.F.

Present State	Inputs	Next State
Q_0^0	X 0 X 0	Q_1^0
Q_0^-	0 X 0 X	Q_1^-
Q_1^0	X X 0 0	Q_2^0
Q_1^-	0 0 X X	Q_2^-
Q_2^0	X X X X 0	Q_3^0
Q_2^-	0 0 0 0 X	Q_3^-
Q_3^0	0 - 0 - 0 - 0 -	Q_4^0
Q_3^-	0 0 - - 0 0 - -	Q_4^-
Q_4^0	0 0 0 0 - - - -	Q_5^0
Q_4^-	0 - 0 - 0 - 0 -	Q_5^-
Q_5^0	0 0 - - 0 0 - -	Q_6^0
Q_5^-	0 0 0 0 - - - -	Q_6^-
Q_6^0	X - X - X - X -	Q_7^0
Q_6^-	- X - X - X - X	Q_7^-
Q_7^0	X X 0 - X X 0 -	Q_8^0
Q_7^-	0 - X X 0 - X X	Q_8^-
Q_8^0	X X X X 0 0 0 -	Q_9^0
Q_8^-	0 0 0 - X X X X	Q_9^-
Q_9^0	- 0 - 0 - 0 - 0 -	Q_{10}^0
Q_9^-	0 - 1 0 - 0 - 0 -	Q_{10}^-
Q_{10}^0	0 0 0 1 0 - 1 - -	Q_{11}^0
Q_{10}^-	0 1 0 - 0 - 0 -	Q_{11}^-
Q_{11}^0	0 0 - - 0 0 - -	Q_{12}^0
Q_{11}^-	0 0 0 0 - - - -	Q_{12}^-

X	O
X	-
X	O
X	O

	X	X
-1	X	X
-1	-1	-1
0	O	O
0	O	-1

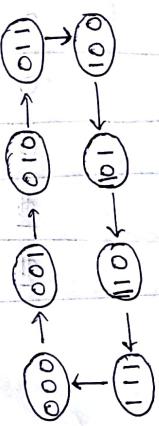


What are the counting states of the counter? (→ edge triggered)

clock	$J_2\ K_2$		$J_1\ K_1$		$Q_2\ Q_1$	
	1	0	1	0	0	1
1	1	1	1	0	0	1
0	0	1	0	1	1	0
1	1	0	0	1	0	1
0	0	1	1	0	1	0
1	1	1	1	1	1	1
0	0	0	0	0	0	0

Rate: 10.9.18

State Diagram of a 3 bit counter



J-K F.F.

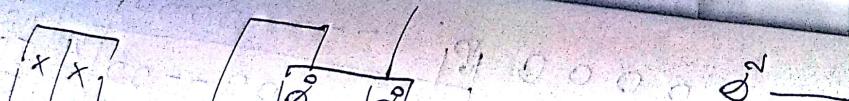
- ② Design a sequential generator using J-K F.F. to generate the sequence $0 \rightarrow 2 \rightarrow 4 \rightarrow 5 \rightarrow 1 \rightarrow 7 \rightarrow 6$

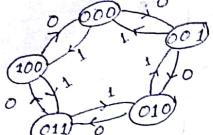
③ Design a MOD-5 up/down counter using

- ④ Design a MOD-5 up/down counter using state table and diagram.

input signal:

- $X \rightarrow$ input signal
- $X = 0 \rightarrow$ up counter
- $X = 1 \rightarrow$ down counter





State Table

Present State			Next State						Q ₀		
			X=0			X=1			Q ₀		
Q ₂	Q ₁	Q ₀	Q ₂	Q ₁	Q ₀	Q ₂	Q ₁	Q ₀	Q ₂	Q ₁	Q ₀
0	0	0	0	0	1	1	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0	0
0	1	0	0	1	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
.

Excitation Table

Present State		I/P	Next State			I/P's of that F.S.							
Q ₂	Q ₁	Q ₀	X	Q ₂	Q ₁	Q ₀	J ₀	K ₀	J ₁	K ₁	J ₂	K ₂	
0	0	0	0	0	0	1	0	X	0	X	1	X	
0	0	0	1	1	0	0	1	X	0	X	0	X	
0	0	1	0	0	1	0	0	X	1	X	X	1	
0	0	1	1	0	0	0	0	X	0	X	X	1	
0	1	0	0	0	1	1	0	X	X	1	1	X	
0	1	0	1	0	0	1	0	X	X	1	1	X	
0	1	1	0	1	0	0	1	X	X	1	X	1	
0	1	1	1	0	1	0	0	X	X	0	X	1	

I	0	0	0	1	0	0	0	0	1	0	0	0	X
Q ₂	Q ₁	Q ₀	X	Q ₂	Q ₁	Q ₀	Q ₂	Q ₁	Q ₀	Q ₂	Q ₁	Q ₀	
00	00	00	0	11	11	10	00	01	11	10	11	10	
01	01	01	1	11	11	10	01	01	11	10	11	10	
11	11	11	0	11	11	10	11	11	11	10	11	10	
10	10	10	1	11	11	10	10	11	11	10	11	10	

$$J_0 = \bar{Q}_0 \bar{Q}_1 X + Q_0 Q_1 \bar{Q}_2 X$$

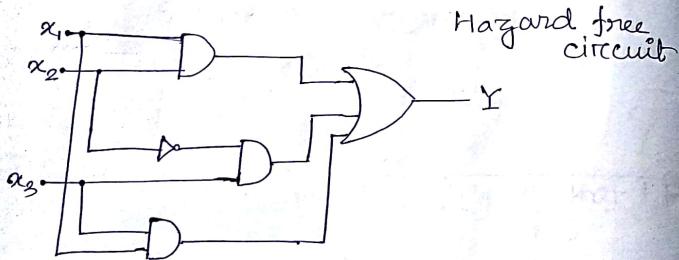
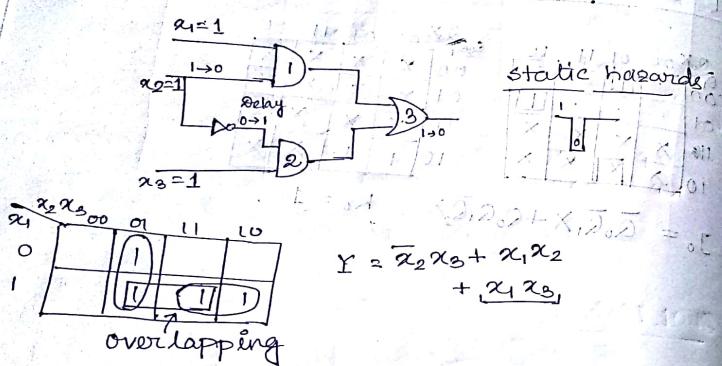
$$K_0 = 1$$

and so on



Hazards in combinational circuit

Date: 20.9.18



Digital Integrated Circuits

RTL, DTL, TTL, ECL - Bipolar Logic.
MOS, CMOS - Unipolar Logic

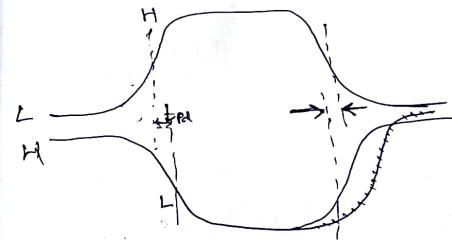
1. fan-out / Fan-in
2. Power dissipation
3. Propagation Delay
4. Noise margin

Power Dissipation:

$$= V_{cc} \times I_{cc(\text{avg})}$$

$$I_{cc(\text{avg})} = \frac{I_L + I_H}{2}$$

Propagation Delay:



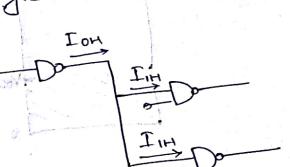
Noise margin:

Date: 27.9.18

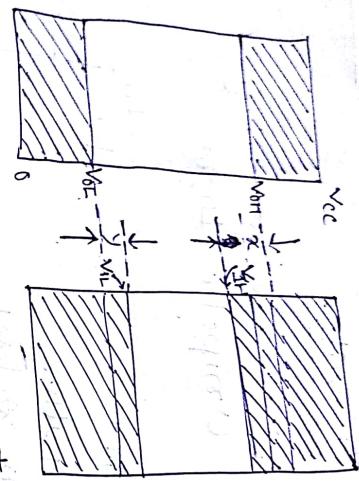
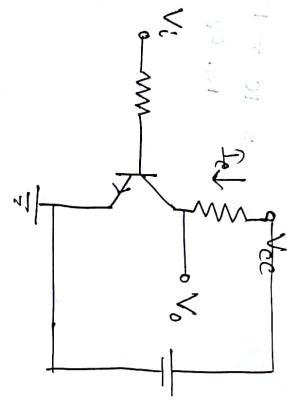
Digital Integrated Circuits

RTL, DTL, TTL, ECL - Bipolar Logic.
MOS, CMOS - Unipolar Logic

1. fan-out / Fan-in
2. Power dissipation
3. Propagation Delay
4. Noise margin

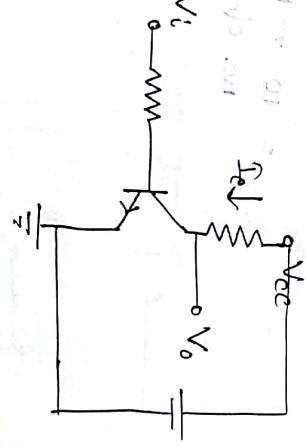


$$\begin{aligned} \text{Fan out} &= \frac{I_{OH}}{I_{IH}} \\ &= \frac{400 \mu\text{A}}{40 \mu\text{A}} \\ &= 10 \leftarrow \text{Max no. of gates} \end{aligned}$$



$\frac{V_0}{V_{ce}} = T_c R_c$

obj. n. sp. Bade. 1. 10. 8



$$V_o = V_{cc} - I_c R_c$$

Accidental Date: 1.10.18

