CSE331 HOMEWORK #3 REPORT

BİLAL YALÇINKAYA

Half_adder: XOR inputs for sum and AND for carry out.

Full_adder: Calls first half adder then uses its carry out for next adder.

ADD32: Adds 1 bit numbers 32 times according to previous adders cout.

AND32: AND 1 bit numbers 32 times, assign it to result.

OR32: OR 1 bit numbers 32 times, assign it to result.

XOR32: XOR 1 bit numbers 32 times, assign it to result.

Complement2s: Adds 1 to not(!) of input.

SUB32: Finds 2s complement of second number and adds it to first number since these are signed numbers.

SLT32: First uses SUB32 to a-b for result then Checks for overflow situation with couts and xor it with results last bit, according to that last bit of result will be 0 or 1.

NOT32: NOT 1 bit numbers 32 times, assign it to result;

NOR32: NOR 1 bit numbers 32 times, assign it to result.

MUX2: Choices between 2 input according to choice input. Mux32 and mux64 uses this module 32 or 64 times also.

MUX3: (3bit)8x1 mux choses proper result.

ALU32: First finds all possible results, assigns them to 8bit 32 wires to use it after with mux then calls mux3 32 times to assign proper result according to choice input.

ShiftR: Shifts input to right 1 bit.

Control: According to reset,clock,p0,done and currentState it will generates nextState according to state table.

Datapath: First if write is 0 then adds product 0, else adds multiplicand to product. Shifts product and if shift is 1 shifts 1 bit, else shifts 0 bit which will decided by mux then adds counter 1 if shift input is 1.

Mult32: After initializing variables it goes to control module to get what we gonna do and with them it goes to datapath to get next step of multiplication. Adds multiplicand step by step to result which we learned at course. If counter reaches 31, input done will be 1 and product will be assigned to result so alu32 can use it.

My mult32 can runs only 1 time even after i change the inputs it will give previous result. So i need to compile again for another input. I couldn't solve that problem.

ModelSim ALTERA STARTER EDITION 10.1d

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Library

Name	Type	Path
work	Library	rtl_work
add32	Module	C:/diger/altera/13.1/co/add32.v
alu32	Module	C:/diger/altera/13.1/co/alu32.v
and32	Module	C:/diger/altera/13.1/co/and32.v
Complement2s	Module	C:/diger/altera/13.1/co/Complement2s.v
control	Module	C:/diger/altera/13.1/co/control.v
datapath	Module	C:/diger/altera/13.1/co/datapath.v
full_adder	Module	C:/diger/altera/13.1/co/full_adder.v
half_adder	Module	C:/diger/altera/13.1/co/half_adder.v
mult32	Module	C:/diger/altera/13.1/co/mult32.v
mux2	Module	C:/diger/altera/13.1/co/mux2.v
mux3	Module	C:/diger/altera/13.1/co/mux3.v
mux32	Module	C:/diger/altera/13.1/co/mux32.v
mux64	Module	C:/diger/altera/13.1/co/mux64.v
nor32	Module	C:/diger/altera/13.1/co/nor32.v
not32	Module	C:/diger/altera/13.1/co/not32.v
or32	Module	C:/diger/altera/13.1/co/or32.v
shiftR	Module	C:/diger/altera/13.1/co/shiftR.v
slt32	Module	C:/diger/altera/13.1/co/slt32.v
sub32	Module	C:/diger/altera/13.1/co/sub32.v
testbench_add3...	Module	C:/diger/altera/13.1/co/testbench_ad...
testbench_alu32	Module	C:/diger/altera/13.1/co/testbench_alu...
testbench_and3...	Module	C:/diger/altera/13.1/co/testbench_an...
testbench_mult3...	Module	C:/diger/altera/13.1/co/testbench_mu...
testbench_nor3...	Module	C:/diger/altera/13.1/co/testbench_no...
testbench_or32	Module	C:/diger/altera/13.1/co/testbench_or...
testbench_slt32	Module	C:/diger/altera/13.1/co/testbench_slt...
testbench_sub3...	Module	C:/diger/altera/13.1/co/testbench_su...
testbench_xor3...	Module	C:/diger/altera/13.1/co/testbench_xo...
top	Module	C:/diger/altera/13.1/co/top.v
xor32	Module	C:/diger/altera/13.1/co/xor32.v

Objects

Name	Value	Kind	Mode
FN	00000000000000000000000000001111101	Pack...	Internal
SN	11111111111111111111111111000001	Pack...	Internal
result	00000000000000000000000000111110	Net	Internal

ADD32

sim - Default

Instance	Desig
testbench_add32	testb
add_test	add32
#vsim_capacity#	

Wave - Default

Msgs

Now 0.1 ns

Cursor 1 0 ns

0.5 ns 1 ns

0.00 ns

Transcript

```
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module testbench_xor32
#
# Top level modules:
#       testbench_xor32
ModelSim> vsim work.testbench_add32
# vsim work.testbench_add32
# Loading work.testbench_add32
# Loading work.add32
# Loading work.full_adder
# Loading work.half_adder
VSIM 12> run
# time =  0, First Number = 00000000000000000000000001111101 |         125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 00000000000000000000000010111100 |         188
# time = 20, First Number = 11111111111111111111111110000011 |        -125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 11111111111111111111111111000010 |         -62
# time = 40, First Number = 11111111111111111111111110000011 |        -125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 11111111111111111111111101000100 |        -188
# time = 60, First Number = 00000000000000000000000001111101 |         125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 00000000000000000000000000111110 |          62

VSIM 13>
```

Now: 100 ps Delta: 0 work

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and32	Module	C:/diger/altera/13.1/co/and32.v
Complement2s	Module	C:/diger/altera/13.1/co/Complement2s.v
control	Module	C:/diger/altera/13.1/co/control.v
datapath	Module	C:/diger/altera/13.1/co/datapath.v
full_adder	Module	C:/diger/altera/13.1/co/full_adder.v
half_adder	Module	C:/diger/altera/13.1/co/half_adder.v
mult32	Module	C:/diger/altera/13.1/co/mult32.v
mux2	Module	C:/diger/altera/13.1/co/mux2.v
mux3	Module	C:/diger/altera/13.1/co/mux3.v
mux32	Module	C:/diger/altera/13.1/co/mux32.v
mux64	Module	C:/diger/altera/13.1/co/mux64.v
nor32	Module	C:/diger/altera/13.1/co/nor32.v
not32	Module	C:/diger/altera/13.1/co/not32.v
or32	Module	C:/diger/altera/13.1/co/or32.v
shiftR	Module	C:/diger/altera/13.1/co/shiftR.v
slt32	Module	C:/diger/altera/13.1/co/slt32.v
sub32	Module	C:/diger/altera/13.1/co/sub32.v
testbench_add3...	Module	C:/diger/altera/13.1/co/testbench_ad...
testbench_alu32	Module	C:/diger/altera/13.1/co/testbench_alu...
testbench_and3...	Module	C:/diger/altera/13.1/co/testbench_an...
testbench_mult3...	Module	C:/diger/altera/13.1/co/testbench_mu...
testbench_nor3...	Module	C:/diger/altera/13.1/co/testbench_no...
testbench_or32	Module	C:/diger/altera/13.1/co/testbench_or...
testbench_slt32	Module	C:/diger/altera/13.1/co/testbench_slt...
testbench_sub3...	Module	C:/diger/altera/13.1/co/testbench_su...
testbench_xor3...	Module	C:/diger/altera/13.1/co/testbench_xo...
top	Module	C:/diger/altera/13.1/co/top.v
xor32	Module	C:/diger/altera/13.1/co/xor32.v

Objects

Name	Value	Kind	Mode
ALUop	111	Pack...	Internal
FN	00000111000101010111000010000000101	Pack...	Internal
SN	11111111111111111111111111000000001	Pack...	Internal
result	11111111111111111111111000000101	Net	Internal

ALU32

sim - Default

Instance	Desig
testbench_alu32	testb
#vsim_capacity#	

Wave - Default

Msgs

Now 400 ps

Cursor 1 0 ps

500 ps

0 ps

Transcript

```
# ALUOP: 000 = +, 001 = xor, 010 = -, 011 = *, 100 = slt, 101 = nor, 110 = and, 111 = or
#
# time =  0, ALUop = 000, First Number = 00000000000000100011000100000101 |      287237, Second Number = 00100000000100001001000000011001 |   537956377, RESULT = 00100000000101001111001000011110 |   538243614
# time = 20, ALUop = 000, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |       -511, RESULT = 00000111000101011100000000000110 |   118865926
# time = 40, ALUop = 001, First Number = 00000000000000100011000100000101 |      287237, Second Number = 00100000000100001001000000011001 |   537956377, RESULT = 00100000000101001111001000011100 |   538243612
# time = 60, ALUop = 001, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |       -511, RESULT = 11111000111010100011110000000100 |  -118866940
# time = 80, ALUop = 010, First Number = 00000000000000100011000100000101 |      287237, Second Number = 00100000000100001001000000011001 |   537956377, RESULT = 11011111111110011110100011101100 |  -537669140
run
# time = 100, ALUop = 010, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |       -511, RESULT = 00000111000101011100010000000100 |   118866948
# time = 120, ALUop = 100, First Number = 00000000000000100011000100000101 |      287237, Second Number = 00100000000100001001000000011001 |   537956377, RESULT = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1 |           X
# time = 140, ALUop = 100, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |       -511, RESULT = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0 |           X
# time = 160, ALUop = 101, First Number = 00000000000000100011000100000101 |      287237, Second Number = 00100000000100001001000000011001 |   537956377, RESULT = 11011111111101011000011011100010 |  -538243614
# time = 180, ALUop = 101, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |       -511, RESULT = 00000000000000000000000111111010 |         506
run
# time = 200, ALUop = 110, First Number = 00000000000000100011000100000101 |      287237, Second Number = 00100000000100001001000000011001 |   537956377, RESULT = 00000000000000000000000000000001 |           1
# time = 220, ALUop = 110, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |       -511, RESULT = 00000111000101011100001000000001 |   118866433
# time = 240, ALUop = 111, First Number = 00000000000000100011000100000101 |      287237, Second Number = 00100000000100001001000000011001 |   537956377, RESULT = 00100000000101001111001000011101 |   538243613
# time = 260, ALUop = 111, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |       -511, RESULT = 11111111111111111111111000000101 |        -507
VSIM 15>
```

Now: 400 ps Delta: 2 | sim:/testbench_alu32 | 0 ps to 1 ns

4°C Clear TUR 22:25 19.12.2021

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and32	Module	C:/diger/altera/13.1/co/and32.v
Complement2s	Module	C:/diger/altera/13.1/co/Complement2s.v
control	Module	C:/diger/altera/13.1/co/control.v
datapath	Module	C:/diger/altera/13.1/co/datapath.v
full_adder	Module	C:/diger/altera/13.1/co/full_adder.v
half_adder	Module	C:/diger/altera/13.1/co/half_adder.v
mult32	Module	C:/diger/altera/13.1/co/mult32.v
mux2	Module	C:/diger/altera/13.1/co/mux2.v
mux3	Module	C:/diger/altera/13.1/co/mux3.v
mux32	Module	C:/diger/altera/13.1/co/mux32.v
mux64	Module	C:/diger/altera/13.1/co/mux64.v
nor32	Module	C:/diger/altera/13.1/co/nor32.v
not32	Module	C:/diger/altera/13.1/co/not32.v
or32	Module	C:/diger/altera/13.1/co/or32.v
shiftR	Module	C:/diger/altera/13.1/co/shiftR.v
slt32	Module	C:/diger/altera/13.1/co/slt32.v
sub32	Module	C:/diger/altera/13.1/co/sub32.v
testbench_add3...	Module	C:/diger/altera/13.1/co/testbench_ad...
testbench_alu32	Module	C:/diger/altera/13.1/co/testbench_alu...
testbench_and3...	Module	C:/diger/altera/13.1/co/testbench_an...
testbench_mult3...	Module	C:/diger/altera/13.1/co/testbench_mu...
testbench_nor3...	Module	C:/diger/altera/13.1/co/testbench_no...
testbench_or32	Module	C:/diger/altera/13.1/co/testbench_or...
testbench_slt32	Module	C:/diger/altera/13.1/co/testbench_slt...
testbench_sub3...	Module	C:/diger/altera/13.1/co/testbench_su...
testbench_xor3...	Module	C:/diger/altera/13.1/co/testbench_xo...
top	Module	C:/diger/altera/13.1/co/top.v
xor32	Module	C:/diger/altera/13.1/co/xor32.v

Objects

Name	Value	Kind	Mode
FN	00000000000000000000000001111101	Pack...	Internal
SN	11111111111111111111111111000001	Pack...	Internal
result	00000000000000000000000001000001	Net	Internal

AND32

sim - Default

Instance	Desig
testbench_and32	testb
and32_test	and32
#vsim_capacity#	

Wave - Default

Msgs

Now 100 ps

Cursor 1 0 ps

500 ps

0 ps

Transcript

```
# time = 180, ALUop = 101, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |        -511, RESULT = 00000000000000000000000111111010 |         506
run
# time = 200, ALUop = 110, First Number = 00000000000001000110001000000101 |      287237, Second Number = 00100000000100001001000000011001 |   537956377, RESULT = 00000000000000000000000000000001 |           1
# time = 220, ALUop = 110, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |        -511, RESULT = 00000111000101011100001000000001 |   118866433
# time = 240, ALUop = 111, First Number = 00000000000001000110001000000101 |      287237, Second Number = 00100000000100001001000000011001 |   537956377, RESULT = 00100000000101001111001000011101 |   538243613
# time = 260, ALUop = 111, First Number = 00000111000101011100001000000101 |   118866437, Second Number = 11111111111111111111111000000001 |        -511, RESULT = 11111111111111111111111000000101 |        -507
run
VSIM 15> vsim work.testbench_and32
VSIM 15> work.testbench_and32
# Loading work.testbench_and32
# Loading work.and32
VSIM 16> run
# time =  0, First Number = 00000000000000000000000001111101 |         125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 00000000000000000000000000111101 |          61
# time = 20, First Number = 11111111111111111111111111000011 |        -125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 00000000000000000000000000000011 |           3
# time = 40, First Number = 11111111111111111111111111000011 |        -125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 11111111111111111111111110000001 |        -127
# time = 60, First Number = 00000000000000000000000001111101 |         125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 00000000000000000000000001000001 |          65

VSIM 17>
```

Now: 100 ps Delta: 0 | Module

4°C Clear TUR 22:25 19.12.2021

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Library

Name	Type	Path
work	Library	rtl_work
add32	Module	C:/diger/altera/13.1/co/add32.v
alu32	Module	C:/diger/altera/13.1/co/alu32.v
and32	Module	C:/diger/altera/13.1/co/and32.v
Complement2s	Module	C:/diger/altera/13.1/co/Complement2s.v
control	Module	C:/diger/altera/13.1/co/control.v
datapath	Module	C:/diger/altera/13.1/co/datapath.v
full_adder	Module	C:/diger/altera/13.1/co/full_adder.v
half_adder	Module	C:/diger/altera/13.1/co/half_adder.v
mult32	Module	C:/diger/altera/13.1/co/mult32.v
mux2	Module	C:/diger/altera/13.1/co/mux2.v
mux3	Module	C:/diger/altera/13.1/co/mux3.v
mux32	Module	C:/diger/altera/13.1/co/mux32.v
mux64	Module	C:/diger/altera/13.1/co/mux64.v
nor32	Module	C:/diger/altera/13.1/co/nor32.v
not32	Module	C:/diger/altera/13.1/co/not32.v
or32	Module	C:/diger/altera/13.1/co/or32.v
shiftR	Module	C:/diger/altera/13.1/co/shiftR.v
slt32	Module	C:/diger/altera/13.1/co/slt32.v
sub32	Module	C:/diger/altera/13.1/co/sub32.v
testbench_add3...	Module	C:/diger/altera/13.1/co/testbench_ad...
testbench_alu32	Module	C:/diger/altera/13.1/co/testbench_alu...
testbench_and3...	Module	C:/diger/altera/13.1/co/testbench_an...
testbench_mult3...	Module	C:/diger/altera/13.1/co/testbench_mu...
testbench_nor3...	Module	C:/diger/altera/13.1/co/testbench_no...
testbench_or32	Module	C:/diger/altera/13.1/co/testbench_or...
testbench_slt32	Module	C:/diger/altera/13.1/co/testbench_slt...
testbench_sub3...	Module	C:/diger/altera/13.1/co/testbench_su...
testbench_xor3...	Module	C:/diger/altera/13.1/co/testbench_xo...
top	Module	C:/diger/altera/13.1/co/top.v
xor32	Module	C:/diger/altera/13.1/co/xor32.v

Objects

Name	Value	Kind	Mode
FN	00000000000000000000000000111101	Pack...	Internal
SN	11111111111111111111111111000001	Pack...	Internal
result	00000000000000000000000000000010	Net	Internal

NOR32

sim - Default

Instance	Desig
testbench_nor32	testb
#vsim_capacity#	

Wave - Default

Msgs

Now 100 ps

Cursor 1 0 ps

500 ps

Transcript

```
# Loading work.and32
VSIM 16> run
# time =  0, First Number = 00000000000000000000000000111101 |         125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 00000000000000000000000000111101 |          61
# time = 20, First Number = 11111111111111111111111111000011 |        -125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 00000000000000000000000000000011 |           3
# time = 40, First Number = 11111111111111111111111111000011 |        -125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 11111111111111111111111110000001 |        -127
# time = 60, First Number = 00000000000000000000000000111101 |         125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 00000000000000000000000001000001 |          65
VSIM 17> vsim work.testbench_nor32
# vsim work.testbench_nor32
# Loading work.testbench_nor32
# Loading work.nor32
# Loading work.not32
VSIM 18> run
# time =  0, First Number = 00000000000000000000000000111101 |         125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 11111111111111111111111110000000 |        -128
# time = 20, First Number = 11111111111111111111111111000011 |        -125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 00000000000000000000000001000000 |          64
# time = 40, First Number = 11111111111111111111111111000011 |        -125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 00000000000000000000000000111100 |          60
# time = 60, First Number = 00000000000000000000000000111101 |         125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 00000000000000000000000000000010 |           2

VSIM 19>
```

Now: 100 ps Delta: 0 | sim:/testbench_nor32 | 0 ps to 1 ns

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mult32	Module	C:/diger/altera/13.1/co/mult32.v
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mux3	Module	C:/diger/altera/13.1/co/mux3.v
mux32	Module	C:/diger/altera/13.1/co/mux32.v
mux64	Module	C:/diger/altera/13.1/co/mux64.v
nor32	Module	C:/diger/altera/13.1/co/nor32.v
not32	Module	C:/diger/altera/13.1/co/not32.v
or32	Module	C:/diger/altera/13.1/co/or32.v
shiftR	Module	C:/diger/altera/13.1/co/shiftR.v
slt32	Module	C:/diger/altera/13.1/co/slt32.v
sub32	Module	C:/diger/altera/13.1/co/sub32.v
testbench_add3...	Module	C:/diger/altera/13.1/co/testbench_ad...
testbench_alu32	Module	C:/diger/altera/13.1/co/testbench_alu...
testbench_and3...	Module	C:/diger/altera/13.1/co/testbench_an...
testbench_mult3...	Module	C:/diger/altera/13.1/co/testbench_mu...
testbench_nor3...	Module	C:/diger/altera/13.1/co/testbench_no...
testbench_or32	Module	C:/diger/altera/13.1/co/testbench_or...
testbench_slt32	Module	C:/diger/altera/13.1/co/testbench_slt...
testbench_sub3...	Module	C:/diger/altera/13.1/co/testbench_su...
testbench_xor3...	Module	C:/diger/altera/13.1/co/testbench_xo...
top	Module	C:/diger/altera/13.1/co/top.v
xor32	Module	C:/diger/altera/13.1/co/xor32.v

Objects

Name	Value	Kind	Mode
FN	00000000000000000000000000111101	Pack...	Internal
SN	00000000000000000000000000111111	Pack...	Internal
result	00000000000000000001111011000011	Net	Internal

MULT32

sim - Default

Instance	Desig
testbench_mult32	testb
c	mult3
#vsim_capacity#	

Wave - Default

Msgs

Now 1100 ps

Cursor 1 0 ps

500 ps 1000 ps

Transcript

```
# Loading work.Complement2s
# Loading work.not32
VSIM 20> run
# FOR MULTIPLICATION PRESS 'run -all' OR KEEP RUNNING UNTIL #1000
#
run
run
run
run
run
run
run
run
run
run
VSIM 21> run
# time = 1000, First Number = 00000000000000000000000001111101 |         125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 00000000000000000001111011000011 |        7875

VSIM 21>
```

Now: 1,100 ps Delta: 2

C:/diger/altera/13.1/co/testbench_alu32.v

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ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rtl_work
add32	Module	C:/diger/altera/13.1/co/add32.v
alu32	Module	C:/diger/altera/13.1/co/alu32.v
and32	Module	C:/diger/altera/13.1/co/and32.v
Complement2s	Module	C:/diger/altera/13.1/co/Complement2s.v
control	Module	C:/diger/altera/13.1/co/control.v
datapath	Module	C:/diger/altera/13.1/co/datapath.v
full_adder	Module	C:/diger/altera/13.1/co/full_adder.v
half_adder	Module	C:/diger/altera/13.1/co/half_adder.v
mult32	Module	C:/diger/altera/13.1/co/mult32.v
mux2	Module	C:/diger/altera/13.1/co/mux2.v
mux3	Module	C:/diger/altera/13.1/co/mux3.v
mux32	Module	C:/diger/altera/13.1/co/mux32.v
mux64	Module	C:/diger/altera/13.1/co/mux64.v
nor32	Module	C:/diger/altera/13.1/co/nor32.v
not32	Module	C:/diger/altera/13.1/co/not32.v
or32	Module	C:/diger/altera/13.1/co/or32.v
shiftR	Module	C:/diger/altera/13.1/co/shiftR.v
slt32	Module	C:/diger/altera/13.1/co/slt32.v
sub32	Module	C:/diger/altera/13.1/co/sub32.v
testbench_add3...	Module	C:/diger/altera/13.1/co/testbench_ad...
testbench_alu32	Module	C:/diger/altera/13.1/co/testbench_alu...
testbench_and3...	Module	C:/diger/altera/13.1/co/testbench_an...
testbench_mult3...	Module	C:/diger/altera/13.1/co/testbench_mu...
testbench_nor3...	Module	C:/diger/altera/13.1/co/testbench_no...
testbench_or32	Module	C:/diger/altera/13.1/co/testbench_or...
testbench_slt32	Module	C:/diger/altera/13.1/co/testbench_slt...
testbench_sub3...	Module	C:/diger/altera/13.1/co/testbench_su...
testbench_xor3...	Module	C:/diger/altera/13.1/co/testbench_xo...
top	Module	C:/diger/altera/13.1/co/top.v
xor32	Module	C:/diger/altera/13.1/co/xor32.v

Objects

Name	Value	Kind	Mode
FN	00000000000000000000000001111101	Pack...	Internal
SN	11111111111111111111111111000001	Pack...	Internal
result	11111111111111111111111111111101	Net	Internal

OR32

sim - Default

Instance	Desig
testbench_or32	testb
#vsim_capacity#	

Wave - Default

Msgs

Now 100 ps

Cursor 1 0 ps

500 ps

Transcript

```
run
run
run
run
run
run
# time = 1000, First Number = 00000000000000000000000001111101 |         125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 00000000000000000001111011000011 |        7875
VSIM 21> vsim work.testbench_or32
VSIM 21> work.testbench_or32
# Loading work.testbench_or32
# Loading work.or32
VSIM 22> run
# time =   0, First Number = 00000000000000000000000001111101 |         125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 00000000000000000000000001111111 |         127
# time =  20, First Number = 11111111111111111111111111000011 |        -125, Second Number = 00000000000000000000000000111111 |          63, RESULT = 11111111111111111111111111111111 |          -65
# time =  40, First Number = 11111111111111111111111111000011 |        -125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 11111111111111111111111111000011 |          -61
# time =  60, First Number = 00000000000000000000000001111101 |         125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 11111111111111111111111111111101 |           -3

VSIM 23>
```

Now: 100 ps Delta: 0 | sim:/testbench_or32 | 0 ps to 1 ns

4°C Clear TUR 22:27 19.12.2021

ModelSim ALTERA STARTER EDITION 10.1d

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Library

Name	Type	Path
work	Library	rtl_work
add32	Module	C:/diger/altera/13.1/co/add32.v
alu32	Module	C:/diger/altera/13.1/co/alu32.v
and32	Module	C:/diger/altera/13.1/co/and32.v
Complement2s	Module	C:/diger/altera/13.1/co/Complement2s.v
control	Module	C:/diger/altera/13.1/co/control.v
datapath	Module	C:/diger/altera/13.1/co/datapath.v
full_adder	Module	C:/diger/altera/13.1/co/full_adder.v
half_adder	Module	C:/diger/altera/13.1/co/half_adder.v
mult32	Module	C:/diger/altera/13.1/co/mult32.v
mux2	Module	C:/diger/altera/13.1/co/mux2.v
mux3	Module	C:/diger/altera/13.1/co/mux3.v
mux32	Module	C:/diger/altera/13.1/co/mux32.v
mux64	Module	C:/diger/altera/13.1/co/mux64.v
nor32	Module	C:/diger/altera/13.1/co/nor32.v
not32	Module	C:/diger/altera/13.1/co/not32.v
or32	Module	C:/diger/altera/13.1/co/or32.v
shiftR	Module	C:/diger/altera/13.1/co/shiftR.v
slt32	Module	C:/diger/altera/13.1/co/slt32.v
sub32	Module	C:/diger/altera/13.1/co/sub32.v
testbench_add3...	Module	C:/diger/altera/13.1/co/testbench_ad...
testbench_alu32	Module	C:/diger/altera/13.1/co/testbench_alu...
testbench_and3...	Module	C:/diger/altera/13.1/co/testbench_an...
testbench_mult3...	Module	C:/diger/altera/13.1/co/testbench_mu...
testbench_nor3...	Module	C:/diger/altera/13.1/co/testbench_no...
testbench_or32	Module	C:/diger/altera/13.1/co/testbench_or...
testbench_slt32	Module	C:/diger/altera/13.1/co/testbench_slt...
testbench_sub3...	Module	C:/diger/altera/13.1/co/testbench_su...
testbench_xor3...	Module	C:/diger/altera/13.1/co/testbench_xo...
top	Module	C:/diger/altera/13.1/co/top.v
xor32	Module	C:/diger/altera/13.1/co/xor32.v

Objects

Name	Value	Kind	Mode
FN	00000000000000000000000001111101	Pack...	Internal
SN	11111111111111111111111111000001	Pack...	Internal
result	zzzzzzzzzzzzzzzzzzzzzzzzzzzzzzz0	Net	Internal

SLT32

sim - Default

Instance	Desig
testbench_slt32	testb
slt_test	slt32
#vsim_capacity#	

Wave - Default

Msgs

Now 100 ps

Cursor 1 0 ps

500 ps

0 ps

Transcript

```
# time = 40, First Number = 11111111111111111111111110000011 |        -125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 11111111111111111111111111000011 |         -61
# time = 60, First Number = 00000000000000000000000001111101 |         125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 11111111111111111111111111111101 |          -3
VSIM 23> vsim work.testbench_slt32
# vsim work.testbench_slt32
# Loading work.testbench_slt32
# Loading work.slt32
# Loading work.Complement2s
# Loading work.not32
# Loading work.add32
# Loading work.full_adder
# Loading work.half_adder
VSIM 24> run
# time =  0, First Number = 00000000000000000000000001111101 |         125, Second Number = 00000000000000000000000001111111 |          63, RESULT = 0 | 0
# time = 20, First Number = 11111111111111111111111110000011 |        -125, Second Number = 00000000000000000000000001111111 |          63, RESULT = 1 | 1
# time = 40, First Number = 11111111111111111111111110000011 |        -125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 1 | 1
# time = 60, First Number = 00000000000000000000000001111101 |         125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 0 | 0

VSIM 25>
```

Now: 100 ps Delta: 0 sim:/testbench_slt32

4°C Clear TUR 22:27 19.12.2021

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SUB32

```
# time = 40, First Number = 11111111111111111111111111000011 |       -125, Second Number = 11111111111111111111111111000001 |        -63, RESULT = 1 | 1
# time = 60, First Number = 00000000000000000000000001111101 |        125, Second Number = 11111111111111111111111111000001 |        -63, RESULT = 0 | 0
VSIM 25> vsim work.testbench_sub32
# vsim work.testbench_sub32
# Loading work.testbench_sub32
# Loading work.sub32
# Loading work.Complement2s
# Loading work.not32
# Loading work.add32
# Loading work.full_adder
# Loading work.half_adder
VSIM 26> run
# time =  0, First Number = 00000000000000000000000001111101 |        125, Second Number = 00000000000000000000000000111111 |         63, RESULT = 00000000000000000000000001111110 |         62
# time = 20, First Number = 11111111111111111111111111000011 |       -125, Second Number = 00000000000000000000000000111111 |         63, RESULT = 11111111111111111111111110000100 |       -188
# time = 40, First Number = 11111111111111111111111111000011 |       -125, Second Number = 11111111111111111111111111000001 |        -63, RESULT = 11111111111111111111111111000010 |        -62
# time = 60, First Number = 00000000000000000000000001111101 |        125, Second Number = 11111111111111111111111111000001 |        -63, RESULT = 00000000000000000000000010111100 |        188

VSIM 27>
```

Now: 100 ps Delta: 0 | sim:/testbench_sub32 | 0 ps to 1 ns

4°C Clear TUR 22:28 19.12.2021

ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rtl_work
add32	Module	C:/diger/altera/13.1/co/add32.v
alu32	Module	C:/diger/altera/13.1/co/alu32.v
and32	Module	C:/diger/altera/13.1/co/and32.v
Complement2s	Module	C:/diger/altera/13.1/co/Complement2s.v
control	Module	C:/diger/altera/13.1/co/control.v
datapath	Module	C:/diger/altera/13.1/co/datapath.v
full_adder	Module	C:/diger/altera/13.1/co/full_adder.v
half_adder	Module	C:/diger/altera/13.1/co/half_adder.v
mult32	Module	C:/diger/altera/13.1/co/mult32.v
mux2	Module	C:/diger/altera/13.1/co/mux2.v
mux3	Module	C:/diger/altera/13.1/co/mux3.v
mux32	Module	C:/diger/altera/13.1/co/mux32.v
mux64	Module	C:/diger/altera/13.1/co/mux64.v
nor32	Module	C:/diger/altera/13.1/co/nor32.v
not32	Module	C:/diger/altera/13.1/co/not32.v
or32	Module	C:/diger/altera/13.1/co/or32.v
shiftR	Module	C:/diger/altera/13.1/co/shiftR.v
slt32	Module	C:/diger/altera/13.1/co/slt32.v
sub32	Module	C:/diger/altera/13.1/co/sub32.v
testbench_add3...	Module	C:/diger/altera/13.1/co/testbench_ad...
testbench_alu32	Module	C:/diger/altera/13.1/co/testbench_alu...
testbench_and3...	Module	C:/diger/altera/13.1/co/testbench_an...
testbench_mult3...	Module	C:/diger/altera/13.1/co/testbench_mu...
testbench_nor3...	Module	C:/diger/altera/13.1/co/testbench_no...
testbench_or32	Module	C:/diger/altera/13.1/co/testbench_or...
testbench_slt32	Module	C:/diger/altera/13.1/co/testbench_slt...
testbench_sub3...	Module	C:/diger/altera/13.1/co/testbench_su...
testbench_xor3...	Module	C:/diger/altera/13.1/co/testbench_xo...
top	Module	C:/diger/altera/13.1/co/top.v
xor32	Module	C:/diger/altera/13.1/co/xor32.v

Objects

Name	Value	Kind	Mode
FN	00000000000000000000000001111101	Pack...	Internal
SN	11111111111111111111111111000001	Pack...	Internal
result	11111111111111111111111110111100	Net	Internal

XOR32

sim - Default

Instance	Desig
testbench_xor32	testb
xor32_test	xor32
#vsim_capacity#	

Wave - Default

Msgs

Now 100 ps

Cursor 1 0 ps

500 ps

Transcript

```
# Loading work.full_adder
# Loading work.half_adder
VSIM 26> run
VSIM 26> =  0, First Number = 00000000000000000000000001111101 |         125, Second Number = 00000000000000000000000001111111 |          63, RESULT = 00000000000000000000000011111110 |          62
# time = 20, First Number = 11111111111111111111111110000011 |        -125, Second Number = 00000000000000000000000001111111 |          63, RESULT = 11111111111111111111111101000100 |        -188
# time = 40, First Number = 11111111111111111111111110000011 |        -125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 11111111111111111111111111000010 |         -62
# time = 60, First Number = 00000000000000000000000001111101 |         125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 00000000000000000000000010111100 |         188
VSIM 27> vsim work.testbench_xor32
# vsim work.testbench_xor32
# Loading work.testbench_xor32
# Loading work.xor32
VSIM 28> run
# time =  0, First Number = 00000000000000000000000001111101 |         125, Second Number = 00000000000000000000000001111111 |          63, RESULT = 00000000000000000000000001000010 |          66
# time = 20, First Number = 11111111111111111111111110000011 |        -125, Second Number = 00000000000000000000000001111111 |          63, RESULT = 11111111111111111111111110111100 |         -68
# time = 40, First Number = 11111111111111111111111110000011 |        -125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 00000000000000000000000001000010 |          66
# time = 60, First Number = 00000000000000000000000001111101 |         125, Second Number = 11111111111111111111111111000001 |         -63, RESULT = 11111111111111111111111110111100 |         -68

VSIM 29>
```

Now: 100 ps Delta: 0 sim:/testbench_xor32

4°C Clear TUR 22:28 19.12.2021