

Projeto - Detector de Maioria

COMP0416 - Fundamentos de Sistemas
Digitais - Turma 01

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Descrição

Projetar um circuito com quatro entradas A,B,C,D e uma saída X com a seguinte característica, **só e somente** se a maioria das entradas estiver no nível lógico 1 a saída X deve ir para o estado 1, em todos os outros casos a saída X deve estar em 0.

Tabela Verdade - Produto da Soma

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

$$(\bar{A} + \bar{B} + \bar{C} + \bar{D})$$

$$(\bar{A} + \bar{B} + \bar{C} + D)$$

$$(\bar{A} + \bar{B} + C + \bar{D})$$

$$(\bar{A} + \bar{B} + C + D)$$

$$(\bar{A} + B + \bar{C} + \bar{D})$$

$$(\bar{A} + B + \bar{C} + D)$$

$$(\bar{A} + B + C + \bar{D})$$

$$(A + \bar{B} + \bar{C} + \bar{D})$$

$$(A + \bar{B} + \bar{C} + D)$$

$$(A + \bar{B} + C + \bar{D})$$

$$(A + B + \bar{C} + \bar{D})$$

$$(A + B + C + D)$$

Expressões - Produto da Soma

$$(\overline{A}+\overline{B}+\overline{C}+\overline{D}) \longrightarrow (\overline{A}.\overline{B}) + (\overline{A}.\overline{C}) + (\overline{B}.\overline{C}) + (\overline{A}.\overline{D}) + (\overline{B}.\overline{D}) + (\overline{C}.\overline{D})$$

$$(\overline{A}+\overline{B}+\overline{C}+D) \longrightarrow (\overline{A}.\overline{B}) + (\overline{A}.\overline{C}) + (\overline{B}.\overline{C})$$

$$(\overline{A}+\overline{B}+C+\overline{D}) \longrightarrow (\overline{A}.\overline{B}) + (\overline{A}.\overline{D}) + (\overline{B}.\overline{D})$$

$$(\overline{A}+\overline{B}+C+D) \longrightarrow (\overline{A}.\overline{B})$$

$$(\overline{A}+B+\overline{C}+\overline{D}) \longrightarrow (\overline{A}.\overline{C}) + (\overline{A}.\overline{D}) + (\overline{C}.\overline{D})$$

$$(\overline{A}+B+\overline{C}+D) \longrightarrow (\overline{A}.\overline{C})$$

$$(\overline{A}+B+C+\overline{D}) \longrightarrow (\overline{A}.\overline{D})$$

$$\overline{X} = \overline{A}.\overline{B} + \overline{A}.\overline{C} + \overline{B}.\overline{C} + \overline{A}.\overline{D} + \overline{B}.\overline{D} + \overline{C}.\overline{D} + A.B.C.D$$

$$(A+\overline{B}+\overline{C}+\overline{D}) \longrightarrow (\overline{B}.\overline{C}) + (\overline{B}.\overline{D}) + (\overline{C}.\overline{D})$$

$$(A+\overline{B}+\overline{C}+D) \longrightarrow (\overline{B}.\overline{C})$$

$$(A+\overline{B}+C+\overline{D}) \longrightarrow (\overline{B}.\overline{D})$$

$$(A+B+\overline{C}+\overline{D}) \longrightarrow (\overline{C}.\overline{D})$$

$$(A+B+C+D) \longrightarrow (A.B.C.D)$$

Expressões - Produto da Soma

$$\overline{X} = \overline{A}.\overline{B} + \overline{A}.\overline{C} + \overline{B}.\overline{C} + \overline{A}.\overline{D} + \overline{B}.\overline{D} + \overline{C}.\overline{D} + A.B.C.D$$



$$\overline{\overline{X}} = \overline{\overline{A}.\overline{B} + \overline{A}.\overline{C} + \overline{B}.\overline{C} + \overline{A}.\overline{D} + \overline{B}.\overline{D} + \overline{C}.\overline{D} + A.B.C.D}$$



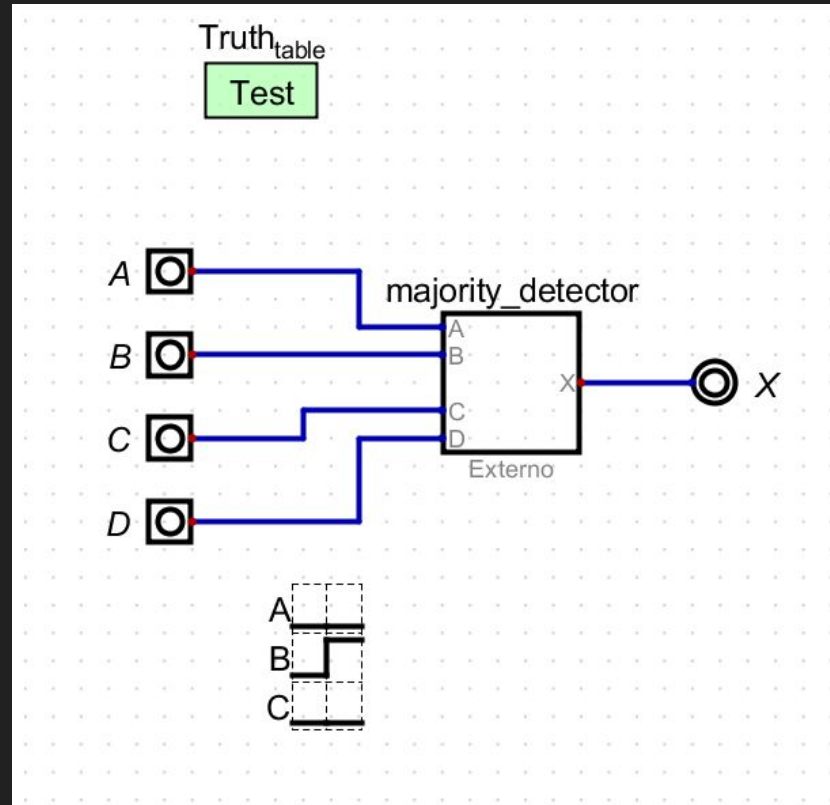
$$X = (A + B) . (A + C) . (B + C) . (A + D) . (B + D) . (C + D) . (\overline{A} + \overline{B} + \overline{C} + \overline{D})$$

Implementação - VHDL

Código de programa:

```
1 library IEEE;
2 use IEEE.std_logic_1164.all;
3
4 ENTITY majority_detector IS
5 PORT (
6     A: in std_logic;
7     B: in std_logic;
8     C: in std_logic;
9     D: in std_logic;
10    X: out std_logic
11 );
12
13 END majority_detector;
14
15 ARCHITECTURE logic_function OF majority_detector IS
16 BEGIN
17
18     X<= (A OR B)
19         AND (A OR C)
20         AND (B OR C)
21         AND (A OR D)
22         AND (B OR D)
23         AND (C OR D)
24         AND (NOT A OR NOT B OR NOT C OR NOT D);
25
26 END logic_function;
```

Integração - Digital



Integração - Digital

The screenshot displays a digital logic simulation environment. At the top, a toolbar contains various icons for simulation and editing. Two dialog boxes are open:

- Caso de teste (Test Case):** The 'Rótulo' (Label) field is set to 'Truth_table'. The 'Dados para teste' (Test Data) section has 'Editar' and 'Editar em separado' buttons. The 'Habilitado' (Enabled) checkbox is checked. 'Ajuda' (Help), 'Cancelar' (Cancel), and 'OK' buttons are at the bottom.
- Dados para teste (Test Data):** This window displays a truth table for a majority gate with four inputs (A, B, C, D) and one output (X). The table lists 17 rows of data.

The main workspace shows a circuit diagram on a grid. Four input components labeled A, B, C, and D are connected to a majority gate component labeled 'majority'. The output of the gate is labeled 'X'. Below the circuit, a small timing diagram shows the waveforms for inputs A, B, and C over time.

	A	B	C	D	X
1	A	B	C	D	X
2	0	0	0	0	0
3	0	0	0	1	0
4	0	0	1	0	0
5	0	0	1	1	0
6	0	1	0	0	0
7	0	1	0	1	0
8	0	1	1	0	0
9	0	1	1	1	1
10	1	0	0	0	0
11	1	0	0	1	0
12	1	0	1	0	0
13	1	0	1	1	1
14	1	1	0	0	0
15	1	1	0	1	1
16	1	1	1	0	1
17	1	1	1	1	0

Testes - Tabela Verdade

Truth_{table}

Test

A B C D

A B C

Resultado de teste

Arquivo Visualizar

Truth_table com êxito

	A	B	C	D	X
L2	0	0	0	0	0
L3	0	0	0	1	0
L4	0	0	1	0	0
L5	0	0	1	1	0
L6	0	1	0	0	0
L7	0	1	0	1	0
L8	0	1	1	0	0
L9	0	1	1	1	1
L10	1	0	0	0	0
L11	1	0	0	1	0
L12	1	0	1	0	0
L13	1	0	1	1	1
L14	1	1	0	0	0
L15	1	1	0	1	1
L16	1	1	1	0	1
L17	1	1	1	1	0

Testes - Gráfico de Dados

Resultado de teste

Arquivo Visualizar

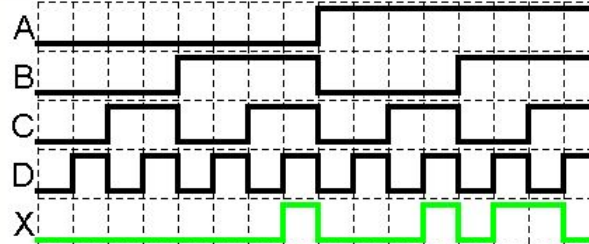
Truth_table com êxito

	A	B	C	D	X
L2	0	0	0	0	0
L3	0	0	0	1	0
L4	0	0	1	0	0
L5	0	0	1	1	0
L6	0	1	0	0	0
L7	0	1	0	1	0
L8	0	1	1	0	0
L9	0	1	1	1	1
L10	1	0	0	0	0
L11	1	0	0	1	0
L12	1	0	1	0	0
L13	1	0	1	1	1
L14	1	1	0	0	0
L15	1	1	0	1	1
L16	1	1	1	0	1
L17	1	1	1	1	0

ty_detector

Dados de teste Truth_table com êxito

Arquivo Visualizar Ajuda



Bibliografia

- ❑ Conteúdo didático e disponibilizado pelo professor.
- ❑ Ferramentas de software:
 - ❑ GHDL - <https://github.com/ghdl/ghdl>
 - ❑ Simulador Digital - <https://github.com/hneemann/Digital>
 - ❑ Mapa de Karnaugh online - <http://www.32x8.com/index.html>