Projeto - Detector de Maioria

COMP0416 - Fundamentos de Sistemas Digitais - Turma 01

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Descrição

Projetar um circuito com quatro entradas A,B,C,D e uma saída X com a seguinte característica, **só e somente** se a maioria das entradas estiver no nível lógico 1 a saída X deve ir para o estado 1, em todos os outros casos a saída X deve estar em 0.

Tabela Verdade - Produto da Soma

A	B	C	D	X	
0	0	0	0	0	$(\overline{A}+\overline{B}+\overline{C}+\overline{D})$
0	0	0	1	0	$(\overline{A}+\overline{B}+\overline{C}+D)$
0	0	1	0	0	$(\overline{A}+\overline{B}+C+\overline{D})$
0	0	1	1	0	$(\overline{A}+\overline{B}+C+D)$
0	1	0	0	0	$(\overline{A}+B+\overline{C}+\overline{D})$
0	1	0	1	0	$(\overline{A}+B+\overline{C}+D)$
0	1	1	0	0	$(\overline{A}+B+C+\overline{D})$
0	1	1	1	1	
1	0	0	0	0	$(A+\overline{B}+\overline{C}+\overline{D})$
1	0	0	1	0	$(A+\overline{B}+\overline{C}+D)$
1	0	1	0	0	$(A+\overline{B}+C+\overline{D})$
1	0	1	1	1	
1	1	0	0	0	$(A+B+\overline{C}+\overline{D})$
1	1	0	1	1	
1	1	1	0	1	
1	1	1	1	0	$(A+B+C+D)$

Expressões - Produto da Soma

$(\overline{A}+\overline{B}+\overline{C}+\overline{D}) \rightarrow (\overline{A}.\overline{B}) + (\overline{A}.\overline{C}) + (\overline{B}.\overline{C}) + (\overline{A}.\overline{D}) + (\overline{B}.\overline{D}) + (\overline{C}.\overline{D})$

$(\overline{A}+\overline{B}+\overline{C}+D) \rightarrow (\overline{A}.\overline{B}) + (\overline{A}.\overline{C}) + (\overline{B}.\overline{C})$

$(\overline{A}+\overline{B}+C+\overline{D}) \rightarrow (\overline{A}.\overline{B}) + (\overline{A}.\overline{D}) + (\overline{B}.\overline{D})$

$(\overline{A}+\overline{B}+C+D) \rightarrow (\overline{A}.\overline{B})$

$(\overline{A}+B+\overline{C}+\overline{D}) \rightarrow (\overline{A}.\overline{C}) + (\overline{A}.\overline{D}) + (\overline{C}.\overline{D})$

$(\overline{A}+B+\overline{C}+D) \rightarrow (\overline{A}.\overline{C})$

$(\overline{A}+B+C+\overline{D}) \rightarrow (\overline{A}.\overline{D})$

$(A+\overline{B}+\overline{C}+\overline{D}) \rightarrow (\overline{B}.\overline{C}) + (\overline{B}.\overline{D}) + (\overline{C}.\overline{D})$

$(A+\overline{B}+\overline{C}+D) \rightarrow (\overline{B}.\overline{C})$

$(A+\overline{B}+C+\overline{D}) \rightarrow (\overline{B}.\overline{D})$

$(A+B+\overline{C}+\overline{D}) \rightarrow (\overline{C}.\overline{D})$

$(A+B+C+D) \rightarrow (A.B.C.D)$

$\overline{X} = \overline{A}.\overline{B} + \overline{A}.\overline{C} + \overline{B}.\overline{C} + \overline{A}.\overline{D} + \overline{B}.\overline{D} + \overline{C}.\overline{D} + A.B.C.D$

Expressões - Produto da Soma

$$\overline{X} = \overline{A}.\overline{B} + \overline{A}.\overline{C} + \overline{B}.\overline{C} + \overline{A}.\overline{D} + \overline{B}.\overline{D} + \overline{C}.\overline{D} + A.B.C.D$$

$$\overline{\overline{X}} = \overline{\overline{A}.\overline{B} + \overline{A}.\overline{C} + \overline{B}.\overline{C} + \overline{A}.\overline{D} + \overline{B}.\overline{D} + \overline{C}.\overline{D} + A.B.C.D}$$

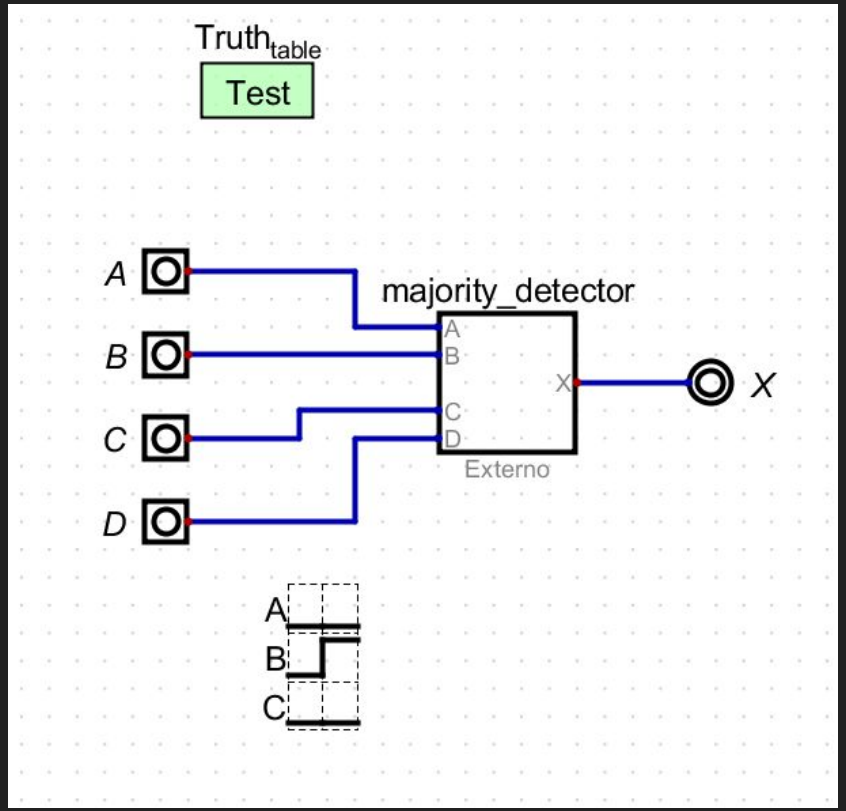
$$X = (A + B) . (A + C) . (B + C) . (A + D) . (B + D) . (C + D) . (\overline{A} + \overline{B} + \overline{C} + \overline{D})$$

Implementação - VHDL

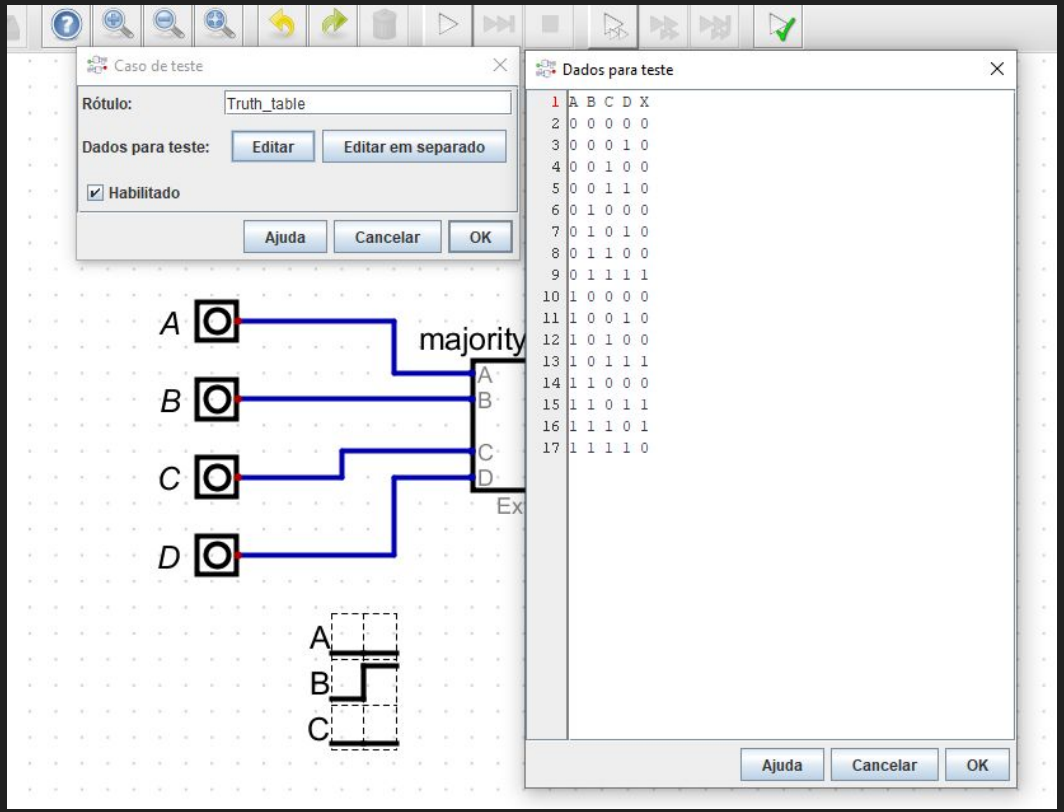
Código de programa:

```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  ENTITY majority_detector IS
5  PORT (
6          A: in std_logic;
7          B: in std_logic;
8          C: in std_logic;
9          D: in std_logic;
10         X: out std_logic
11       );
12
13 END majority_detector;
14
15 ARCHITECTURE logic_function OF majority_detector IS
16 BEGIN
17
18         X<= (A OR B)
19         AND (A OR C)
20         AND (B OR C)
21         AND (A OR D)
22         AND (B OR D)
23         AND (C OR D)
24         AND (NOT A OR NOT B OR NOT C OR NOT D);
25
26 END logic_function;
```

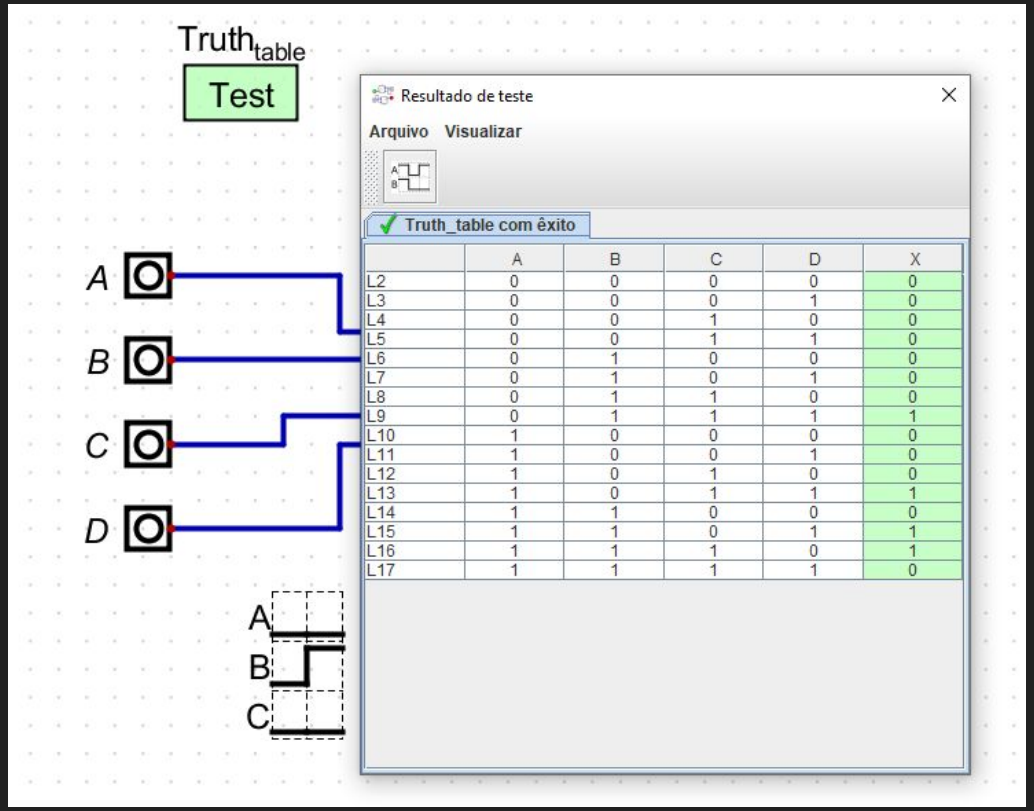
Integração - Digital



Integração - Digital

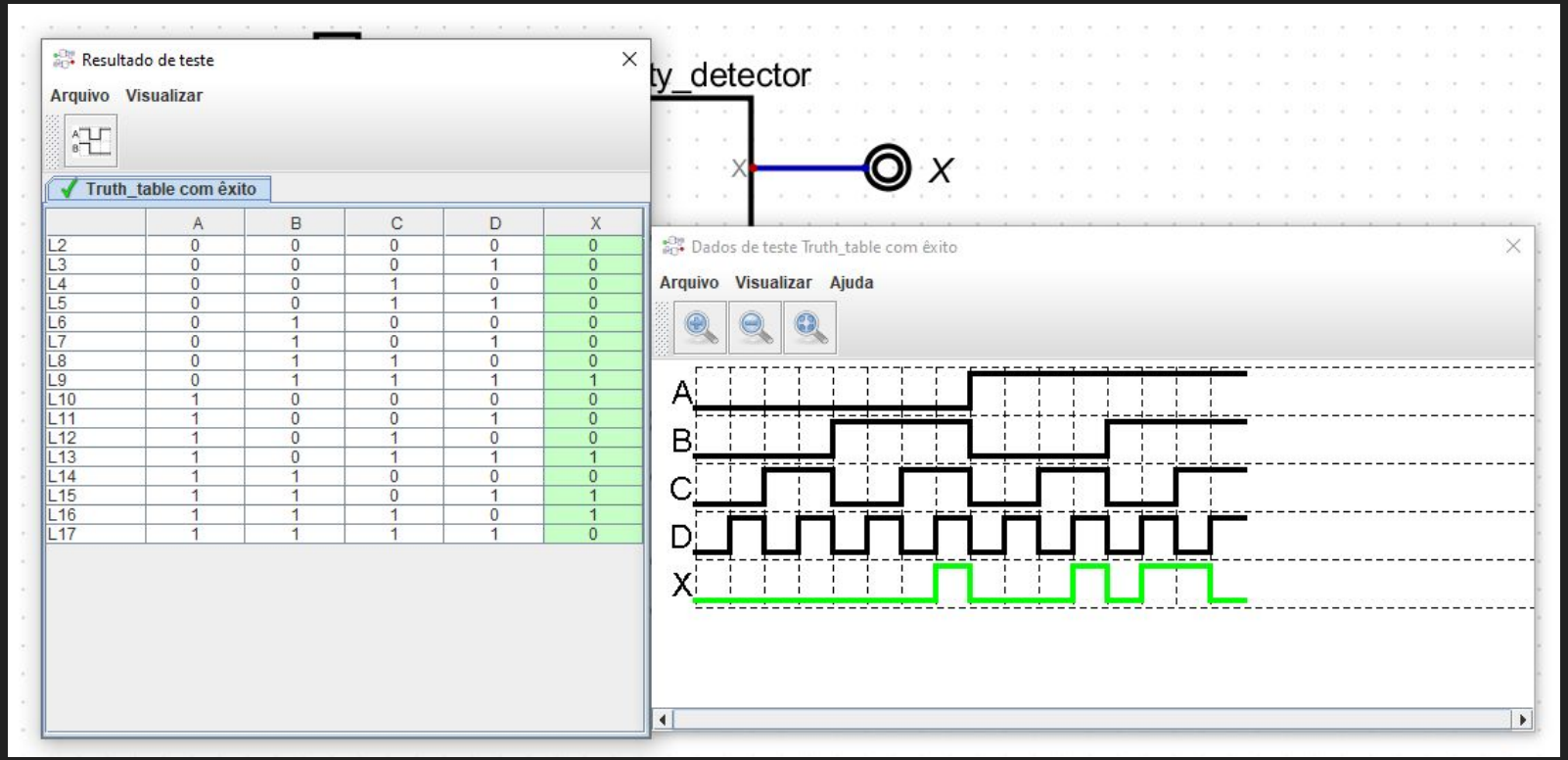


Testes - Tabela Verdade



	A	B	C	D	X
L2	0	0	0	0	0
L3	0	0	0	1	0
L4	0	0	1	0	0
L5	0	0	1	1	0
L6	0	1	0	0	0
L7	0	1	0	1	0
L8	0	1	1	0	0
L9	0	1	1	1	1
L10	1	0	0	0	0
L11	1	0	0	1	0
L12	1	0	1	0	0
L13	1	0	1	1	1
L14	1	1	0	0	0
L15	1	1	0	1	1
L16	1	1	1	0	1
L17	1	1	1	1	0

Testes - Gráfico de Dados



	A	B	C	D	X
L2	0	0	0	0	0
L3	0	0	0	1	0
L4	0	0	1	0	0
L5	0	0	1	1	0
L6	0	1	0	0	0
L7	0	1	0	1	0
L8	0	1	1	0	0
L9	0	1	1	1	1
L10	1	0	0	0	0
L11	1	0	0	1	0
L12	1	0	1	0	0
L13	1	0	1	1	1
L14	1	1	0	0	0
L15	1	1	0	1	1
L16	1	1	1	0	1
L17	1	1	1	1	0

Bibliografia

- Conteúdo didático e disponibilizado pelo professor.
- Ferramentas de software:
  - GHDL - https://github.com/ghdl/ghdl
  - Simulador Digital - https://github.com/hneemann/Digital
  - Mapa de Karnaugh online - http://www.32x8.com/index.html