Simulating virtual memory, TLB, Cache and man memory

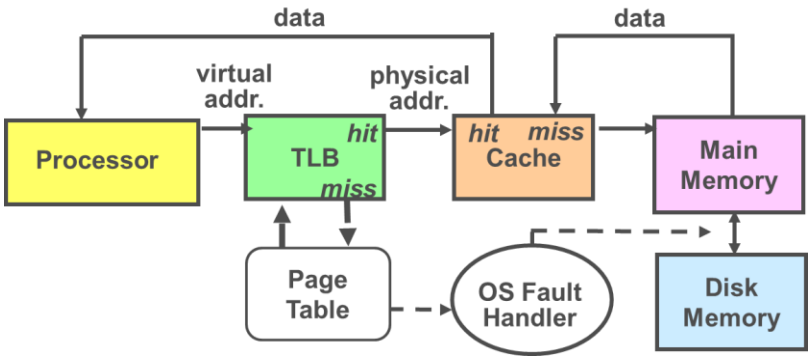
Final Project: Computer Architecture course

Language of simulation: VHDL or Verilog

Simulation environment: ISE (Xilinx) or Quartus (Intel) or Modelsim

Deadline: 12 Tir, 1401

CPU generates virtual address of size 16 bits. The address is a data address. The address is sent to TLB in order to translate it to physical address. TLB has 48 entries. The structure of TLB is explained below. If TLB could not translate the address, it is sent to the page table. The address of page table is hold in a register. The structure of page table is stated below. If page table indicates the address is in the main memory, the TLB should be updated and is the data is not in cache, the cache also is updated. If the data is not in the main memory, you should transfer one page of data from storage to the main memory, update the page table, TLB and the cache.



Role of processor in the project: processor is a black box that reads virtual addresses from a file. The virtual addresses are belong to an imaginary program.

Cache in the project: The cache has 32 entries. At any line of the cache, two words are hold.

Version #1: direct cache

Version #2: 2-way set associate cache

TLB: your TLB has 48 entries.

Version #1: fully associative

Version #2: 4-way set associative

Main memory: the RAM has 512 words.

Virtual address: 16 bits

Page size: 128B

The units you should design:

1) A black box for processor
2) Main memory
3) Two versions of cache
4) Two versions of TLB
5) Page table inside the RAM
6) A black box for hard disk.

Use random positions of RAM for PPN (physical page number) in the page table

All questions may rise during your implementation can be answered by me or by TAs.

Good luck!

Dr. Hakem Beitollahi,