In the name of God

HOMEWORK #3

(Arithmetic)

Computer Architecture

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Spring 1401

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Deadline:
1401/02/11

Notes:

1. Do the homework with your own information.
2. Any similarity between solutions reduces 1 point from overall point of your assignments.
3. No submissions will be accepted after the announced deadline.

1-Considering Division Hardware, calculate -52/24. Write down the related comparison, Quotient, divisor and reminder for each iteration.

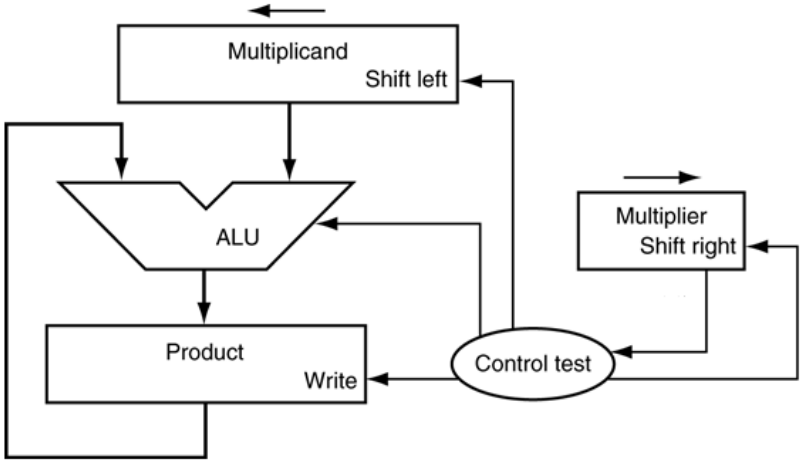
2-Calculate $2.3109375 \times 10^{1} + 6.391601562 \times 10^{-1}$ using Floating point addition algorithm.

3-show the IEEE-769 binary representation of the number -0.47_{ten} in single and double precision.

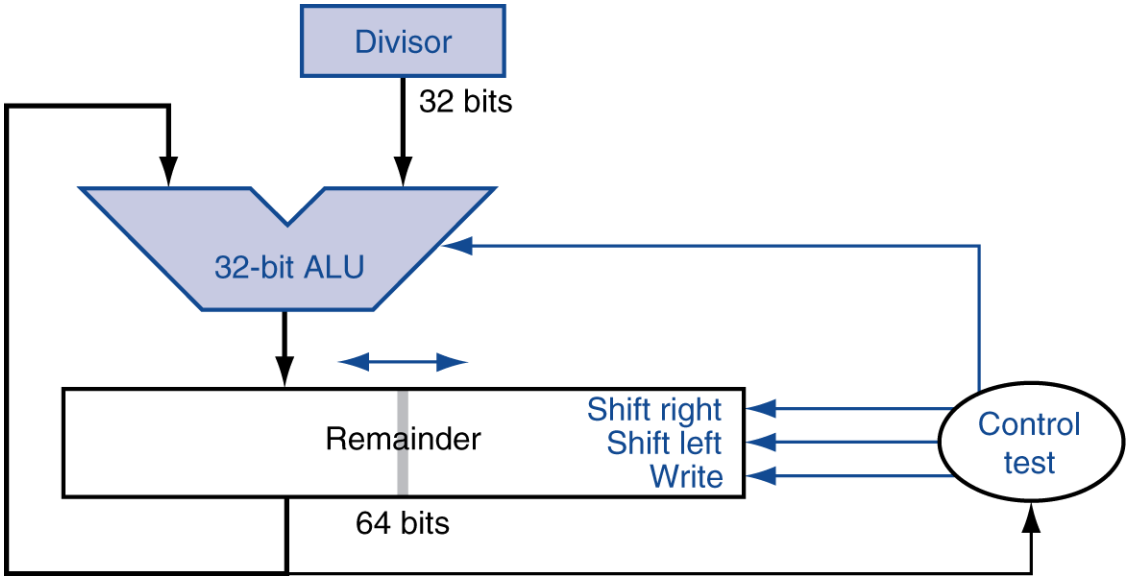
Implementation

1- Implement the following multiplier with VHDL, assuming that multiplicand and multiplier is respectively 8- and 6-bits **signed** integers.

Give an example and run the algorithm on the paper. Write all iterations to calculate the answer.



2- Implement the following optimized division circuit with VHDL.



3- Implement an ALU with multiplier and adder for the following floating-point representation.

Suppose you have a new standard representation for 16-bits floating-point that use 7 bits for exponent and 8-bits for the fraction part (1 bit is used for sign).

Good luck ☺