

In the name of God

HOMEWORK #4

Computer Architecture

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Spring 1400

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Deadline:
1400/3/11

Notes :

1. Do the homeworks with your own information.
2. Any similarity between solutions reduces **1** point from overall point of your assignments.
3. No submissions will be accepted after the announced deadline.

Written:

Q1. How many stalls does the following code need using dynamic prediction? Suppose, the last branch before the following code is taken.

A) 1-bit prediction system

B) 2-bits prediction system

```
i=0;
for( i =0; i<100; i++)
  for (j=i; j<100; j+=2)
  {
    i++;
  }
```

Q2. Design a pipeline implementation for the following new instruction. You should update the architecture of MIPS pipeline to support the following instruction. Your answer should include the updated datapath and also all control signals for this particular instruction.

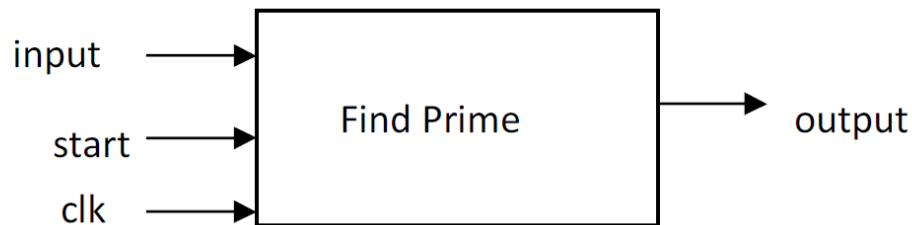
Swi Rd, Rs (Rt) // $\text{Mem}[\text{Rs} + \text{Mem}[\text{Rt}]] = \text{Rd}$

Implement

Q1. Implement a 4-bit-carry-ripple adder using full adders. Note that the adder should be a pipelined version of adder, each stage contains only one full adder

Hint: Use D-flip flop (DFF) to help implementing the pipeline.

Q2. Design a datapath and controller for the following circuit specification. The circuit receives a 10-bit number bigger than one and generates a prime number less than-or-equal to the input number. The circuit has a start signal such that when the start signal becomes one, the circuit starts finding the output.

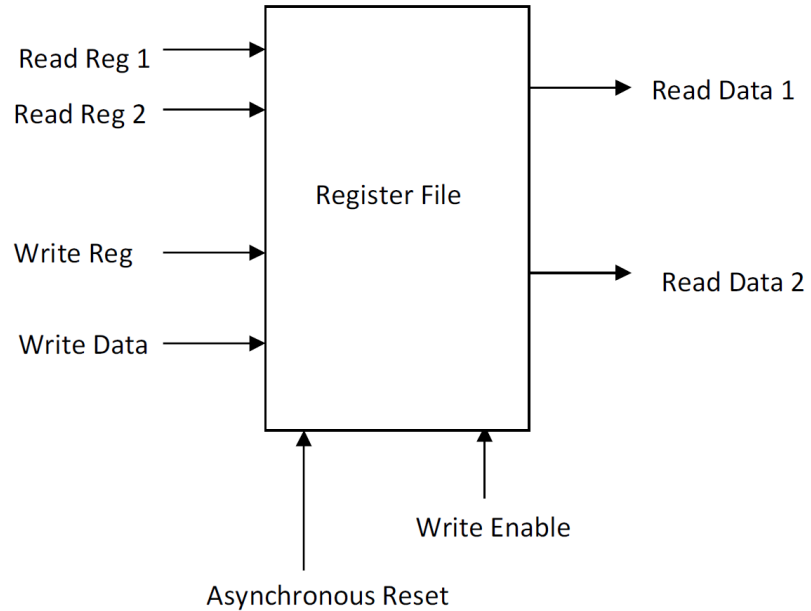


For example when the input is 17, the output becomes 17. When the input is 21, the output becomes 19.

You can search from algorithms that find the prime numbers less than particular number (you can find them in discrete mathematic books or in security books)

The circuit must have both datapath and controller.

Q3. Implement a register file with the following attributes



The Asynchronous reset, will reset all registers to zero value. The specification of the rest of signals have been provided in the slides (Lecture 6: Processor). Data width of the registers is 8 bits.