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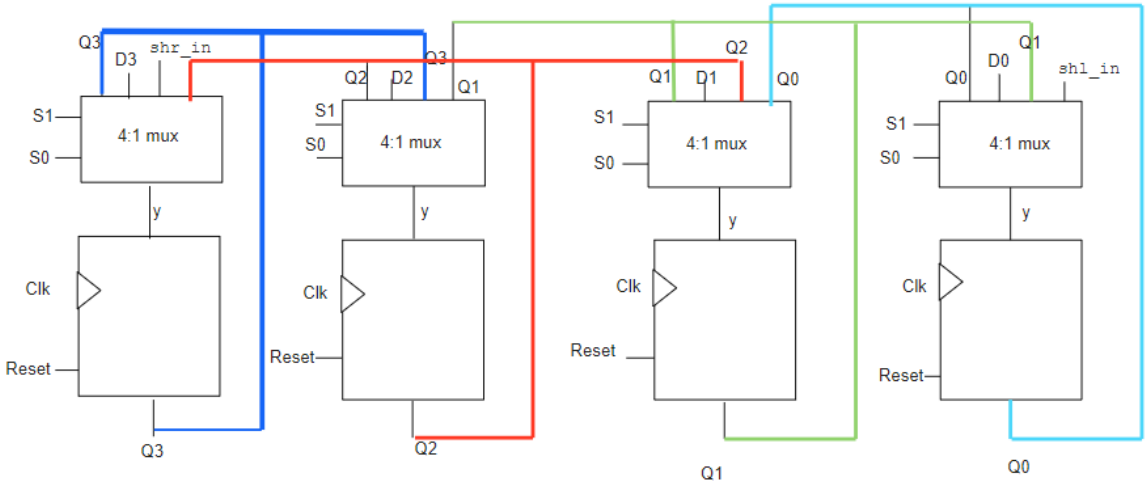
21902532 Lab4-preliminary

Cs223-06

```
module flip_flop(input logic clk,
                 input logic reset,
                 input logic [3:0] d,
                 output logic [3:0] q);
    // synchronous reset
    always_ff @(posedge clk)
    if (reset) q <= 4'b0;
    else q <= d;
endmodule
```



MULTIFUNCTION REGISTER BY USİNG FLIP FLOPS

Multifunction register

```
module mux2to1( input logic d0, d1, s,
                output logic y);
   logic w1, w2;
   assign w1 = d0 & !s;
   assign w2 = d1 & s;
   assign y = w1 || w2;
endmodule
//4to1 mux by using 2to1 mux
module mux4to1( input logic a, b, c, d, s0, s1,
                output logic y);
   logic w1 , w2;
   mux2to1 mux1( a, b, s0 , w1);
   mux2to1 mux2( c, d , s0, w2);
   mux2to1 mux3( w1, w2, s1, y );
endmodule
module multifunction_register( input logic clk,
                               input logic reset,
                               input logic  s1, s0, shr_in, shl_in, d3, d2, d1, d0,
                               output logic [3:0] q );
   logic [3:0] w;
   mux4to1 mux1( w[3], d3, shr_in, q[2], s1, s0, w[3]);
   mux4to1 mux2 (w[2], d2, q[3],q[1], s1, s0, w[2]);
   mux4to1 mux3 (w[1], d1, q[2], q[0], s1, s0, w[1]);
   mux4to1 mux4 (w[0], d0, q[1], shl_in, s1, s0, w[0] );
    flip_flop flop(clk, reset, w, q );
```

```
   endmodule //////////////////////

module multi_register_testbench();

    logic clk, reset;

    logic s1, s0, shr_in, shl_in, d3, d2, d1, d0;

    logic [3:0] q;

    multifunction_register dut( clk, reset, s1, s0, shr_in, shl_in, d3, d2, d1, d0, q );

   always

   begin

   clk = 1; #5; clk = 0; #5;

   end

   initial begin

       q[3]= 0; q[2]= 0; q[1] = 0; q[0] = 0;

       s1 = 0; s0= 0; shr_in = 0; shl_in = 0; d3 = 0; d2 = 0; d1 = 0; d0 = 0; #10

       //reset = 1; #10

       //reset = 0;

       s1 = 0; s0= 1;

       for (int i=0; i<16; i=i+1) begin

            {d3, d2, d1, d0} = i;

            #10

      end

       s1 = 1; s0 = 0; #10

       shr_in = 1; #10

       s1 = 1; s0 = 1; #10

       shl_in = 1;

   end

endmodule
```