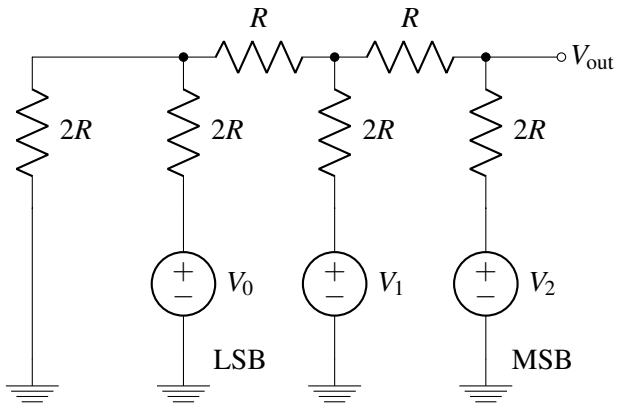
EECS 16B Designing Information Devices and Systems II
Fall 2018 Elad Alon and Miki Lustig **Homework 1**

This homework is due on Wednesday September 5, 2018, at 11:59PM.
Self-grades are due on Monday, September 10, 2018, at 11:59PM.

1. Digital-Analog Converter

A digital-analog converter (DAC) is a circuit for converting a digital representation of a number (binary) into a corresponding analog voltage. In this problem, we will consider a DAC made out of resistors only (resistive DAC) called the R-$2R$ ladder. Here is the circuit for a 3-bit resistive DAC.



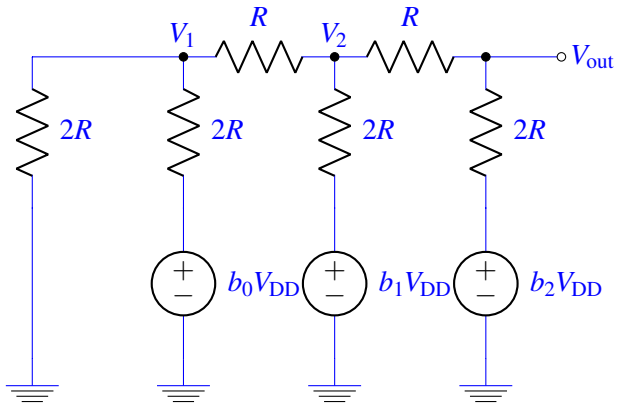
Let $b_0, b_1, b_2 = \{0, 1\}$ (that is, either 1 or 0), and let the voltage sources $V_0 = b_0 V_{DD}$, $V_1 = b_1 V_{DD}$, $V_2 = b_2 V_{DD}$, where V_{DD} is the supply voltage.

As you may have noticed, (b_2, b_1, b_0) represents a 3-bit binary (unsigned) number where each of b_i is a binary bit. We will now analyze how this converter functions.

(a) If $b_2, b_1, b_0 = 1, 0, 0$, what is V_{out}? Express your answer in terms of V_{DD}.

Solution:

There are several ways to solve this problem. For this solution set, we are going to solve for the generic solution rather than solve for each specific case of (a), (b), (c), and (d).



Applying KCL at nodes V_1, V_2, and V_{out}, we get

$$\frac{V_1}{2R} + \frac{V_1 - b_0 V_{\text{DD}}}{2R} + \frac{V_1 - V_2}{R} = 0$$
$$\frac{V_2 - b_1 V_{\text{DD}}}{2R} + \frac{V_2 - V_1}{R} + \frac{V_2 - V_{\text{out}}}{R} = 0$$
$$\frac{V_{\text{out}} - b_2 V_{\text{DD}}}{2R} + \frac{V_{\text{out}} - V_2}{R} = 0$$

Solving this system of equations leads to

$$\frac{b_2 V_{\text{DD}}}{2} + \frac{b_1 V_{\text{DD}}}{4} + \frac{b_0 V_{\text{DD}}}{8} = V_{\text{out}}$$

Plugging in 1, 0, 0 gives the answer.

$$V_{\text{out}} = \frac{V_{\text{DD}}}{2}$$

(b) If $b_2, b_1, b_0 = 0, 1, 0$, what is V_{out}? Express your answer in terms of V_{DD}.

Solution:

Plugging into the equation from part (a), we get

$$V_{\text{out}} = \frac{V_{\text{DD}}}{4}.$$

(c) If $b_2, b_1, b_0 = 0, 0, 1$, what is V_{out}? Express your answer in terms of V_{DD}.

Solution:

Plugging into the equation from part (a), we get

$$V_{\text{out}} = \frac{V_{\text{DD}}}{8}.$$

(d) If $b_2, b_1, b_0 = 1, 1, 1$, what is V_{out}? Express your answer in terms of V_{DD}.

Solution:

Plugging into the equation from part (a), we get

$$V_{\text{out}} = \frac{7V_{\text{DD}}}{8}.$$

(e) Finally, solve for V_{out} in terms of V_{DD} and the binary bits b_2, b_1, b_0.

Solution:

From part (a),

$$\frac{b_2 V_{\text{DD}}}{2} + \frac{b_1 V_{\text{DD}}}{4} + \frac{b_0 V_{\text{DD}}}{8} = V_{\text{out}}.$$

(f) Explain how your results above show that the resistive DAC converts the 3-bit binary number (b_2, b_1, b_0) to the output analog voltage V_{out}.

Solution:

Every increment of $\frac{1}{8}V_{\text{DD}}$ on V_{DD} represents an increment of 1 to the 3-bit binary number $(b_2 b_1 b_0)$.

For example, if $V_{\text{out}} = \frac{5}{8}V_{\text{DD}}$, the input was 5 in binary (1 0 1)$\rightarrow$ $(b_2 = 1\ b_1 = 0\ b_0 = 1)$.

2. Logical Comparator

In this problem, we are going to implement a two-bit comparator. We take in two numbers a, b, which are composed of bits a_1, a_0, b_1, b_0 respectively. For example, $a_1 = 1, a_0 = 0$ would mean $a = 10_2 = 2_{10}$.

(a) Let's first implement a one-bit comparator. Give a logical expression for the $>$ operator. To be more specific, create a logical function such that $f(a_0, b_0)$ will be true if $a_0 > b_0$ and false otherwise.

Solution:

The only way $f(a_0, b_0)$ can be true is if $a_0 = 1, b_0 = 0$. Thus, we can say $f(a_0, b_0) = a_0 \cdot \overline{b_0}$.

(b) Now, let's extend this function to implement a two-bit comparator. More specifically, make a function $g(a, b)$ such that $g(a, b)$ is true if $a > b$ and false otherwise. Recall that a, b can be decomposed to two digits each. You may optionally use $f(a_0, b_0)$ to implement $g(a, b)$.

Solution:

$a > b$ only if $a_1 > b_1$ or $a_1 = b_1$ and $a_0 > b_0$. This in itself is almost a complete logical function, except we need to express equality. Fortunately, the exclusive or function does the exact opposite, so we can simply negate it to get an equality function. Thus, $g(a, b) = (a_1 > b_1) + (\overline{a_1 \bigoplus b_1} \cdot (a_0 > b_0))$.

We can also use the truth table to find the expression:

a_1	a_0	b_1	b_0	$g(a,b)$
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

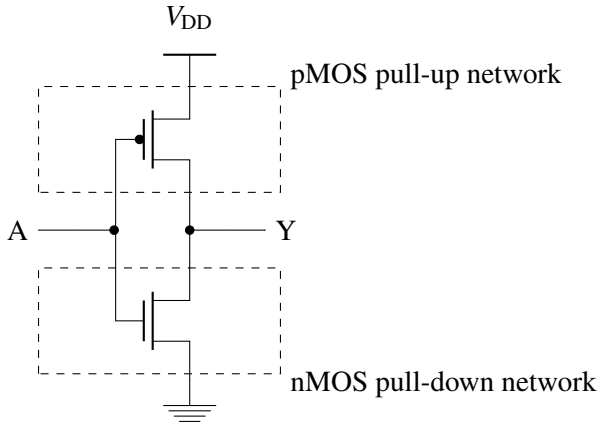
Now we can choose the rows which make $g(a, b)$ true, and string them together with OR's, hence

$$g(a,b) = \overline{a_1} \cdot a_0 \cdot \overline{b_1} \cdot \overline{b_0} + a_1 \cdot \overline{a_0} \cdot \overline{b_1} \cdot \overline{b_0} + a_1 \cdot \overline{a_0} \cdot \overline{b_1} \cdot b_0 + a_1 \cdot a_0 \cdot \overline{b_1} \cdot \overline{b_0} + a_1 \cdot a_0 \cdot \overline{b_1} \cdot b_0 + a_1 \cdot a_0 \cdot b_1 \cdot \overline{b_0}$$

3. Transistors and Boolean Logic

A boolean formula can be implemented in digital circuitry using nMOS and pMOS transistors. In circuits, the truth value 1 (*true*) is represented by a high voltage, called POWER (V_{DD}). The truth value 0 (*false*) is represented by a low voltage, called GROUND (GND). In this problem, we will only use the truth values in order to simplify notations. That is, if you see $A = 1$ for a point A, then it means the voltage of A is equal to V_{DD}. Similarly, if $A = 0$, then the voltage of A is equal to GND.

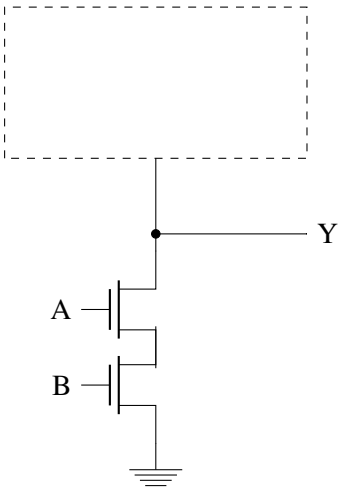
An inverter can be implemented with 1 nMOS and 1 pMOS, as shown in the figure below. When the input A is 0, then the nMOS is OFF and the pMOS is ON. Thus, the output Y is pulled up to 1 because it is connected to V_{DD}. Conversely, when A is 1, then the nMOS is ON and the pMOS is OFF, and Y is pulled down to 0. Therefore, the circuit implements the Boolean formula, $Y = \overline{A}$.



In general, a Boolean-formula circuit has an nMOS *pull-down network* to connect the output to 0 (GND) and a pMOS *pull-up network* to connect the output to 1 (V_{DD}). The pull-up and pull-down networks in the inverter example each consist of a single transistor.

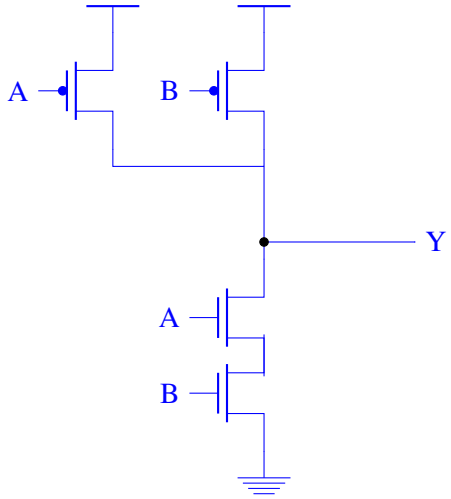
In this problem, you will design pull-up networks given the pull-down networks.

(a) The pull-down network of the Boolean formula (a 2-input NAND gate), $Y = \overline{(A \cdot B)}$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.

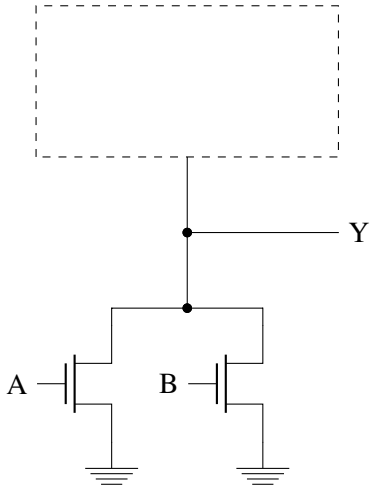


Solution:

From De Morgan's laws, we have $Y = \overline{A} + \overline{B}$, which means that when $A = 0$ or $B = 0$, Y should be pulled up to 1. Therefore, we connect two pMOS transistors in parallel in the pull-up network.

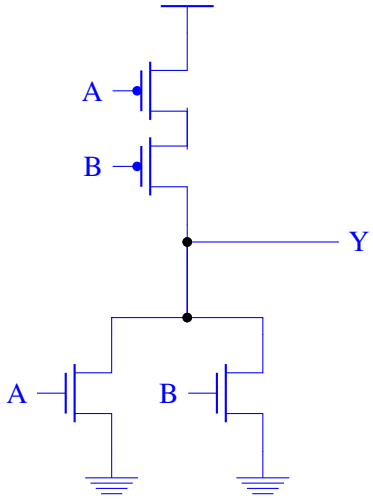


(b) The pull-down network of the Boolean formula (a 2-input NOR gate), $Y = \overline{(A+B)}$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.

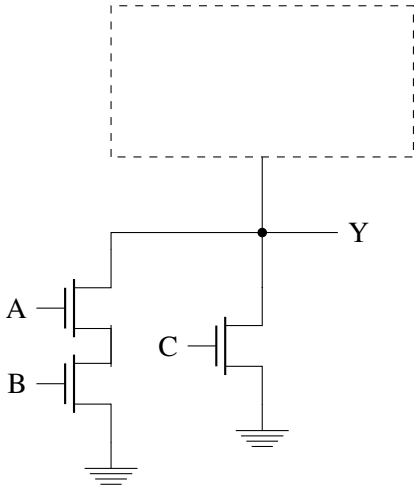


Solution:

From De Morgan's laws, we have $Y = \overline{A} \cdot \overline{B}$, which means that when $A = 0$ and $B = 0$, Y should be pulled up to 1. Therefore, we connect two pMOS transistors in series in the pull-up network.

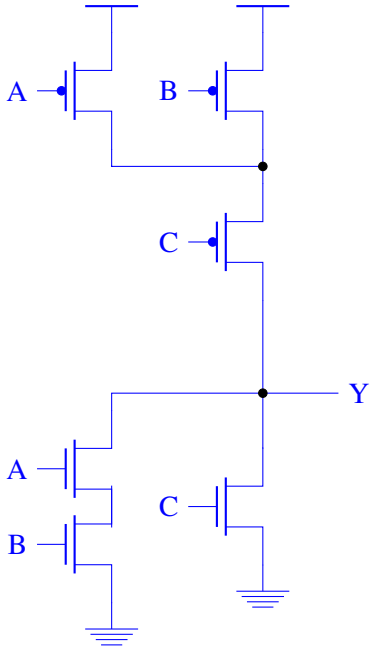


(c) The pull-down network of the Boolean formula, $Y = \overline{\left((A \cdot B) + C\right)}$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.

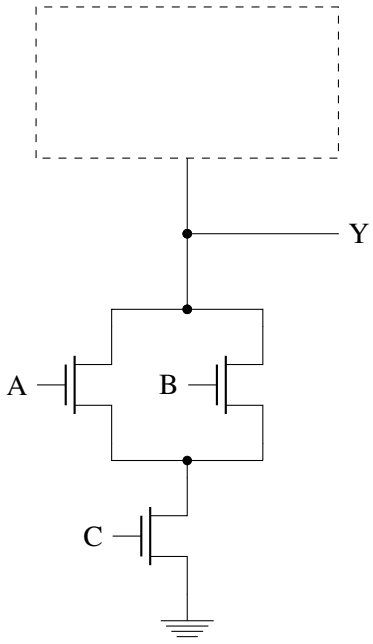


Solution:

Let Z be $Z = \overline{A} + \overline{B}$. From De Morgan's laws, we have $Y = \left(\overline{A} + \overline{B}\right) \cdot \overline{C} = Z \cdot \overline{C}$, which means that when $Z = 1$ and $C = 0$, Y should be pulled up to 1. For Z, we connect 2 pMOS transistors in parallel as in part (a). Then, we connect the two pMOS transistors of Z and the one pMOS transistor of C in series in the pull-up network.

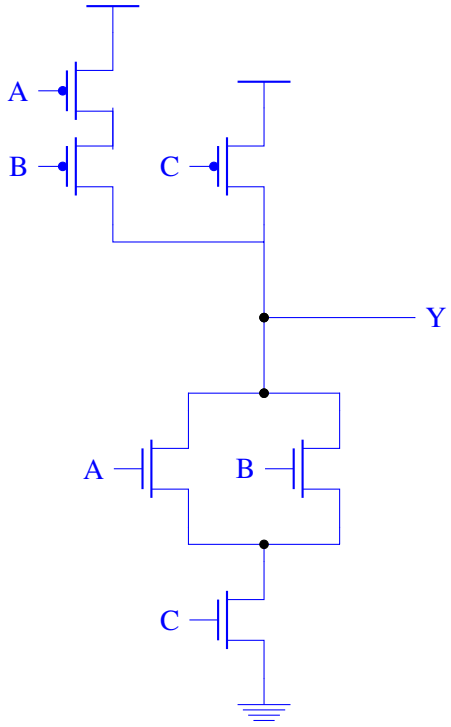


(d) The pull-down network of the Boolean formula, $Y = \overline{\left((A+B)\cdot C\right)}$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.

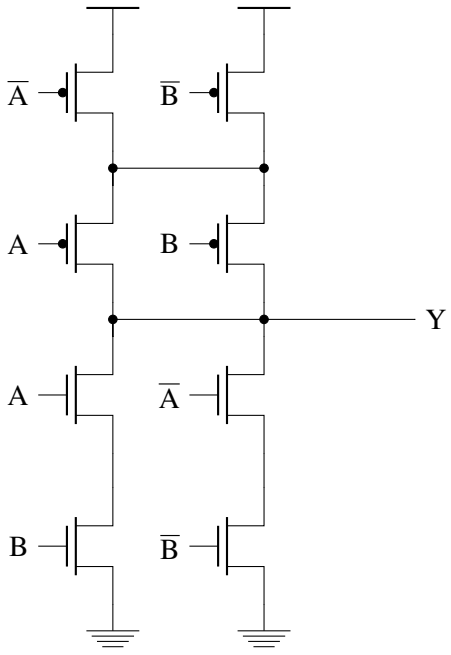


Solution:

Let Z be $Z = \overline{A}\cdot\overline{B}$. From De Morgan's laws, we have $Y = \left(\overline{A}\cdot\overline{B}\right) + \overline{C} = Z + \overline{C}$, which means that when $Z = 1$ or $C = 0$, Y should be pulled up to 1. For Z, we connect 2 pMOS transistors in series as in part (b). Then, we connect the two pMOS transistors of Z and the one pMOS transistor of C in parallel in the pull-up network.



(e) For the circuit below, write the truth table for inputs A and B with output Y. What boolean operation is this?
Note some of the gate voltages are $\overline{A}$ and $\overline{B}$.

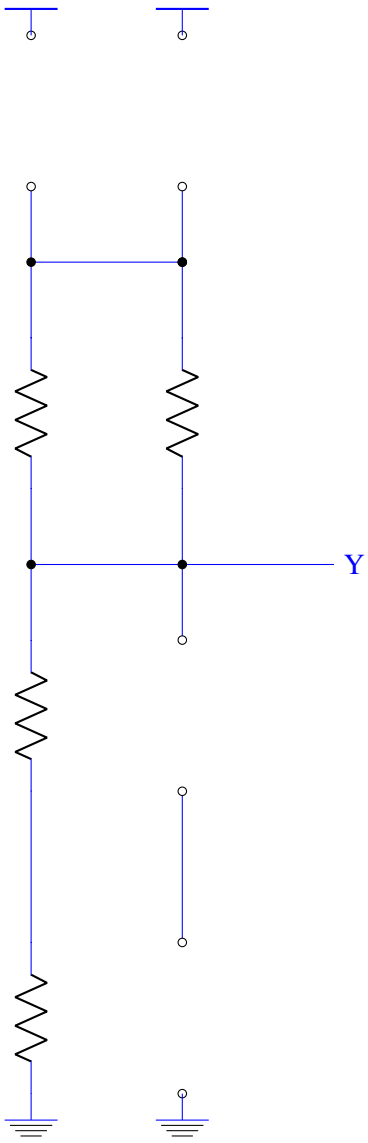


Solution:

In CMOS, if the gate of an nMOS is 1, the switch is closed and acts as a resistor. If the gate voltage is 0, then it acts as an open. The opposite is true for pMOS.

To get the truth table, draw the circuit for each input case and see whether the output is connected to ground or V_{DD}

This is what the circuit should look like for $A = 0, B = 0$:



Y is connected to ground through resistors, so for the input combination $A = 0, B = 0$, $Y = 0$. Repeat this for the 3 other cases and you will get the following truth table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

This circuit is an XOR gate ($A \oplus B$).

Mechanical:

4. First-Order Differential Equation Practice

(a) Solve the equation $3\frac{d}{dt}f(t)+6f(t)=0$ given that $f(0)=7$

Solution:

We know that the solution to the first-order differential equation must be of the form $f(t)=Ae^{\lambda t}+B$. If we plug in that definition of $f(t)$ into the given equation, we get

$$\begin{aligned}3(A\lambda e^{\lambda t})+6(Ae^{\lambda t}+B)&=0\\(3A\lambda+6A)e^{\lambda t}+6B&=0\end{aligned}$$

We know that the coefficient of the exponential $e^{\lambda t}$ and the constant must be zero, which means that $3A\lambda+6A=0$ and $6B=0$. Solving these yield $\lambda=-2, B=0$. If we use our initial condition alongside the parameters we just found, we get $7=f(0)=Ae^{-2(0)}+0=A$, implying that $A=7$. Therefore, $f(t)=7e^{-2t}$.

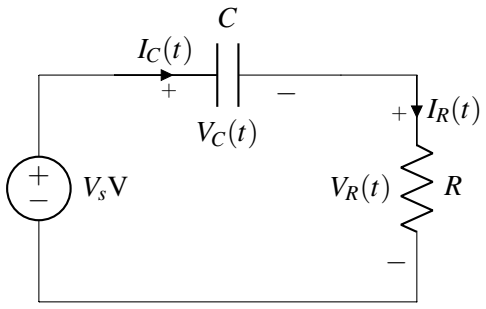
(b) Solve the equation $3f(t)-6f'(t)=4$ given that $f(2)=\frac{1}{3}$

Solution:

$f(t)=Ae^{\lambda t}+B$

$$\begin{aligned}3(Ae^{\lambda t}+B)-6(A\lambda e^{\lambda t})&=4\\(3A-6A\lambda)e^{\lambda t}+3B&=4\\\lambda&=\frac{1}{2}\\B&=\frac{4}{3}\\f(t)&=Ae^{\frac{1}{2}t}+\frac{4}{3}\\f(2)=\frac{1}{3}&=Ae^{\frac{1}{2}(2)}+\frac{4}{3}\\A&=-\frac{1}{e}\\f(t)&=-\frac{1}{e}e^{\frac{1}{2}t}+\frac{4}{3}\\&=-e^{\frac{1}{2}t-1}+\frac{4}{3}\end{aligned}$$

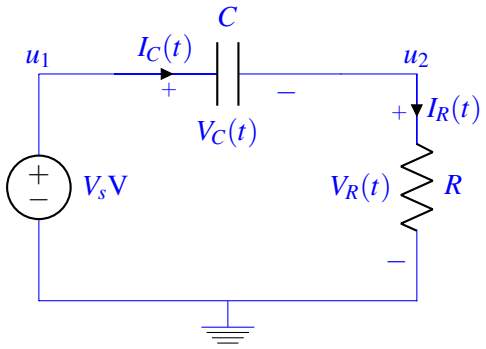
5. RC Circuit



(a) Find a differential equation for $V_c(t)$ for $t \geq 0$. Solve the differential equation using the initial condition $V_c(0) = 1\text{V}$. Use component values of $C = 1\text{fF}$ ($1\text{fF} = 10^{-15}\text{F}$), $R = 10\text{k}\Omega$, and $V_s = 2\text{V}$

Solution:

First, we set one node to ground and label the other two nodes as u_1 and u_2.



$$\begin{aligned} V_c(t) &= u_1 - u_2 \\ u_1 &= V_s \\ u_2 &= V_R(t) \\ V_c(t) &= V_s - V_R(t) \end{aligned} \tag{1}$$

Using Ohm's law:

$$V_R(t) = RI_R(t)$$

Using KCL at u_2

$$\begin{aligned} I_R(t) &= I_C(t) \\ V_R(t) &= RI_C(t) \end{aligned}$$

The current through a capacitor is:

$$\begin{aligned} I_C(t) &= C\frac{dV_C(t)}{dt} \\ V_R(t) &= RC\frac{dV_C(t)}{dt} \end{aligned}$$

Plugging back into (1):

$$V_c(t) = V_s - RC\frac{dV_C(t)}{dt}$$

Rearranging, we get our differential equation:

$$\frac{dV_C(t)}{dt} + \frac{V_C(t)}{RC} = \frac{V_s}{RC}$$

We can convert this to a homogeneous differential equation by using a change of variables:

$$x = V_C(t) - V_s$$

$$V_C(t) = x + V_s$$

$$\frac{dV_C(t)}{dt} = \frac{dx}{dt}$$

substituting $V_C(t)$ in our differential equation, we get:

$$\frac{dx}{dt} + \frac{x + V_s}{RC} = \frac{V_s}{RC}$$

$$\frac{dx}{dt} + \frac{x}{RC} = 0$$

$$\frac{dx}{dt} = -\frac{1}{RC}x$$

The general solution to the differential equation $\frac{dx}{dt} = \lambda x$ is:

$$x = Ae^{\lambda t}$$

Where A is a constant determined by initial conditions. In this case, $\lambda = -\frac{1}{RC}$, giving us the solution:

$$x = Ae^{-\frac{t}{RC}}$$

Next, we substitute $V_C(t)$ back into the equation:

$$V_C(t) - V_s = Ae^{-\frac{t}{RC}}$$

$$V_C(t) = Ae^{-\frac{t}{RC}} + V_s$$

Plugging in values for R, C, and V_s gives us:

$$V_C(t) = Ae^{-\frac{t}{10^{-11}}} + 2$$

The final step is to determine A by plugging in the initial condition.

$$V_C(0) = 1 = A + 2$$

$$A = -1$$

The overall answer is then:

$$V_C(t) = 2 - e^{-\frac{t}{10^{-11}}} \text{ [V]}$$

(b) Instead of having an initial condition of $V_c(0) = 1$V, we now have an initial condition of $I_R(0) = 150\mu$A ($1\mu\text{A} = 10^{-6}$A). Find the new expression for $V_C(t)$ for $t \geq 0$. Use the same component values listed in part (a)

Solution:

We can use the same general solution as in part (a), but we need to plug in our new initial condition to solve for A. To do that, we need to determine what $V_C(0)$ is using our current's initial condition.

Using Ohm's law:

$$V_R(0) = I_R(0) * R = 150 * 10^{-6} * 10^4 = 1.5 \text{ V}$$

We know that:

$$V_C(0) = V_s - V_R(0) = 2 - 1.5 = 0.5 \text{ V}$$

Now we can plug it back into the general solution:

$$0.5 = A + 2$$

$$A = -1.5$$

This gives us the answer:

$$V_C(t) = 2 - 1.5e^{-\frac{t}{10^{-11}}} \text{ [V]}$$

6. Write Your Own Question And Provide a Thorough Solution.

Writing your own problems is a very important way to really learn material. The famous "Bloom's Taxonomy" that lists the levels of learning is: Remember, Understand, Apply, Analyze, Evaluate, and Create. Using what you know to create is the top level. We rarely ask you any homework questions about the lowest level of straight-up remembering, expecting you to be able to do that yourself (e.g. making flashcards). But we don't want the same to be true about the highest level. As a practical matter, having some practice at trying to create problems helps you study for exams much better than simply counting on solving existing practice problems. This is because thinking about how to create an interesting problem forces you to really look at the material from the perspective of those who are going to create the exams. Besides, this is fun. If you want to make a boring problem, go ahead. That is your prerogative. But it is more fun to really engage with the material, discover something interesting, and then come up with a problem that walks others down a journey that lets them share your discovery. You don't have to achieve this every week. But unless you try every week, it probably won't ever happen.

Contributors:

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