EECS 16B Designing Information Devices and Systems II
Fall 2018 Elad Alon and Miki Lustig **Homework 2**

This homework is due on Wednesday, September 12, 2018, at 11:59 PM.
Self-grades are due on Monday, September 17, 2018, at 11:59 PM.

1. Complex Numbers (Mechanical)

A common way to visualize complex numbers is to use the complex plane. Recall that a complex number z is often represented in Cartesian form.

$$z = x + jy \text{ with } \text{Re}\{z\} = x \text{ and } \text{Im}\{z\} = y$$

See the Figure 1 for how z looks like in the complex plane.

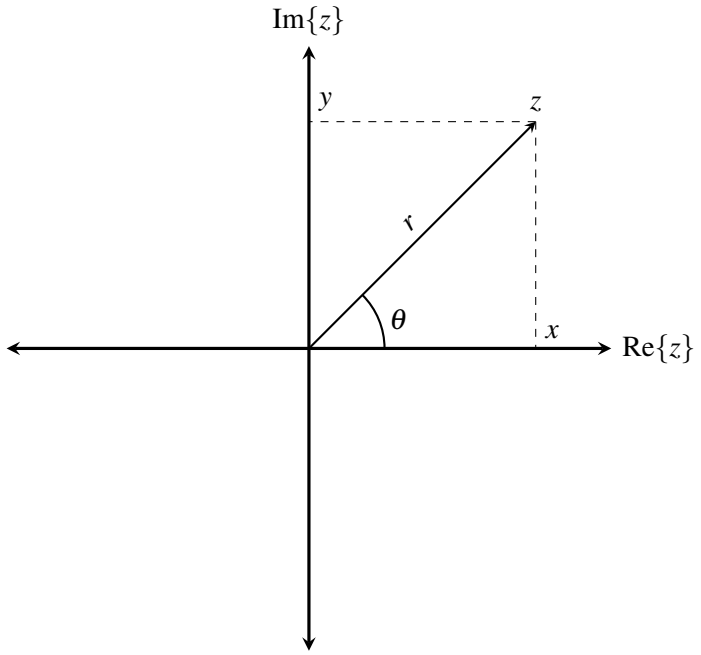


Figure 1: Complex Plane

In this question, we will derive the polar form of a complex number and use this form to make some interesting conclusions.

(a) Calculate the length of z in terms of x and y as shown in Figure 1. This is the magnitude of a complex number and is denoted $|z|$ or r. *Hint.* Use the Pythagoras theorem.

(b) Represent the real and imaginary parts of z in terms of r and θ.

(c) Euler's formula relates an imaginary exponential function to a combination of sines and cosines:

$$e^{j\theta} = \cos(\theta) + j\sin(\theta)$$

In future lectures, we'll see the importance of this relationship and why it's useful.
Use Euler's formula and your answer to part (b) to show that:

$$z = re^{j\theta}$$

(d) If $z = re^{j\theta}$, prove that $z^* = re^{-j\theta}$. Recall that the complex conjugate of a complex number $z = x + jy$ is $z^* = x - jy$.

(e) If we have a complex number

$$z = x + jy = re^{j\theta}$$

then we define the complex conjugate of z as

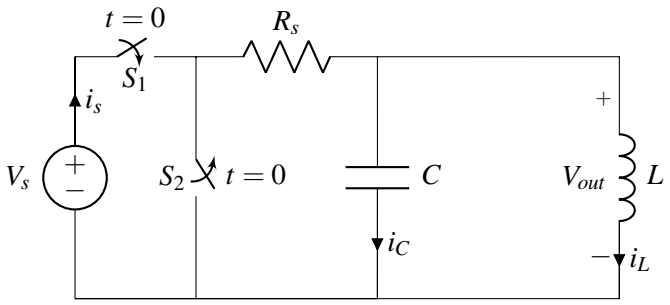
$$z^* = x - jy = re^{-j\theta}$$

Show that

$$r^2 = zz^*$$

2. RLC Circuit (Mechanical)

Consider the circuit shown below. For $t \leq 0$, switch S_1 is off (disconnected) while switch S_2 is on (connected). At $t = 0$, S_1 turns on while S_2 turns off.



(a) Immediately before the switches flip states at $t = 0$, find the initial conditions for the inductor and capacitor: $i_L(0)$ and $V_c(0)$. Assume the circuit has reached DC steady state (voltages and currents are constant) before the switches flip states.

(b) Define your state variables as $V_{out}(t)$ and $i_L(t)$, and use nodal analysis to derive the homogenous vector differential equation ($\frac{d\vec{x}}{dt} = A\vec{x} + b$) that captures the behaviour of the ciruit at $t \geqq 0$ (after the switch flips).

(c) Solve the vector differential equation to find $V_{out}(t)$. Use $V_s = 6\text{V}$, $R = 1\text{k}\Omega$, $C = 1\text{fF}$, and $L = 6.25\text{nH}$.

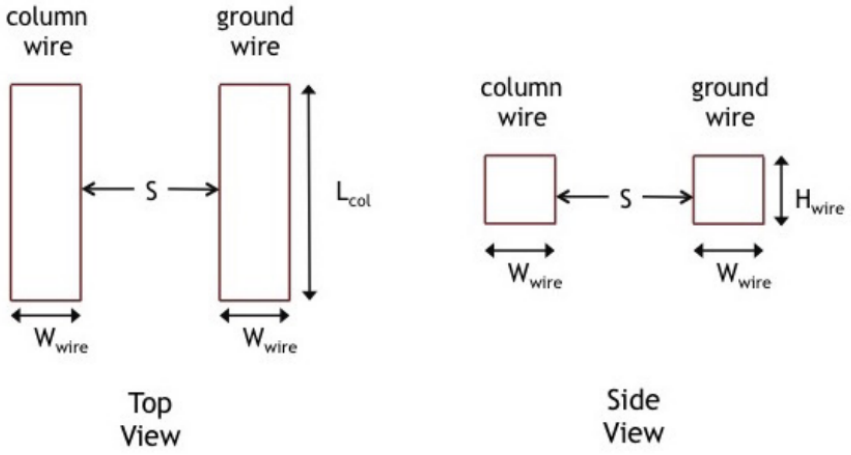
3. DRAM: How Big Can We Make Them?

Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store $>$ 8 billion bits and is sold for $\approx$ \$3-\$5.

At the most basic level, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a "1" or a "0" is stored in that location. In order to pack as many bits together as possible on to a single chip, rather than running a massive number of wires to access every single bit of the DRAM individually, the bits are arranged into a set of columns, where each column uses a single wire to access information from one of the bits. By turning ON the access switch within the particular bit cell via the single column wire, the corresponding bit is accessed (while leaving all of the switches in the rest of the cells off).

In this problem we'll take a look at how long we can make the DRAM columns and still get the device to work at a reasonable speed. For the purpose of this problem we'll mostly ignore details of how the DRAM actually works (and that making the column too long might actually stop the device from functioning at all) and just focus on the delay introduced by the column wire due to its resistance and its capacitance.

The column wire and its adjacent ground wire are arranged as follows.

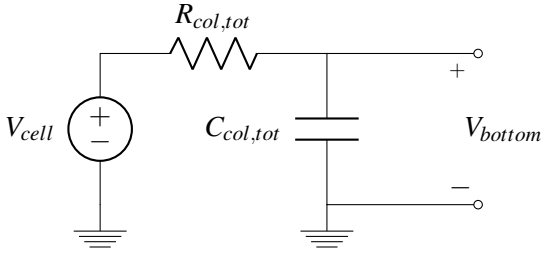


Each DRAM cell that gets added adds a length of 0.5μm (i.e., $0.5 \cdot 10^{-6}$ m) to the column and ground wires, the spacing between the column and ground wires is $S = 0.1\mu$m, and the wires have dimensions $H_{wire} = W_{wire} = 0.5\mu$m. Note that you can assume that the two wires are separated by air; in a real chip they would be separated by silicon dioxide, but we'll ignore that for this exercise. You should also assume that all of the capacitance is purely parallel plate. Furthermore, you can assume that the wire is made out of copper, with a resistivity $\rho = 1.68 \times 10^{-8}\Omega$·m.

(a) As a function of the number of cells on the column N_{cells}, what is the total capacitance of the column wire?

(b) As a function of the number of cells on the column N_{cells}, what is the total resistance of the column wire?

(c) Assuming that we can model the column wire and the top DRAM cell as below (note that this is not a truly accurate model, but it gives the right form for the answer), what will be the delay between information from the top of the DRAM column arriving to the bottom of the DRAM column (i.e., the delay between V_{cell} and V_{bottom}) as a function of N_{cells}? We define the delay to be the length of time it takes for the output value to reach $1/2$ of it's final value. Note that $V_{bottom}(0) = 0V$



(d) Given your answer to part (c), how many cells could you put on a single column (i.e., solve for N_{cells}) such that DRAM can operate at $400MHz$ (i.e. a $2.5ns$ clock period).

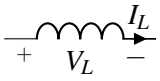
(e) For the sake of comparison, how long would it take for light to travel from the top of the column to the bottom of the column for the dimension of column wire associated with your answer to part (d)? Note that the speed of light is $c = 3 \times 10^8 \frac{m}{s}$

4. Speakers revisited

In EE16A you were given several homework problems where we had to build circuits to drive a speaker, and you were told to model the speaker as being an 8Ω resistor. In this problem we will develop a somewhat more accurate model for the speaker and use this model to understand a few interesting characteristics and limitations of these devices.

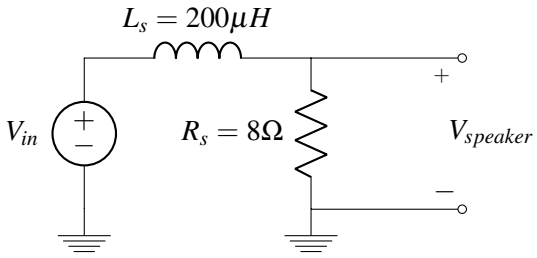
As we will learn about in more detail later on in this class, it turns out that besides just a resistance, speakers usually have another "parasitic" (i.e., potentially undesired) circuit element associated with them - this element is known as an inductor. The symbol for an inductor is shown below; the physics behind this relationship will be covered later, but for now all you need to know is that the inductor enforces the following relationship between its voltage and its current:

$$V_L = L \times \frac{dI_L}{dt}$$



where L is the "inductance" (which has units of Henries, with typical values in the range of pH to mH).

For the rest of the problem we will assume that the speaker is driven by an ideal voltage source, and that we can now model the speaker as follows:



Note that the audio coming out of the speaker is directly set by $V_{speaker}$ - i.e., in the model above, the voltage across the resistor is what we care about in terms of what we hear.

(a) If V_{in} is statically set to 1V (i.e., V_{in} is and always has been 1V), what will $V_{speaker}$ be?

(b) Now let's start examining what may happen when V_{in} changes. Write the differential equation relating $V_{speaker}$ to V_{in}, R_s, and L_s.

(c) If V_{in} starts at 1V and then instantaneously transitions to 0V, solve the differential equation from part (b) and sketch the resulting waveform $V_{speaker}(t)$.

(d) Given your solution to (c), how long will it take for $V_{speaker}$ to reach 0.25V?

5. CMOS Scaling

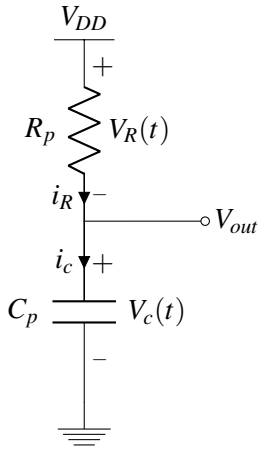
Jerry wants to create a new machine learning accelerator chip utilizing CMOS technology. When designing his chip, he considers the most important parameters of his design to be the amount of energy dissipated when the gate transisions, and the delay time it takes for the output of a gate to hit $\frac{V_{DD}}{2}$ from either ground or V_{DD} (i.e. the delay of the gate).

Jerry has access to two different fabrication processes: process A and process B.

Process A uses a supply voltage of $V_{DD} = 1$V. The transistors have a parasitic resistance of $R_p = 10\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 5$fF.

Process B uses a supply voltage of $V_{DD} = 3$V. The transistors have a parasitic resistance of $R_p = 30\text{k}\Omega$, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 1$fF.

In order to determine which process is better for the design, Jerry decides to analyze the circuit where the input of an inverter transitions from V_{DD} to 0. This can be modeled as the following circuit:



Since the input of the inverter is transitioning from V_{DD} to 0, the initial condition for $V_c(t)$ is:

$$V_c(0) = 0$$

(a) Using the values of V_{DD}, R_p, and C_p from process A, calculate the total energy delivered by the voltage source, V_{DD}, while the capacitor is being charged to V_{DD}. Also calculate the time it takes for V_{out} to reach $\frac{V_{DD}}{2}$.

(b) Repeat part (a), but with the values from process B.

(c) Compare the energy and delay of process A and B

(d) Jerry's friend Pat tells Jerry that with process B, one can reduce V_{DD} to 2V. However, the reduction in supply voltage increases the parasitic resistance R_p to 50kΩ. Calculate the new delay and energy.

(e) Based on your previous answers, which process should Jerry choose to use?

6. Write Your Own Question And Provide a Thorough Solution.

Writing your own problems is a very important way to really learn material. The famous "Bloom's Taxonomy" that lists the levels of learning is: Remember, Understand, Apply, Analyze, Evaluate, and Create. Using what you know to create is the top level. We rarely ask you any homework questions about the lowest level of straight-up remembering, expecting you to be able to do that yourself (e.g. making flashcards). But we don't want the same to be true about the highest level. As a practical matter, having some practice at trying to create problems helps you study for exams much better than simply counting on solving existing practice problems. This is because thinking about how to create an interesting problem forces you to really look at the material from the perspective of those who are going to create the exams. Besides, this is fun. If you want to make a boring problem, go ahead. That is your prerogative. But it is more fun to really engage with the material, discover something interesting, and then come up with a problem that walks others down a journey that lets them share your discovery. You don't have to achieve this every week. But unless you try every week, it probably won't ever happen.

Contributors:

- Siddharth Iyer.
- Kyle Tanghe.