EECS 16B Designing Information Devices and Systems II
Fall 2018 Elad Alon and Miki Lustig **Homework 2**

This homework is due on Wednesday, September 12, 2018, at 11:59 PM.
Self-grades are due on Monday, September 17, 2018, at 11:59 PM.

1. Complex Numbers (Mechanical)

A common way to visualize complex numbers is to use the complex plane. Recall that a complex number z is often represented in Cartesian form.

$$z = x + jy \text{ with } \text{Re}\{z\} = x \text{ and } \text{Im}\{z\} = y$$

See the Figure 1 for how z looks like in the complex plane.

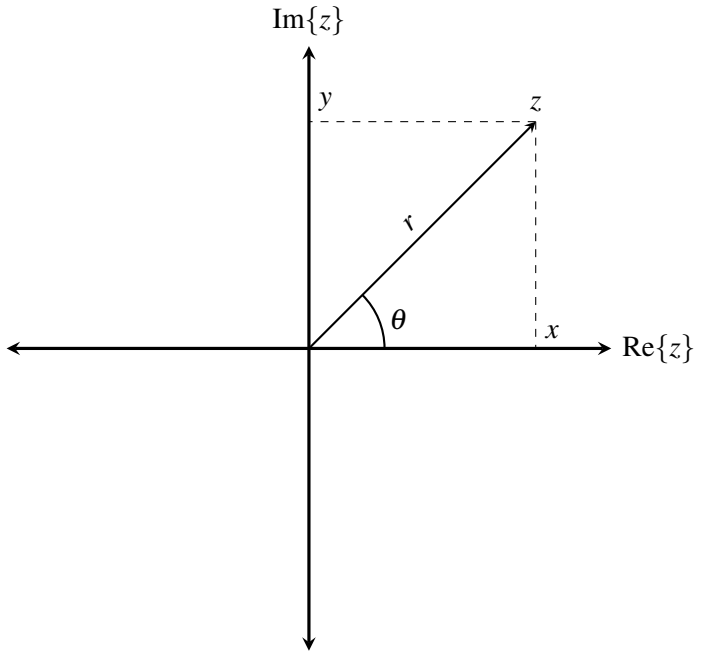


Figure 1: Complex Plane

In this question, we will derive the polar form of a complex number and use this form to make some interesting conclusions.

(a) Calculate the length of z in terms of x and y as shown in Figure 1. This is the magnitude of a complex number and is denoted $|z|$ or r. *Hint.* Use the Pythagoras theorem.

Solution:

$$r = \sqrt{x^2 + y^2} = |z|$$

(b) Represent the real and imaginary parts of z in terms of r and θ.

Solution:

$$x = r\cos(\theta) \text{ and } y = r\sin(\theta)$$

(c) Euler's formula relates an imaginary exponential function to a combination of sines and cosines:

$$e^{j\theta} = \cos(\theta) + j\sin(\theta)$$

In future lectures, we'll see the importance of this relationship and why it's useful.
Use Euler's formula and your answer to part (b) to show that:

$$z = re^{j\theta}$$

Solution:

$$\begin{aligned} z &= r\cos(\theta) + jr\sin(\theta) \\ &= r(\cos(\theta) + j\sin(\theta)) \\ &= re^{j\theta} \end{aligned}$$

(d) If $z = re^{j\theta}$, prove that $z^* = re^{-j\theta}$. Recall that the complex conjugate of a complex number $z = x + jy$ is $z^* = x - jy$.

Solution:

$$\begin{aligned} z^* &= (r(\cos(\theta) + j\sin(\theta)))^* \\ &= r(\cos(\theta) - j\sin(\theta)) \\ &= r(\cos(-\theta) + j\sin(-\theta)) \\ &= re^{-j\theta} \end{aligned}$$

(e) If we have a complex number

$$z = x + jy = re^{j\theta}$$

then we define the complex conjugate of z as

$$z^* = x - jy = re^{-j\theta}$$

Show that

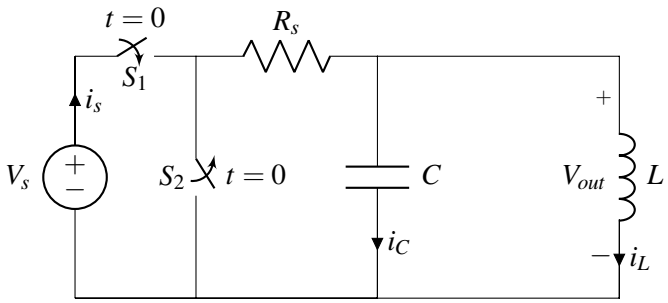
$$r^2 = zz^*$$

Solution:

$$zz^* = re^{j\theta}re^{-j\theta} = r^2e^{j\theta - j\theta} = r^2e^0 = r^2$$

2. RLC Circuit (Mechanical)

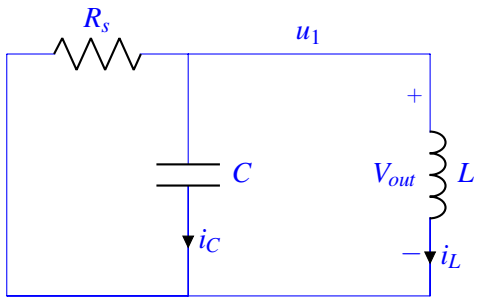
Consider the circuit shown below. For $t \leq 0$, switch S_1 is off (disconnected) while switch S_2 is on (connected). At $t = 0$, S_1 turns on while S_2 turns off.



(a) Immediately before the switches flip states at $t = 0$, find the initial conditions for the inductor and capacitor: $i_L(0)$ and $V_c(0)$. Assume the circuit has reached DC steady state (voltages and currents are constant) before the switches flip states.

Solution:

Before the switches flip states, the circuit looks like:



Since the capacitor and inductor are in parallel,

$$V_c(t) = V_L(t)$$

We know that for an inductor,

$$V_L(t) = L\frac{di_L(t)}{dt}$$

Because the circuit is in steady state, all the currents and voltages are constant, which means

$$\frac{di_L(0)}{dt} = 0$$

Thus:

$$V_c(0) = V_L(0) = 0$$

To find $i_L(0)$, we apply KCL at u_1:

$$\frac{u_1(0)}{R_s} + C\frac{dV_c(0)}{dt} + i_L(0) = 0$$

$$u_1(0) = V_c(0) = 0$$

Since the circuit is in steady state, all voltage and current derivatives are 0, so

$$0\frac{dV_c(0)}{dt} = 0$$

Plugging these back into our KCL equation, we get

$$0 + 0 + i_L(0) = 0$$

$$i_L(0) = 0$$

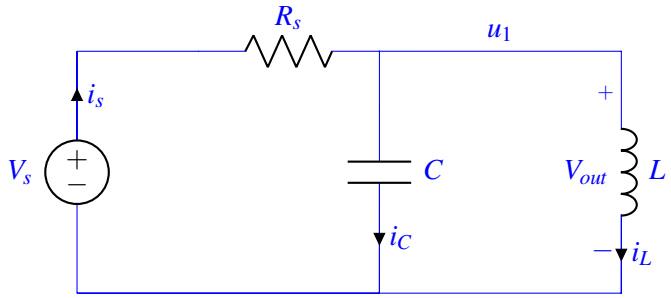
This gives us the initial conditions:

$$V_c(0) = 0$$

$$i_L(0) = 0$$

(b) Define your state variables as $V_{out}(t)$ and $i_L(t)$, and use nodal analysis to derive the homogenous vector differential equation ($\frac{d\vec{x}}{dt} = A\vec{x} + b$) that captures the behaviour of the ciruit at $t \geqq 0$ (after the switch flips).

Solution: After the switches flip states, the circuit looks like:



Doing KCL at u_1:

$$i_s = i_C + i_L$$

Using $i_C = C\frac{dV_{out}}{dt}$ and Ohm's law:

$$\frac{V_s - V_{out}}{R_s} = C\frac{dV_{out}}{dt} + i_L$$

$$\frac{dV_{out}}{dt} = \frac{V_s}{R_sC} - \frac{V_{out}}{R_sC} - \frac{i_L}{C}$$

We also know that $V_{out} = L\frac{di_L}{dt}$. These two equations give us a nonhomogeneous differential equation. We can actually turn i_L into an auxilary variable using $i_L = i' + \frac{V_s}{R}$, which turns the first equation into

$$-\frac{V_{out}}{R_sC} - \frac{i'}{C} = \frac{dV_{out}}{dt}$$

We can then turn this into a vector differential equation

$$\begin{bmatrix} \frac{dV_{out}}{dt} \\ \frac{di'}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_sC} & -\frac{1}{C} \\ \frac{1}{L} & 0 \end{bmatrix} \begin{bmatrix} V_{out} \\ i' \end{bmatrix}$$

(c) Solve the vector differential equation to find $V_{out}(t)$. Use $V_s = 6\text{V}$, $R_s = 1\text{k}\Omega$, $C = 1\text{fF}$, and $L = 6.25\text{nH}$.

Solution: Plugging in values for V_s, R, C, L give us the vector differential equation

$$\begin{bmatrix} \frac{dV_{out}}{dt} \\ \frac{di'}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{10^3 * 10^{-15}} & -\frac{1}{10^{-15}} \\ \frac{1}{6.25 * 10^{-12}} & 0 \end{bmatrix} \begin{bmatrix} V_{out} \\ i' \end{bmatrix}$$

We can find the eigenvalues of the **A** matrix.

$$\det\left(\begin{bmatrix} -10^{12} & -10^{15} \\ 1.6 * 10^8 & 0 \end{bmatrix}\right) = 0 = \lambda^2 + 10^1 2\lambda + 1.6 * 10^2 3$$

$$\lambda = -2 * 10^{11}, -8 * 10^{11}$$

We have 2 distinct λ values, so the general form of the solution is:

$$V_{out}(t) = c_1 e^{\lambda_1 t} + c_2 e^{\lambda_2 t}$$

In order to solve for c_1 and c_2, we need initial conditions for $V_{out}(0)$ and $\frac{dV_{out}(0)}{dt}$. In part (a), we saw:

$$V_{out}(0) = 0$$

before the switches flipped states. We also know that it must be the initial condition immediately after the switches flip states because of the relationship:

$$i_c(t) = C\frac{dV_c(t)}{dt}$$

if V_{out} changed instantaneously at $t = 0$, then there would be an infinite current through the capacitor, which is not possible. This means we can say that immediately after the switch flips states,

$$V_{out}(0) = 0$$

This gives us the first relationship between c_1 and c_2:

$$0 = c_1 + c_2 \tag{1}$$

We can get an initial condition for $\frac{dV_{out}}{dt}$ by looking at the current through the capacitor since:

$$i_c(0) = C\frac{dV_c(0)}{dt}$$

Doing KCL at u_1, we get:

$$i_c(0) + i_L(0) = i_s(0)$$

For the same reason why $V_c(0) = 0$, we know $i_L(0) = 0$, since the voltage across the inductor depends on $\frac{di_L(t)}{dt}$, so $i_L(t)$ cannot change instantaneously. This means:

$$i_c(0) = i_s(0) = \frac{V_s - V_{out}(0)}{R_s} = \frac{V_s}{R_s}$$

Relating i_c back to $\frac{dV_{out}}{dt}$:

$$C\frac{dV_{out}(0)}{dt} = \frac{V_s}{R_s}$$

$$\frac{dV_{out}(0)}{dt} = \frac{V_s}{CR_s}$$

By taking the derivative of $c_1 e^{\lambda_1 t} + c_2 e^{\lambda_2 t}$, plugging in $t - 0$, and setting equal to $\frac{V_s}{CR_s}$, we get the 2nd equation relating c_1 and c_2:

$$\lambda_1 c_1 + \lambda_2 c_2 = \frac{V_s}{CR_s} \tag{2}$$

Equations (1) and (2) gives us a system of equations with two unknowns. Solving the system of equations gives us:

$$c_1 = -\frac{V_s}{R_S C(\lambda_2 - \lambda_1)}$$

$$c_2 = \frac{V_s}{R_S C(\lambda_2 - \lambda_1)}$$

Plugging in component values:

$$c_1 = -\frac{6}{10^3 \times 10^{-15} \times (-2+8)10^{11}} = -10$$

$$c_2 = \frac{6}{10^3 \times 10^{-15} \times (-2+8)10^{11}} = 10$$

This gives us:

$$V_{out}(t) = -10e^{-8\times 10^{11} t} + 10e^{-2\times 10^{11} t}$$

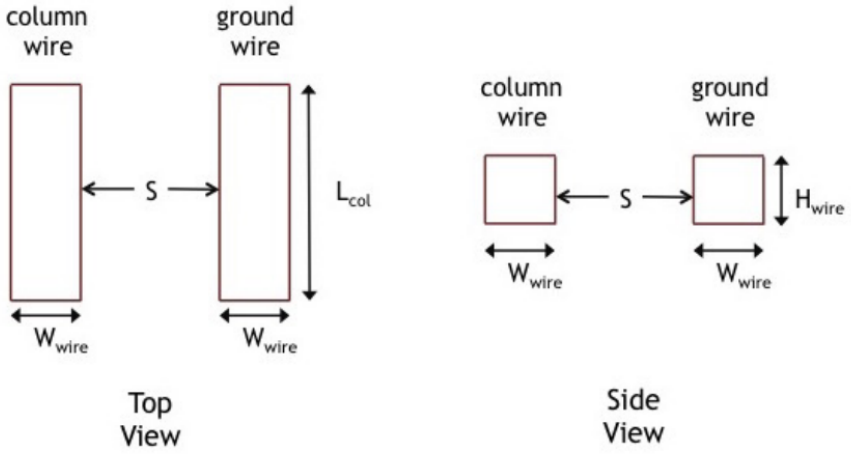
3. DRAM: How Big Can We Make Them?

Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor is typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store $>$ 8 billion bits and is sold for $\approx$ \$3-\$5.

At the most basic level, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a "1" or a "0" is stored in that location. In order to pack as many bits together as possible on to a single chip, rather than running a massive number of wires to access every single bit of the DRAM individually, the bits are arranged into a set of columns, where each column uses a single wire to access information from one of the bits. By turning ON the access switch within the particular bit cell via the single column wire, the corresponding bit is accessed (while leaving all of the switches in the rest of the cells off).

In this problem we'll take a look at how long we can make the DRAM columns and still get the device to work at a reasonable speed. For the purpose of this problem we'll mostly ignore details of how the DRAM actually works (and that making the column too long might actually stop the device from functioning at all) and just focus on the delay introduced by the column wire due to its resistance and its capacitance.

The column wire and its adjacent ground wire are arranged as follows.



Each DRAM cell that gets added adds a length of 0.5μm (i.e., $0.5 \cdot 10^{-6}$ m) to the column and ground wires, the spacing between the column and ground wires is $S = 0.1\mu$m, and the wires have dimensions $H_{wire} = W_{wire} = 0.5\mu$m. Note that you can assume that the two wires are separated by air; in a real chip they would be separated by silicon dioxide, but we'll ignore that for this exercise. You should also assume that all of the capacitance is purely parallel plate. Furthermore, you can assume that the wire is made out of copper, with a resistivity $\rho = 1.68 \times 10^{-8}\Omega$·m.

(a) As a function of the number of cells on the column N_{cells}, what is the total capacitance of the column wire?

Solution: From EE16A, we know that the equation for capacitance of parallel plate is

$$C = \frac{\varepsilon_0 A}{d}$$

Here, ε_0 is the permittivity of free space (about $8.854 \times 10^{-12} \frac{F}{m}$), A is the area of the parallel plate capacitor, and d is the separation distance between the two plates. Using the variables as defined in the problem ($L_{cell} = 0.5\mu$m, which is the length of wire per cell),

$$C = \frac{\varepsilon_0 H_{wire} L_{cell}}{S}$$

By increasing the number of cells, we are just increasing the area of the parallel plate capacitor by the specified amount, which is equivalent to having the capacitors connected in parallel.

$$C_{tot} = N_{cells} \frac{\varepsilon_0 H_{wire} L_{cell}}{S} = 2.21 \times 10^{-17}\text{F} \times N_{cells}$$

(b) As a function of the number of cells on the column N_{cells}, what is the total resistance of the column wire?

Solution: From EE16A, we know the equation for resistance of a wire:

$$R = \frac{\rho L}{A}$$

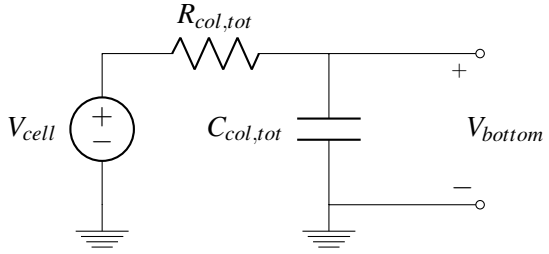
In this equation, ρ is the resistivity of the material, L is the length of the wire, and A is the cross sectional area of the wire. Using the variables defined in the problem:

$$R = \frac{\rho L_{cell}}{H_{wire} W_{wire}}$$

The resistors that form each cell are in series here (this can be seen by the fact that they are clearly connected end to end within each ground and column wire). Thus we get

$$R = N_{cells} \frac{\rho L_{cell}}{H_{wire} W_{wire}} = N_{cells} \times (3.36 \times 10^{-2})\Omega$$

(c) Assuming that we can model the column wire and the top DRAM cell as below (note that this is not a truly accurate model, but it gives the right form for the answer), what will be the delay between information from the top of the DRAM column arriving to the bottom of the DRAM column (i.e., the delay between V_{cell} and V_{bottom}) as a function of N_{cells}? We define the delay to be the length of time it takes for the output value to reach $1/2$ of it's final value. Note that $V_{bottom}(0) = 0V$



Solution: In this case, it is defined as the time it takes for $V_{bottom} = \frac{1}{2}V_{cell}$.

We recognize that this is exactly the same circuit as the pull-up network from class. Therefore we have the following relation

$$V_{bottom} = V_{cell}(1 - e^{\frac{t}{\tau}})$$
$$\tau = -R_{col}C_{col}$$

Substituting in and solving for the delay, we get the following

$$\begin{aligned}
V_{bottom}(t) &= V_{cell}(1 - e^{\frac{t}{\tau}}) \\
\frac{V_{bottom}(t)}{V_{cell}} &= 1 - e^{\frac{t}{\tau}} \\
\frac{1}{2} &= 1 - e^{\frac{t_d}{\tau}} \\
e^{\frac{t_d}{\tau}} &= \frac{1}{2} \\
\frac{t_d}{\tau} &= ln(\frac{1}{2}) \\
t_d &= -ln(2)\tau \\
t_d &= ln(2)R_{col}C_{col} \\
t_d &= ln(2)(N_{cells}\frac{\rho L_{cell}}{H_{wire}W_{wire}})(N_{cells}\frac{\varepsilon_0 H_{wire}L_{cell}}{S}) \\
t_d &= ln(2)N_{cells}^2\frac{\rho\varepsilon_0 L_{cell}^2}{W_{wire}S} \\
t_d &= N_{cells}^2 \times (5.15 \times 10^{-19})s
\end{aligned}$$

What is interesting to note here is that the time delay doesn't scale linearly with an increase in column, but quadratically. This dramatically decreases the number of cells we can put into a column.

(d) Given your answer to part (c), how many cells could you put on a single column (i.e., solve for N_{cells}) such that DRAM can operate at $400MHz$ (i.e. a $2.5ns$ clock period).

Solution: From above, we have the following relation:

$$2.5 \times 10^{-9} = N_{cells}^2 \times (5.15 \times 10^{-19})$$
$$N_{cells} = 69640$$

(e) For the sake of comparison, how long would it take for light to travel from the top of the column to the bottom of the column for the dimension of column wire associated with your answer to part (d)? Note that the speed of light is $c = 3 \times 10^8 \frac{m}{s}$

Solution:

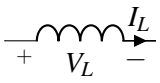
$$L_{cell} = 0.5\mu m$$
$$t_{light} = \frac{L_{cell}N_{cell}}{c} = 0.116ns$$

4. Speakers revisited

In EE16A you were given several homework problems where we had to build circuits to drive a speaker, and you were told to model the speaker as being an 8Ω resistor. In this problem we will develop a somewhat more accurate model for the speaker and use this model to understand a few interesting characteristics and limitations of these devices.

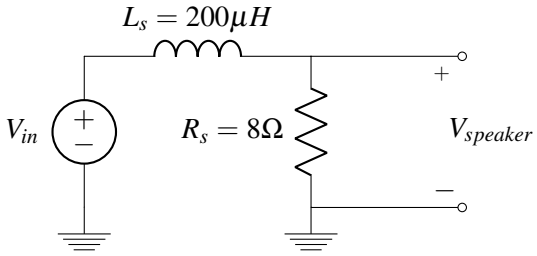
As we will learn about in more detail later on in this class, it turns out that besides just a resistance, speakers usually have another "parasitic" (i.e., potentially undesired) circuit element associated with them - this element is known as an inductor. The symbol for an inductor is shown below; the physics behind this relationship will be covered later, but for now all you need to know is that the inductor enforces the following relationship between its voltage and its current:

$$V_L = L \times \frac{dI_L}{dt}$$



where L is the "inductance" (which has units of Henries, with typical values in the range of pH to mH).

For the rest of the problem we will assume that the speaker is driven by an ideal voltage source, and that we can now model the speaker as follows:



Note that the audio coming out of the speaker is directly set by $V_{speaker}$ - i.e., in the model above, the voltage across the resistor is what we care about in terms of what we hear.

(a) If V_{in} is statically set to 1V (i.e., V_{in} is and always has been 1V), what will $V_{speaker}$ be?

Solution: If V_{in} is statically set, we can solve for the voltage across the inductor fairly easily. Because the voltage is static, that means the current through the circuit is also static (ie, the current is not changing). This means $\frac{dI_L}{dt} = 0$, implying $V_L = 0$. Thus, all the voltage drop is across the resistor, and $V_{speaker} = V_{in} = 1V$.

(b) Now let's start examining what may happen when V_{in} changes. Write the differential equation relating $V_{speaker}$ to V_{in}, R_s, and L_s.

Solution: Let the current I be flowing left to right across the inductor, which also means it flows down through the resistor. We know $I = \frac{V_{speaker}}{R_s}$. We also know that $(V_{in} - V_{speaker}) = L_s \frac{dI}{dt}$. Differentiating

the first equation and placing it within the second gives us

$$\frac{dI}{dt} = \frac{1}{R_S}\frac{dV_{speaker}}{dt}$$
$$V_{in} - V_{speaker} = L_s\left(\frac{1}{R_s}\frac{dV_{speaker}}{dt}\right)$$
$$V_{in} = \frac{L}{R_s}\frac{dV_{speaker}}{dt} + V_{speaker}$$

Interestingly, this is a very similar form to the RC circuit we saw in class! In fact, we already know the solutions to this equation.

(c) If V_{in} starts at 1V and then instantaneously transitions to 0V, solve the differential equation from part (b) and sketch the resulting waveform $V_{speaker}(t)$.

Solution:

$$V_{in} = \frac{L}{R_s}\frac{dV_{speaker}}{dt} + V_{speaker}$$
$$V_{in} - V_{speaker} = \frac{L}{R_s}\frac{dV_{speaker}}{dt}$$
$$-V_{speaker} = \frac{L}{R_s}\frac{dV_{speaker}}{dt}$$

The last step we did because V_{in} is zero for all time $t > 0$. We will need it later to set the boundary conditions.

We know that eigenfunctions of the derivative function of exponentials, so we substitute an arbitrary exponential ($V_0 e^{\frac{t}{\tau}}$) into the equation to solve.

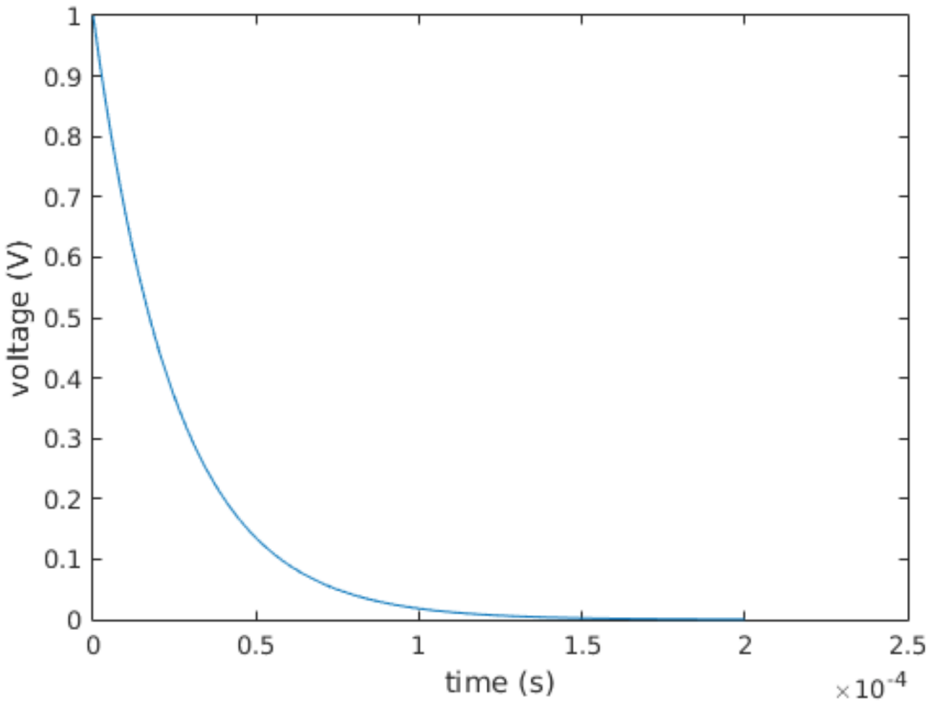
$$-V_{speaker} = \frac{L}{R_s}\frac{dV_{speaker}}{dt}$$
$$-V_0 e^{\frac{t}{\tau}} = \frac{L}{R_s}\frac{1}{\tau}V_0 e^{\frac{t}{\tau}}$$
$$\tau = -\frac{L}{R_s}$$

Now we need to solve for V_0, which is the initial value of the exponential. We know that at times $t < 0$ that the inductor had zero volts across it, and therefore $V_{speaker} = V_{in}$. The inductor resists sudden change to voltage, as can be seen by the relation $V = L\frac{dI}{dt}$. Taking the integral of both sides, we see that $\int V\,dt = LI$. If a sudden change of voltage were to occur, it would not change the output current. From this we can say that the boundary between the two states should be continuous and $V_0 = 1V$. Thus, our final answer is:

$$V_{speaker} = 1V \times e^{-\frac{R_s t}{L}}$$

This is a decaying exponential starting from time t = 0. The plot would look like the following:

(d) Given your solution to (c), how long will it take for $V_{speaker}$ to reach 0.25V?



Solution:

$$V_{speaker} = 1V \times e^{-\frac{R_s t}{L}}$$
$$\frac{1}{4} = e^{-\frac{R_s t}{L}}$$
$$-2ln(2) = -\frac{R_s t}{L}$$
$$t = 2ln(2)\frac{L}{R_s}$$
$$t = 3.47 \times 10^{-5} s$$

5. CMOS Scaling

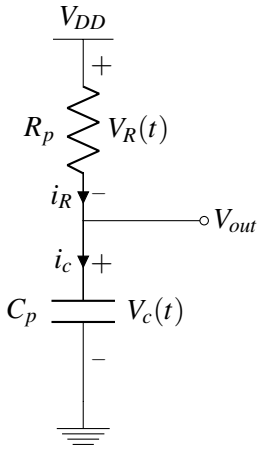
Jerry wants to create a new machine learning accelerator chip utilizing CMOS technology. When designing his chip, he considers the most important parameters of his design to be the amount of energy dissipated when the gate transisions, and the delay time it takes for the output of a gate to hit $\frac{V_{DD}}{2}$ from either ground or V_{DD} (i.e. the delay of the gate).

Jerry has access to two different fabrication processes: process A and process B.

Process A uses a supply voltage of $V_{DD} = 1$V. The transistors have a parasitic resistance of $R_p = 10$kΩ, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 5$fF.

Process B uses a supply voltage of $V_{DD} = 3$V. The transistors have a parasitic resistance of $R_p = 30$kΩ, and the output driven by a representative inverter has a parasitic capacitance of $C_p = 1$fF.

In order to determine which process is better for the design, Jerry decides to analyze the circuit where the input of an inverter transitions from V_{DD} to 0. This can be modeled as the following circuit:



Since the input of the inverter is transitioning from V_{DD} to 0, the initial condition for $V_c(t)$ is:

$$V_c(0) = 0$$

(a) Using the values of V_{DD}, R_p, and C_p from process A, calculate the total energy delivered by the voltage source, V_{DD}, while the capacitor is being charged to V_{DD}. Also calculate the time it takes for V_{out} to reach $\frac{V_{DD}}{2}$.

Solution:

In order to determine the energy dissipation and delay time, first we need to find an expression for $V_{out}(t)$

$$V_c(t) = V_{out}(t)$$

KCL at V_{out}:

$$i_R = i_c$$

$$\frac{V_{DD} - V_{out}}{R_p} = C_p \frac{dV_{out}}{dt}$$

$$\frac{dV_{out}}{dt} + \frac{1}{R_p C_p} V_{out} = \frac{V_{DD}}{R_p C_p}$$

Using substitution of variables:

$$x = V_{out} - V_{DD}$$

$$V_{out} = x + V_{DD}$$

$$\frac{dV_{out}}{dt} = \frac{dx}{dt}$$

$$\frac{dx}{dt} + \frac{1}{R_p C_p} x = 0$$

$$x(t) = Ae^{-\frac{t}{R_pC_p}}$$

$$V_{out}(t) = V_{DD} + Ae^{-\frac{t}{R_pC_p}}$$

Using our initial condition:

$$V_{out}(0) = 0 = V_{DD} + A$$

$$A = -V_{DD}$$

$$V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{R_pC_p}}\right)$$

We can now find the delay time by setting $V_{out}(t) = \frac{V_{DD}}{2}$:

$$\frac{V_{DD}}{2} = V_{DD}\left(1 - e^{-\frac{t}{R_pC_p}}\right)$$

$$\frac{1}{2} = e^{-\frac{t}{R_pC_p}}$$

$$\ln\left(\frac{1}{2}\right) = -\frac{t}{R_pC_p}$$

$$t = -\ln\left(\frac{1}{2}\right)R_pC_p$$

From this, we can say that the delay time to reach $\frac{V_{DD}}{2}$ for any R_p and C_p is:

$$t_d = 0.69R_pC_p$$

Next, we need to find an equation for the energy delivered. The total energy delivered by the source:

$$U_s = \int_0^\infty V_{DD} i_R(t) dt$$

$$i_R(t) = C_p \frac{dV_{out}}{dt}$$

$$i_R(t) = C_p V_{DD} \frac{1}{R_pC_p} e^{-\frac{t}{R_pC_p}} = \frac{V_{DD}}{R_p} e^{-\frac{t}{R_pC_p}}$$

$$U_s = \int_0^\infty (V_{DD})\left(\frac{V_{DD}}{R_p} e^{-\frac{t}{R_pC_p}}\right) dt$$

$$U_R = \int_0^\infty \frac{V_{DD}^2}{R_p} e^{-\frac{t}{R_pC_p}} dt$$

$$U_s = \left(\frac{V_{DD}^2}{R_p}\right)\left(-R_pC\right) e^{-\frac{t}{R_pC_p}}\Bigg|_0^\infty$$

The total energy supplied by the supply when charging up the capacitor is:

$$U_s = CV_{DD}^2$$

Plugging in component values of process A for the energy dissipation and time delay:

$$U_s = (5 \times 10^{-15})1^2 = 5 \times 10^{-15}\text{J}$$

$$t_d = 0.69(10 \times 10^3 \times 5 \times 10^{-15}) = 3.45 \times 10^{-11}\text{s}$$

(b) Repeat part (a), but with the values from process B.

Solution:

Using the equations from part (a):

$$U_s = (1 \times 10^{-15})3^2 = 9 \times 10^{-15}\text{J}$$

$$t_d = 0.69(30 \times 10^3 \times 1 \times 10^{-15}) = 2.07 \times 10^{-11}\text{s}$$

(c) Compare the energy and delay of process A and B

Solution:

Compared to process B, process A dissipates less energy per transition, but has a longer delay time.

(d) Jerry's friend Pat tells Jerry that with process B, one can reduce V_{DD} to 2V. However, the reduction in supply voltage increases the parasitic resistance R_p to 50kΩ. Calculate the new delay and energy.

Solution:

$$U_s = (1 \times 10^{-15})2^2 = 4 \times 10^{-15}\text{J}$$

$$t_d = 0.69(50 \times 10^3 \times 1 \times 10^{-15}) = 3.45 \times 10^{-11}\text{s}$$

(e) Based on your previous answers, which process should Jerry choose to use?

Solution:

With the new V_{DD} and R_p of process B, it ends up that process B and process A have the same delay time. However, process B dissipates less energy per transition, which means Jerry should choose process B.

6. Write Your Own Question And Provide a Thorough Solution.

Writing your own problems is a very important way to really learn material. The famous "Bloom's Taxonomy" that lists the levels of learning is: Remember, Understand, Apply, Analyze, Evaluate, and Create. Using what you know to create is the top level. We rarely ask you any homework questions about the lowest level of straight-up remembering, expecting you to be able to do that yourself (e.g. making flashcards). But we don't want the same to be true about the highest level. As a practical matter, having some practice at trying to create problems helps you study for exams much better than simply counting on solving existing practice problems. This is because thinking about how to create an interesting problem forces you to really look at the material from the perspective of those who are going to create the exams. Besides, this is fun. If you want to make a boring problem, go ahead. That is your prerogative. But it is more fun to really engage with the material, discover something interesting, and then come up with a problem that walks others down a journey that lets them share your discovery. You don't have to achieve this every week. But unless you try every week, it probably won't ever happen.

Contributors:

- Siddharth Iyer.
- Jaymo Kang.
- Kyle Tanghe.