*1. Summarize the (at most) 3 key main ideas.*

1. The motivation for creating energy efficient memories is due to the increasing data from growth in IoT devices and exascale computers that constantly collect data and perform memory intensive machine learning algorithms that need to meet energy budgets.
2. Explained several solutions researched by Kulkarni for robust energy efficient circuits, such as adaptive and resilient logic and memory design.
3. Kulkarni ended with future research that may be applied to machine learning, 3D nand flash and architecture circuit design such as cache.

*2. State the main contribution of the presentation.*

The main contribution of the presentation was to focus academia towards realizing the need for creating energy efficient memory and showcase and explain the current prospects for solutions and future research possibilities that Kulkarni and his team at Intel are working on.

*3. State the limitation of the presentation.*

The limitation of this presentation is that his main research and circuit designs that will address this issue have not been fully implemented into products for real life use by Intel. Rather, his designs are currently in the process of showing proof of concept through prototypes that hopefully in the future will work.

*4. Find at least one open question and try to answer it.*

Is the 10T Schmitt Trigger bitcell the best option for lowest power consumption.

According to *Low Voltage Low Power SRAM design based on Schmitt Trigger technique,* by Suresh, Padmaja, and Kumari, the ST-2 SRAM has the lowest power dissipation at 0.98N watts vs. the 10T SRAM at 1.89N watts. However, Kulkarni may have chosen the 10T Schmitt Trigger bitcell for other attributes.