

Block diagram Vivado



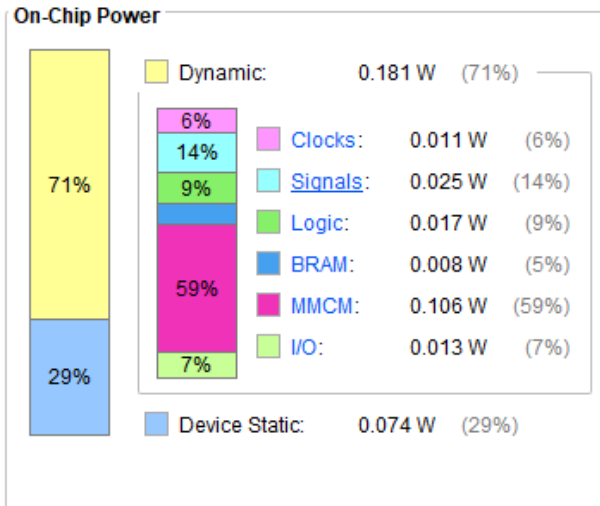
Component	Percentage
LUT	18%
LUTRAM	1%
FF	4%
BRAM	64%
IO	19%
MMCM	20%

Power

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 0.254 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 26.3°C
Thermal Margin: 58.7°C (11.7 W)
Effective θ_{JA} : 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Vitis Result

Here I have taken following matrixes:

A =
 {{1, 2, 3, 4},
 {5, 6, 7, 8},
 {9, 10, 11, 12},
 {13, 14, 15, 16}}

B =
 {{1, 0, 0, 0},
 {0, 1, 0, 0},
 {0, 0, 1, 0},
 {0, 0, 0, 1}};

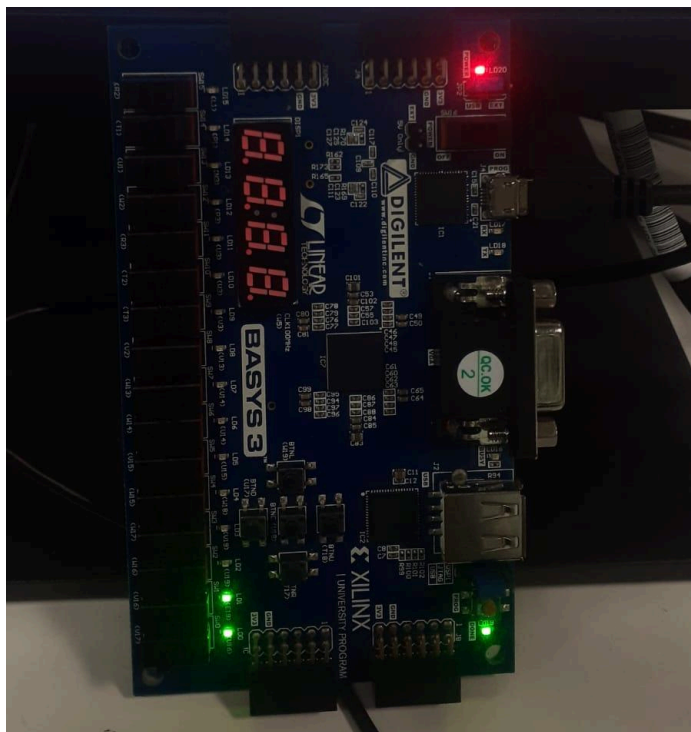
D =
 {{1, 2, 3},
 {4, 5, 6},
 {7, 8, 9},
 {10, 11, 12}};

```
Console Vitis Serial Terminal Executables Debug Shell Vitis Log Problems Debugger Console
Connected to: Serial ( COM13, 9600, 0, 8 )

Already connected to port: COM13Already connected to port: COM13GPIO INIT SUCCESSFUL
max = 16, min = 1
max_new = 3608, min_new = 190

-----1-iteration-----
Max value: 16
|Min value: 1
|add = 17 |sub = 15 |div = 16 |mod = 0 |
-----2-iteration-----
Max value: 3608
|Min value: 190
|add = 3798 |sub = 3418 |div = 18 |mod = 188 |
-----1-iteration-----
Max value: 16
|Min value: 1
|add = 17 |sub = 15 |div = 16 |mod = 0 |
-----2-iteration-----
Max value: 3608
|Min value: 190
|add = 3798 |sub = 3418 |div = 18 |mod = 188 |
-----1-iteration-----
Max value: 16
|Min value: 1
|add = 17 |sub = 15 |div = 16 |mod = 0 |
-----2-iteration-----
Max value: 3608
|Min value: 190
|add = 3798 |sub = 3418 |div = 18 |mod = 188 |
```

Basys3 demo



Live demo

https://drive.google.com/file/d/1T70s9CmqojA2KPrL29cNFhQhcgU9m-IZ/view?usp=drive_link