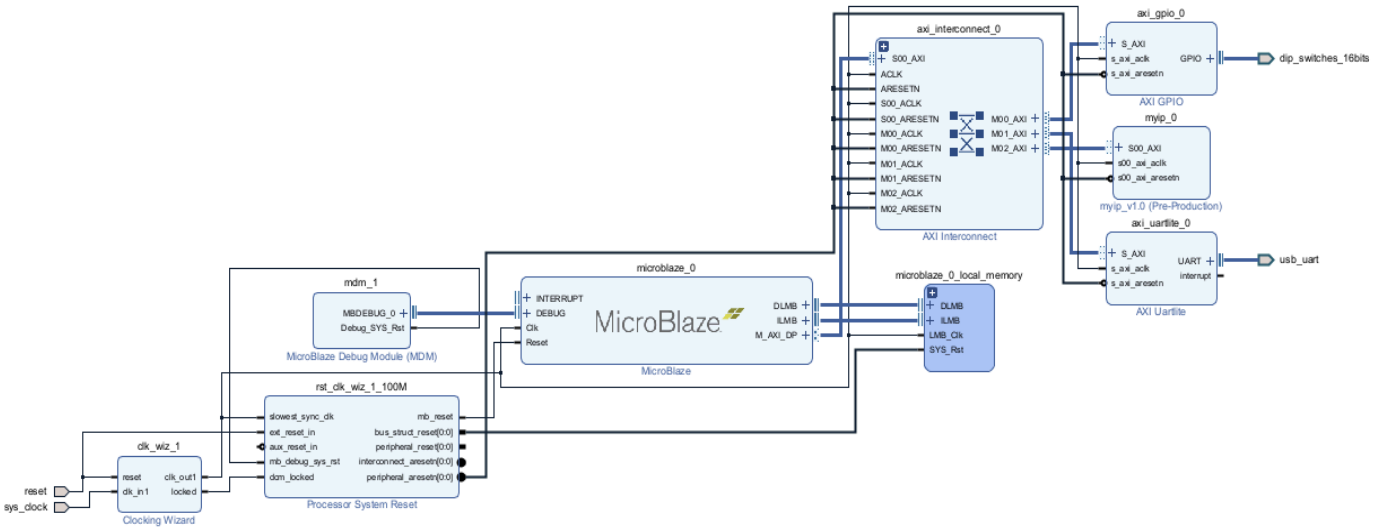
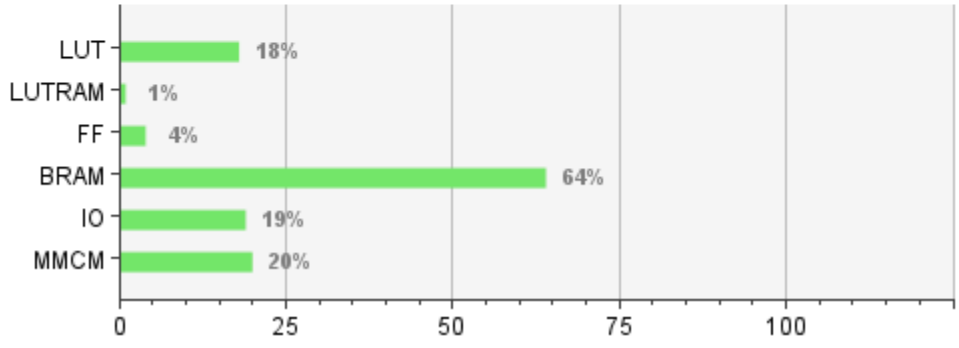
Ayush Dixit (M23EEV006)
Without using SD CARD**
Block diagram Vivado



Utilization

Resource	Utilization	Available	Utilization %
LUT	3838	20800	18.45
LUTRAM	138	9600	1.44
FF	1637	41600	3.94
BRAM	32	50	64.00
IO	20	106	18.87
MMCM	1	5	20.00

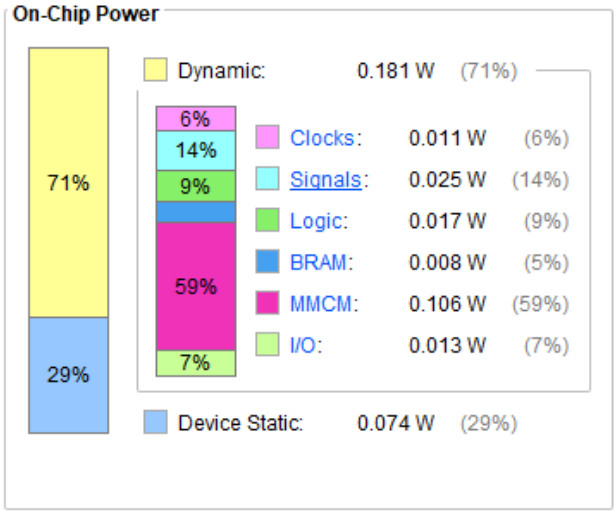


Power

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.254 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.3°C**
Thermal Margin:	58.7°C (11.7 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

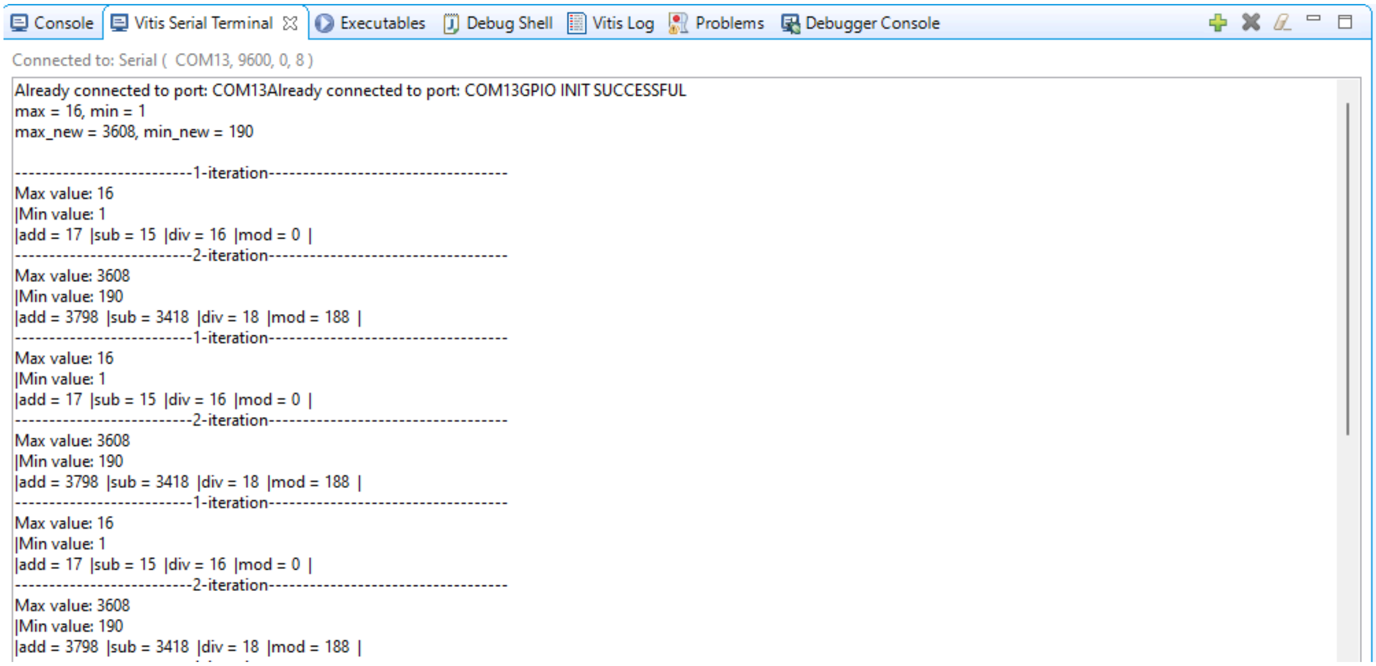


Vitis Result
Here I have taken following matrixes:

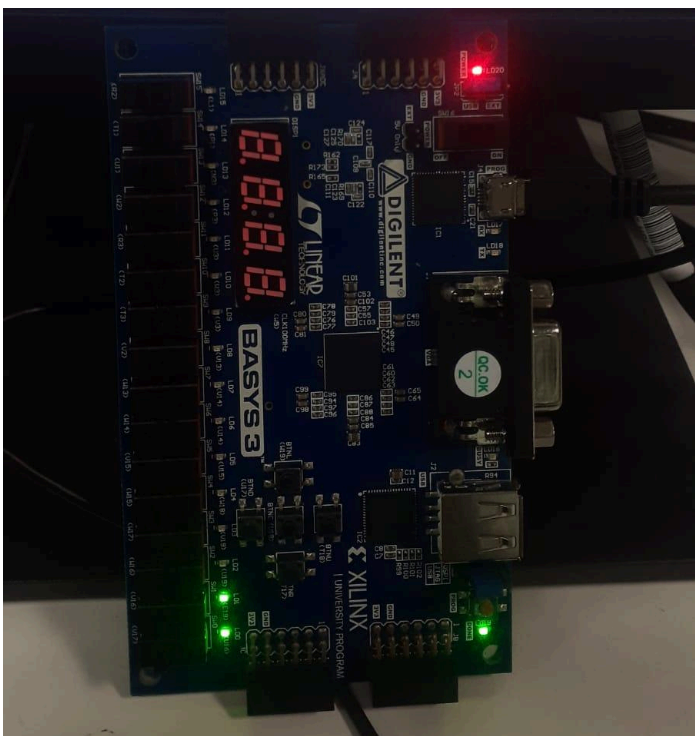
A = {{1, 2, 3, 4},
{5, 6, 7, 8},
{9, 10, 11, 12},
{13, 14, 15, 16}}

B = {{1, 0, 0, 0},
{0, 1, 0, 0},
{0, 0, 1, 0},
{0, 0, 0, 1}};

D = {{1, 2, 3},
{4, 5, 6},
{7, 8, 9},
{10, 11, 12}};



Basys3 demo



Live demo

https://drive.google.com/file/d/1T70s9CmqojA2KPrL29cNFiQhcgU9m-IZ/view?usp=drive_link