Lab 4

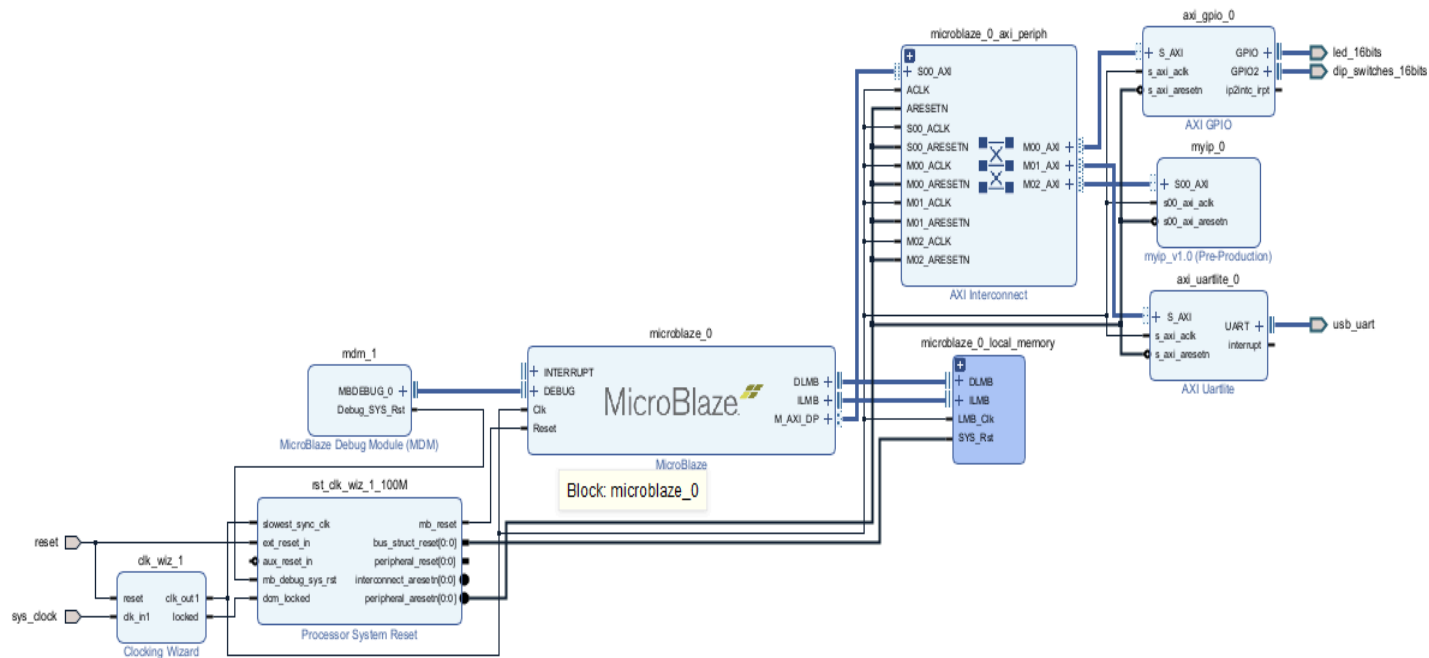## Block diagram

*Deployed on basys3 fpga board

Deployed on basys3 FPGA

With custom Axi peripheral for doing subtraction
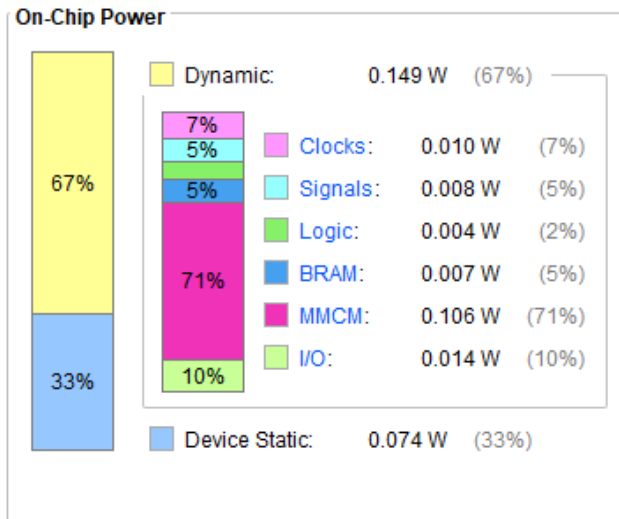
Utilization

Resource	Utilization	Available	Utilization %
LUT	1651	20800	7.94
LUTRAM	138	9600	1.44
FF	1849	41600	4.44
BRAM	32	50	64.00
IO	36	106	33.96
MMCM	1	5	20.00

Power

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.223 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.1°C**
Thermal Margin:	58.9°C (11.7 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.149 W	(67%)	
Clocks:	0.010 W	(7%)	
Signals:	0.008 W	(5%)	
Logic:	0.004 W	(2%)	
BRAM:	0.007 W	(5%)	
MMCM:	0.106 W	(71%)	
I/O:	0.014 W	(10%)	
Device Static:	0.074 W	(33%)	

67% 33% 7% 5% 5% 71% 10%

Vitis

| Console | Vitis Serial Terminal ✕ | Executables | Debug Shell | Vitis Log | Problems | Debugger Console |

Connected to: Serial (COM13, 9600, 0, 8)

```
Already connected to port: COM13GPIO INIT SUCCESSFUL
/////////Welcome to the Application ///////////////
UART= 9600  Second switch is pressed!
Max value: 80
result  = 30  Second switch is pressed!
Max value: 80
result  = 30  Second switch is pressed!
Max value: 80
result  = 30  Second switch is pressed!
Max value: 80
result  = 30
```

MAX = 80
RESULT = 80 - 50 = 30
LED = MULTIPLE LEDS SHOULD BE TURN ON