Differential Voltage Sense Amplifier

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Connections Between Sense Amplifier and 6T SRAM Cell

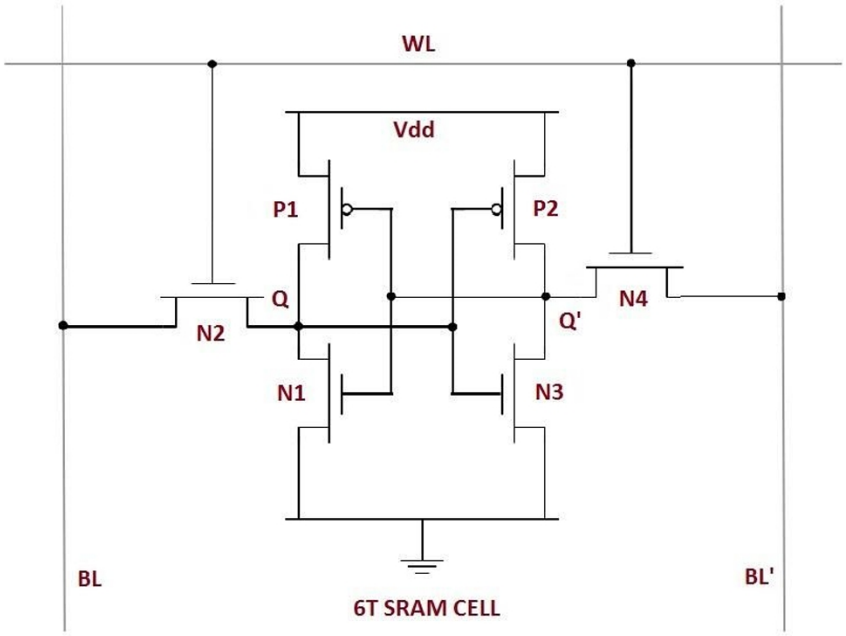

Figure 1: 6T SRAM CELL

Components of the Circuit

- **6T SRAM Cell:**
  - *Bitlines (bl and $\overline{bl}$):* These lines carry the differential voltage representing the stored data.
  - *Wordline (WL):* Enables access to the SRAM cell during a read or write operation.
  - *Access Transistors:* NMOS transistors connecting the storage nodes of the SRAM to the bitlines, controlled by the wordline.

Connections

1. **Bitlines (bl and $\overline{bl}$):**
   - The differential bitlines from the SRAM cell are directly connected to the input terminals of the sense amplifier.
   - These bitlines carry a small voltage difference representing the data stored in the SRAM cell.
2. **Wordline (WL):**
   - The wordline is connected to the access transistors of the SRAM cell.

- When activated, it allows the stored data to appear as a differential voltage on the bitlines.

3. **Sense Amplifier Enable (SAEn):**
   - The SAEn signal is connected to the NMOS transistor (N3) in the sense amplifier circuit.
   - When SAEn is high, the sense amplifier is activated, and the small voltage difference on the bitlines is amplified.
4. **Power (Precharge):**
   - The bitlines are precharged to V_{DD} before the read operation using a precharge circuit controlled by the PCH signal.

Working

1. During the **Precharge Phase**, the bitlines (bl and $\overline{bl}$) are precharged to V_{DD} by the precharge circuit.
2. When the **Wordline (WL)** is enabled, the access transistors of the 6T SRAM cell connect the storage nodes to the bitlines, creating a small voltage difference based on the stored data.
3. The **Sense Amplifier (SA)** is enabled by the $SAEn$ signal, amplifying the small differential voltage on the bitlines to full logic levels.

Circuit Layout Guidance

- **Placement:** The sense amplifier should be placed as close as possible to the SRAM array to minimize parasitic capacitance and signal delay.
- **Matching:** Ensure that the bitlines and transistors in the sense amplifier are carefully matched to avoid offset errors.
- **Power Routing:** Provide dedicated power routing for the sense amplifier to handle the current during the amplification phase.

Circuit Description

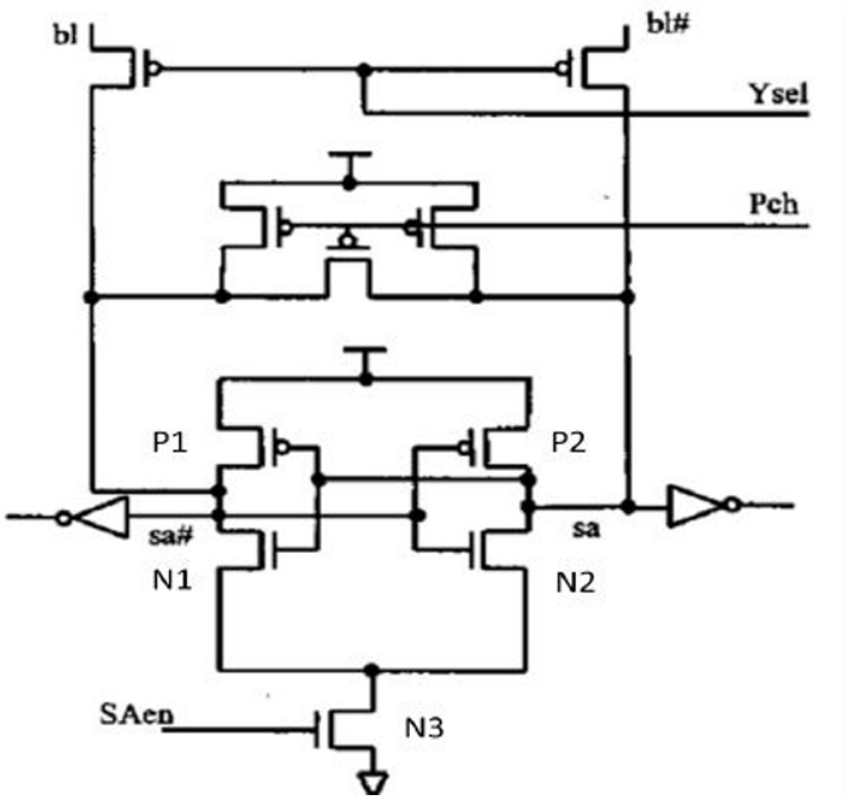

Figure 2: Differential Sense Amplifier

Sense Amplifier:

- *Input Terminals (bl and $\overline{bl}$):* Connected to the bitlines from the SRAM array.
- *SAEn (Sense Amplifier Enable):* Activates the sense amplifier during a read operation.
- *Cross-Coupled Inverters:* Amplify the small voltage difference between the bitlines.

Components and Connections

- **Bitlines (bl and $\overline{bl}$):** These are the input lines from the memory array. They carry the small voltage difference representing the data stored in memory cells.
- **P1 and P2 (PMOS Transistors):** Form part of the cross-coupled inverter circuit. Their gates are connected to the outputs (sa and $\overline{sa}$) of the opposite inverter, enabling positive feedback.
- **N1 and N2 (NMOS Transistors):** Connected in parallel to form the pull-down path. Their gates are connected to the bitlines (bl and $\overline{bl}$), and they control which bitline is pulled low.
- **N3 (NMOS Transistor):** Controlled by the *SAEn* (Sense Amplifier Enable) signal. It acts as the enable switch for the amplifier circuit.
- **Ysel (Column Selector):** Enables this specific sense amplifier for operation.

Working

1. When a wordline (WL) is enabled, it selects a memory cell, and a small voltage difference develops between bl and $\overline{bl}$.

2. When $SAEn$ is activated, N3 turns on, allowing the cross-coupled inverters (P1-P2 and N1-N2) to amplify this differential signal.

3. Positive feedback ensures one side (sa or $\overline{sa}$) goes high (VDD), and the other side goes low (GND), depending on the initial voltage difference between bl and $\overline{bl}$.

Control Signals

- **PCH (Precharge):** Used to precharge the bitlines (bl and $\overline{bl}$) to VDD before a read operation. Ensures that both bitlines start at the same voltage.
- **SAEn (Sense Amplifier Enable):** Activates the sense amplifier to read and amplify the differential voltage on the bitlines.
- **WL Enable:** Activates the wordline of the desired memory cell to develop the voltage differential.

Timing Diagram

The timing diagram explains the sequence of control signals during a read operation:

- **Precharge (PCH):** High at the beginning to precharge the bitlines.
- **Wordline Enable (WL Enable):** Goes high to activate the memory cell and create a differential voltage on the bitlines.
- **SAEn (Sense Amplifier Enable):** After a delay (Δt), $SAEn$ goes high to enable the sense amplifier.
- **Ysel:** Ensures the column with the required bitline pair is selected.

Key Connections

- **Bitlines (bl and $\overline{bl}$):** Connected to the memory cell array.
- **Wordline (WL):** Connected to the row decoder to activate specific memory cells.
- **SAEn:** Connected to the control circuitry to enable the sense amplifier.
- **PCH:** Connected to the precharge circuit to initialize the bitlines.
- **Ysel:** Connected to the column selection circuitry for selecting the appropriate sense amplifier.

Detailed Design Guidance

- **Precharge Circuit:** Use PMOS transistors for precharging the bitlines to VDD, controlled by the PCH signal.
- **Sense Amplifier Enable (SAEn):** Ensure proper timing synchronization between $SAEn$, $WL\ Enable$, and PCH for accurate data sensing.
- **Layout Design:**
  - Place sense amplifiers close to the memory cells for minimal signal delay.
  - Ensure proper matching of bitlines and transistors to avoid offset errors.

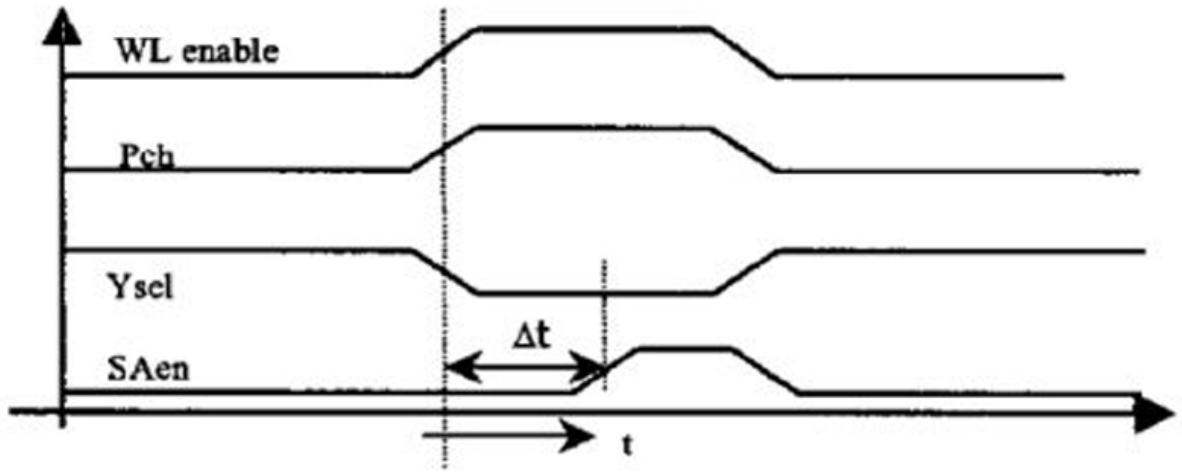

Figure 3: Timing Diagram