64X16 Static Random Access Memory (SRAM)

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***Abstract*—Static Random Access Memory (SRAM) is a type of semiconductor memory that retains data bits as long as power is supplied to the device. Unlike Dynamic RAM (DRAM), which requires periodic refreshing to retain data, SRAM uses flip-flop circuits to store each bit, making it more reliable and faster, but also more expensive and power-consuming. This paper provides an overview of the architecture of SRAM, focusing on its key components including the memory cell, row and column decoders, control circuitry, and sense amplifiers. It discusses the operation principles of read and write cycles, addressing how data is accessed and stored. The control circuitry manages address decoding, read/write operations, and data integrity, ensuring synchronous and reliable data access. Additionally, the paper covers the significance of refresh mechanisms in maintaining data integrity. SRAM's applications are widespread in high-speed memory systems, cache memory, and other scenarios where fast access time and reliability are critical.**

***Index Terms*—memory cell, sensing amplifier, decoder**

I. Introduction

Static Random Access Memory (SRAM) is a type of semiconductor memory that stores data in bistable flip-flop circuits, offering fast access times and reliable data retention as long as power is supplied. Unlike Dynamic RAM (DRAM), which requires regular refreshing, SRAM maintains data without needing to refresh, making it more power-hungry but significantly faster. The basic unit of SRAM is the memory cell, constructed from a pair of cross-coupled inverters that store one bit of data as either 0 or 1. The memory array consists of rows and columns, with row and column decoders selecting specific cells for read or write operations.

The control circuitry manages address decoding, timing, and synchronization, utilizing signals like read/write enable and clock signals. A sense amplifier reads data from the memory cell and amplifies the signal to a readable level. SRAM is commonly used in high-speed applications such as cache memory in microprocessors, embedded systems, and other memory-intensive tasks where fast access and data integrity are critical. Despite its advantages, SRAM is more expensive than DRAM and consumes more power, which limits its use in larger, cost-sensitive memory applications.

II. SRAM (STATIC RANDOM ACCESS MEMORY

The architecture of SRAM (Static Random-Access Memory) refers to the design and organization of its internal components and circuitry. Understanding SRAM architecture is crucial for applications requiring high-speed, low-power memory systems.

KEY COMPONENTS:
- Memory Cell Array
- Row Decoder
- Column Decoder
- Word Lines (WL)
- Bit Lines (BL and BL')
- Sense Amplifiers

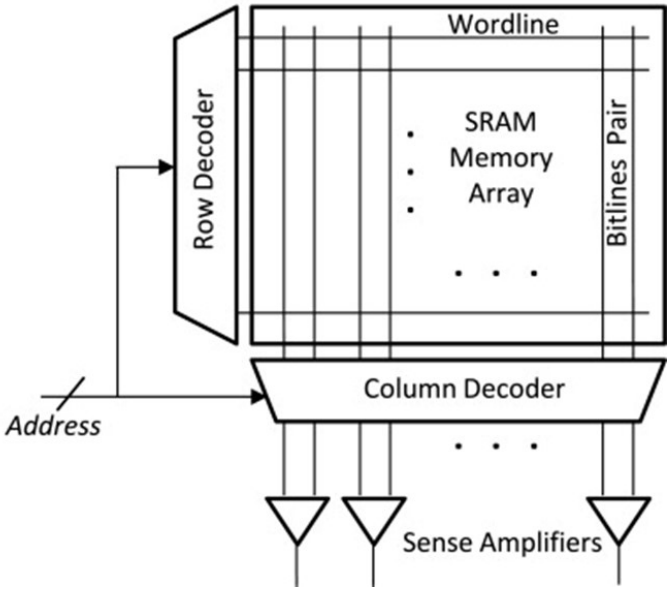

Fig. 1. SRAM ARCHITECTURE

A. Row decoder

The row decoder is a critical component of the SRAM architecture. Its primary function is to decode the input address and activate a specific row (or word line) in the memory array for read or write operations. It ensures that only one row is accessed at a time, while the rest remain inactive.

1) Functionality of the Row Decoder:: The row decoder receives the binary address inputs and translates them into a single active word line. This enables the access transistors of all memory cells in the corresponding row, allowing data to

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be read from or written to the bit lines.
Steps in Operation:
a.Address Input:
A binary address is provided by the control logic to the row decoder.
b.Decoding:
The row decoder converts the binary address into a one-hot signal. For an n-bit address, 2n word lines are possible, and only one word line is activated.
c.Word Line Activation:
The activated word line enables the memory cells in the corresponding row.

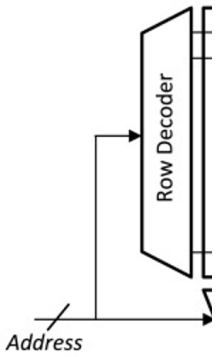

Fig. 2. ROW DECODER

2) Components of a Row Decoder: a.Input Address Lines: Carry the binary address signals (e.g., A0, A1, A2).The number of address lines determines the number of rows in the memory array (2 power of n).
b.Decoder Logic:
Consists of combinational logic gates (AND, OR, NAND, etc.) to decode the binary address. Each unique combination of address bits corresponds to a specific word line.
c.Word Lines:
Horizontal lines in the memory array that connect to all memory cells in a row.Only one word line is activated at a time by the decoder.

3) Design of Row Decoder:: If there are 3 address bits (A2, A1, A0), the row decoder can select one out of 2 power of 3=8 rows. The decoding logic uses AND gates to generate the one-hot signals for the word lines.

4) Types of Row Decoders: generally decoders are 2 types a.Static Decoders:
A static decoder is built using static CMOS logic gates such as AND, OR, NAND, or NOR. The output of the decoder remains stable (high or low) as long as the inputs are stable, and no clock signal is required to control the operation.
b.Dynamic Decoders:
A dynamic decoder uses dynamic CMOS logic instead of static gates. These decoders rely on capacitive charge storage and operate in synchronization with a clock signal.

B. Column Decoder in SRAM:

The column decoder in SRAM is responsible for selecting a specific column of memory cells (bit line) for data access during read and write operations. It works in conjunction with the row decoder to pinpoint the exact memory cell being accessed within the memory array.

1) Purpose of the Column Decoder: The column decoder enables access to the appropriate bit line pair (BL and BL') based on the column address.
Read Operations:
Routing data from the selected bit line to the sense amplifier.
Write Operations:
Enabling the write driver to update the selected bit line with new data.

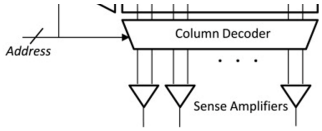

Fig. 3. COLUMN DECODER

2) Components of the Column Decoder: The column decoder consists of the following key components:
a. Address Lines:
• Input signals representing the binary column address.
Decoding Logic:
• Uses combinational logic gates (AND, NAND, etc.) to decode the column address.
• Converts the binary input into a one-hot signal, activating only the targeted column.
b. Multiplexers (MUX):
• In large SRAM arrays, multiplexers are used to reduce the number of sense amplifiers and write drivers.The column decoder activates one MUX channel based on the column address, connecting the selected bit line to the sense amplifier or write driver
. c .Bit Line Pair (BL and BL'):
• Vertical lines in the memory array corresponding to each column.The column decoder controls access to these lines for read and write operation

3) Working of the Column Decoder: a .During Read Operations:
1. The column address is input to the column decoder.
2. The decoding logic activates the corresponding bit line pair.
3. The selected bit line is connected to the sense amplifier via a multiplexer.
4. The sense amplifier amplifies the small voltage difference on the bit lines to determine the stored data ('0' or '1').

b .During Write Operations: 1. The column address is input to the column decoder.
2. The decoding logic activates the corresponding bit line pair.
3. The write driver updates the voltage on the bit lines to store the desired data in the selected memory cell.

4) Types of Column Decoders: a.Static Column Decoder:
• Built using static CMOS gates (similar to static row decoders).Reliable and robust but requires more area.
b. Dynamic Column Decoder:
• Uses dynamic CMOS logic to reduce the number of transistors.Operates faster but requires a clock signal and is more prone to charge leakage.
c.Pre-decoded Column Decoder:
• The decoding process is split into stages (hierarchical decoding). A subset of address bits is decoded in the first stage, and the rest in the second stage.This approach improves scalability and reduces complexity

C. Memory Cell Array in SRAM:

The memory cell array is the core of any SRAM architecture. It is a structured grid where each element is a memory cell capable of storing a single bit of data. The arrangement and functionality of the memory cell array determine the performance, power efficiency, and density of the SRAM.

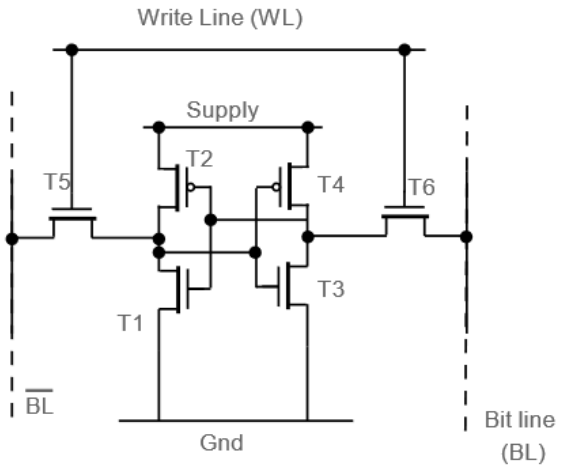

Fig. 4. MEMORY CELL

D. Row decoder

1) Structure:: The array is organized in a matrix/grid format of rows and columns. Rows: Represent word lines, controlled by the row decoder. Columns: Represent bit lines, controlled by the column decoder. Each intersection in the grid is a memory cell capable of storing a single bit.
The basic unit of the memory cell array is the 6T SRAM cell, which consists of:
1. Two Cross-Coupled Inverters:
Form a bistable latch to hold one bit of data (either '0' or '1'). Provide non-volatile behevior as long as power is supplied.
2. Two Access Transistors:
Connect the latch to the bit lines. Controlled by the word line.

2) Working of the Memory Cell Array: 1. Write Operation:
The row decoder activates the desired word line. The column decoder connects the appropriate bit lines to the write driver. The write driver changes the voltage on the bit lines to store the desired data in the selected memory cell.
2. Read Operation:
The row decoder activates the desired word line. The column decoder connects the bit lines to the sense amplifier. The sense amplifier reads the small voltage difference on the bit lines and determines the stored data. The memory cell array is the heart of SRAM, enabling fast, reliable, and stable data storage. It combines optimized circuit design with architectural techniques to achieve high performance and density.

E. sense amplifier

A sense amplifier is a critical component in SRAM, responsible for detecting and amplifying the small voltage difference on the bit lines during a read operation. It ensures fast and accurate data retrieval from memory cells, even when the voltage difference is minimal.

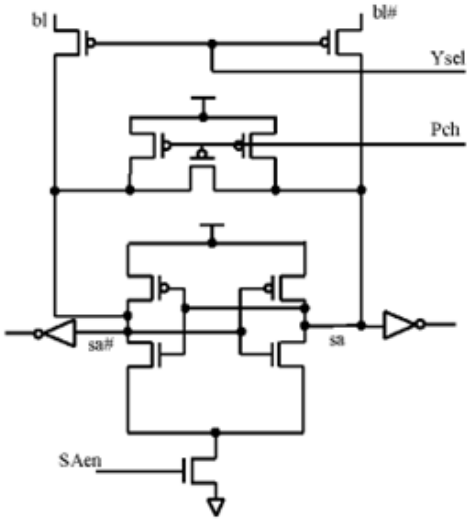

Fig. 5. SENSE AMPLIFIER

1) working of sense amplifier: the working of sense amplifier is mainly devided into two parts.
a .Bit Line Pair:
SRAM cells are connected to differential bit lines BL and BL'. The sense amplifier measures the voltage difference between BLand BL'
b .During a Read Operation:

1. Precharge Phase:
Before reading, both BL and BL' are precharged to the same voltage (usually VDD).This ensures the bit lines start with equal potentials.
2. Differential Development:
When a word line is activated, the memory cell slightly pulls down one of the bit lines BL and BL'.A small voltage difference (delta V) is created between BLand BL'. 3. Amplification:
The sense amplifier detects the small delta V and amplifies it to produce a full logic level (either '0' or '1').This amplified signal is sent to the output or further processing circuits.
c .Differential Sense Amplifier:
Most commonly used in SRAM.A differential amplifier that measures the difference between BL and BL' Advantages of this is High sensitivity. Robust against noise and common-mode variations.

F. Bit Lines in SRAM

Bit lines are vertical lines in the SRAM memory array that serve as the primary communication path for data transfer between the memory cells and peripheral circuits (such as sense amplifiers and write drivers). They are a crucial part of the SRAM architecture, as they enable read and write operations by connecting memory cells to the external data bus.

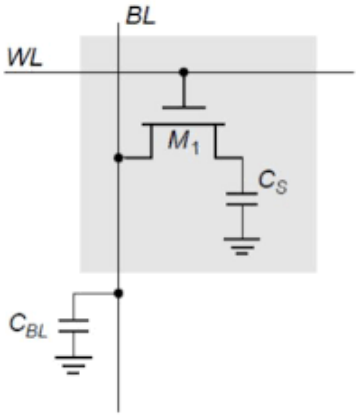

Fig. 6. bit line and word line

G. word line in SRAM

A word line is a horizontal line in the SRAM memory array that enables access to a specific row of memory cells during read and write operations. It plays a crucial role in the addressing mechanism of SRAM, determining which row of memory cells will be active for a particular operation.

H. pre-charge circuit in SRAM

A precharge circuit is a key component of SRAM used to prepare the bit lines BL and BL' for efficient and reliable read and write operations. Before accessing any memory cell, the bit lines are precharged to a common voltage level, typically VDD/2, ensuring that read and write operations start from a balanced and predictable state.

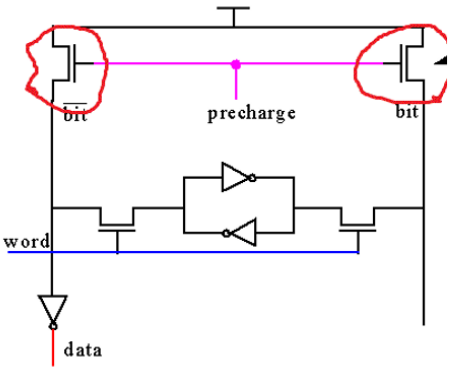

Fig. 7. pre-charge circuit

The precharge circuit is an essential part of SRAM that ensures the reliability and efficiency of memory operations. It prepares the bit lines by setting them to a balanced voltage level before each operation. With advancements in design, modern precharge circuits achieve faster operation, lower power consumption, and greater robustness, making them indispensable in high-performance and low-power SRAM systems.

I. control circuitary

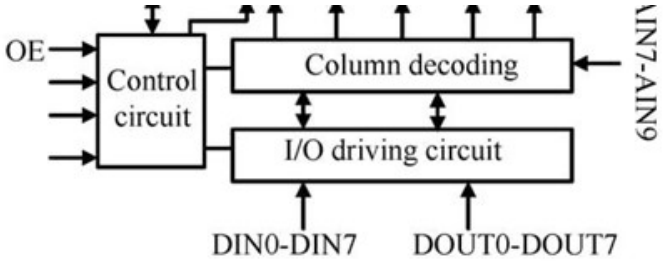

Fig. 8. control circuit

The control circuitry in SRAM (Static Random Access Memory) is responsible for managing the operation of the memory array. It includes various signals and mechanisms that coordinate the read, write, and refresh operations of the SRAM cells. The control circuitry ensures efficient data access and storage Management.

III. CIRCUITS

A. Decoder

1) 2x4 Decoder: A 2x4 decoder is a combinational circuit that decodes a 2-bit binary input into one of four mutually

exclusive output lines. It is used in digital systems for addressing, selecting, or enabling specific outputs based on the binary input. In SRAM, it can be a component of the row or column decoders.

Fig. 9. The 2x4 decoder

a. inputs:
The decoder has 2 input lines (A1 A2) representing a 2-bit binary number.
b. outputs:
It produces 4 output lines (Y0 Y1 Y2 Y3), with only one active (logic HIGH) at any time. The active output corresponds to the binary value of the input. We used AND for constructing the 2x4 decoder.

A_1	A_0	Y_0	Y_1	Y_2	Y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig. 10. truth table of the 2x4 decoder

2) 4x16 decoder: A 4x16 decoder is a combinational logic circuit that decodes a 4-bit binary input into one of 16 mutually exclusive outputs. This type of decoder is commonly used in digital systems for memory addressing, multiplexing, and control logic. Each output corresponds uniquely to a particular 4-bit input combination.

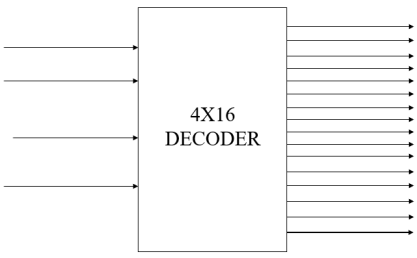

Fig. 11. The 4X16 decoder

a .Inputs:
The decoder has 4 input lines (A3 A2 A1 A0)representing a 4-bit binary number.
b .Outputs:
It produces 16 output lines (Y0 to Y15, with only one active (logic HIGH) at any time. The active output corresponds to the binary value of the input.
c .Using pass transistor logic A 4x16 decoder using pass transistor logic is a method of implementing a decoder circuit where pass transistors are used as switches to control the flow of signals to the output lines. This approach is often preferred due to its efficient use of transistors, reduced number of gates, and improved performance in terms of speed and power consumption.
A 4x16 decoder with pass transistor logic takes a 4-bit binary input and decodes it into one of 16 output lines, with only one active (logic HIGH) output at any time. The core idea is to use pass transistors (analogous to switches) to connect or disconnect the output lines based on the binary input.

3) 6x16 decoder: A 6x16 decoder is a combinational logic circuit that takes a 6-bit binary input and produces one of 16 outputs, with only one output being active (HIGH) at any time. This type of decoder is useful in various digital applications, such as memory address decoding and logic circuit implementation.
a.Inputs:
The decoder has 6 input lines (A5, A4, A3,A2,A1,A0) representing a 6-bit binary number.
b. Outputs:
It produces 16 output lines (Y0 to Y15).Each output corresponds uniquely to a particular 6-bit input combination.

B. Unit SRAM

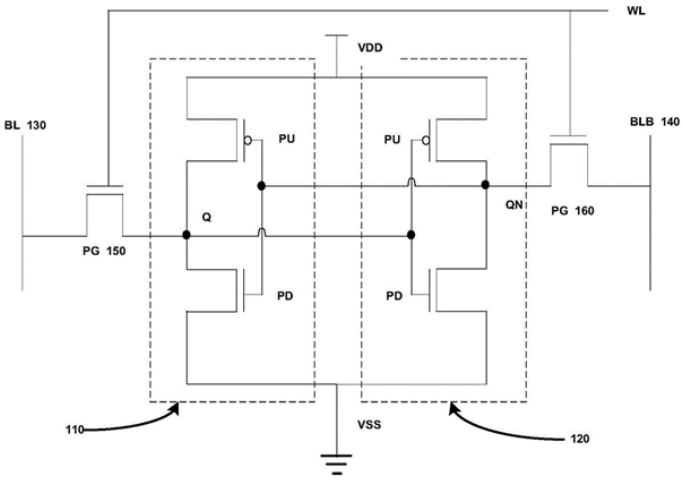

Fig. 12. UNIT SRAM

1) 2X2 SRAM: A 2x2 SRAM (Static Random Access Memory) is a basic form of SRAM that consists of 2 bits of storage, organized into a 2-row by 2-column matrix. It is

a simplified example of SRAM architecture, illustrating the basic principles of how data is stored and accessed.
Structure and Architecture
• Number of Cells: A 2x2 SRAM has 4 SRAM cells. Each cell can store 1 bit of data. The memory is divided into rows and columns: Rows: 2 rows. Columns: 2 columns.

2) 4x4 SRAM: A 4x4 SRAM (Static Random Access Memory) is a slightly more complex version of an SRAM, consisting of 16 memory cells arranged in a 4-row by 4-column matrix. Each cell stores 1 bit of data, and the memory is designed to store and access data efficiently. Let's break down the structure, operation, and key concepts involved in a 4x4 SRAM. Structure and Architecture Number of Cells: A 4x4 SRAM has 16 SRAM cells. Each cell stores 1 bit of data. The memory is divided into rows and columns: Rows: 4 rows. Columns: 4 columns.

An 8x8 SRAM (Static Random Access Memory) consists of 64 memory cells organized in an 8-row by 8-column matrix. Each cell stores 1 bit of data, and it provides more storage capacity compared to smaller SRAMs like 2x2 or 4x4, making it suitable for more complex memory applications. Let's break down the structure, operation, and key concepts involved in an 8x8 SRAM.
Structure and Architecture: Number of Cells: An 8x8 SRAM has 64 SRAM cells. Each cell stores 1 bit of data. The memory is divided into rows and columns: Rows: 8 rows. Columns: 8 columns.

3) 16X64 SRAM: A 16x64 SRAM (Static Random Access Memory) is a memory architecture consisting of 16 rows and 64 columns, resulting in 1024 SRAM cells. Each cell stores 1 bit of data. This structure allows for a larger storage capacity compared to smaller SRAMs like 8x8 or 4x4, making it suitable for applications that require a significant amount of memory space. Let's explore the structure, operation, and key concepts involved in a 16x64 SRAM.
Structure and Architecture:
Number of Cells: A 16x64 SRAM contains 1024 SRAM cells .Each cell stores 1 bit of data .The memory is divided into rows and columns: Rows: 16 rows Columns: 64 columns.
by usin these all we have to construct the 64x16 SRAM in the cadance software.

IV. PROJECT

A. Decoder

In the below we can see the decoder circuit diagram by using the AND gates and also we can see the symbol of the decoder . This circuit is from the cadence software and it is 2x4 decoder.

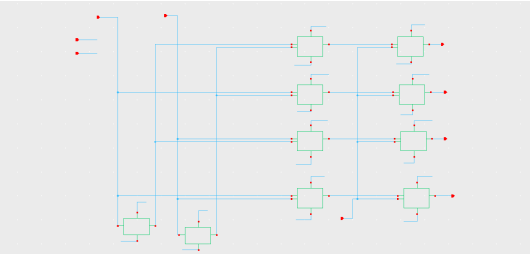

Fig. 13. The 2x4 decoder

in the below we can this the symbol of the 2x4 decoder . And also the test circuit and the outputs of the 2x4 decoder.

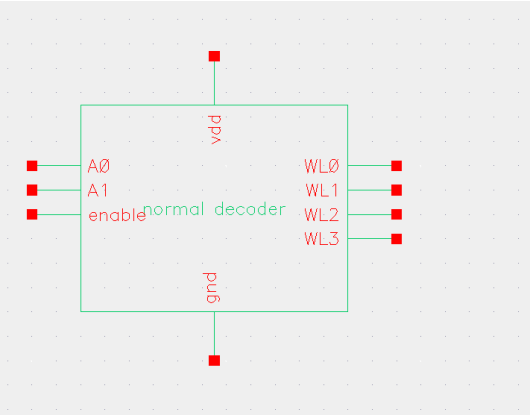

Fig. 14. The 2x4 decoder symbol

Row decoders are used to select word lines. In this project , we have made 8x256 NAND based decoder.Nand based decoder is used to achieve low power and lesser area requirements.Low power→ less leakage power.

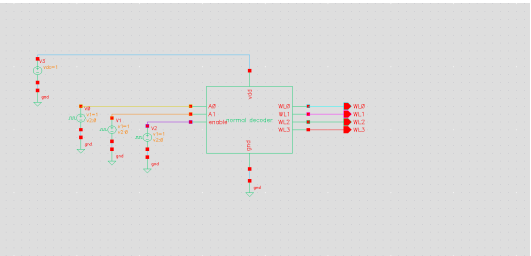

Fig. 15. The 2x4 decoder test circuit

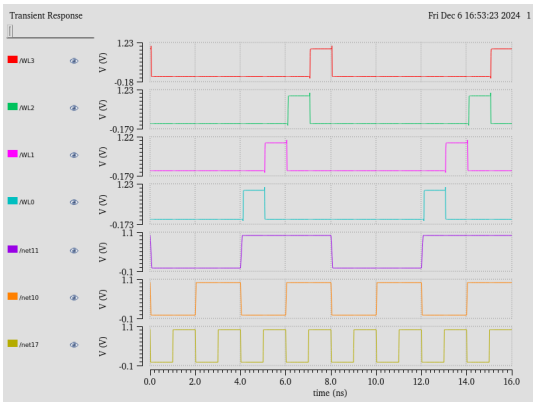

Fig. 16. output of the 2x4 decoder

In the above we are considering the static decoder. but we are using the 4x16 decoder. for decoding the column decoder.

B. DYNAMIC DECODER

for this 16x64 SRAM project we are using the dynamic type decoder. In the below we can see the basic structure of the Dynamic decoder (2x4)

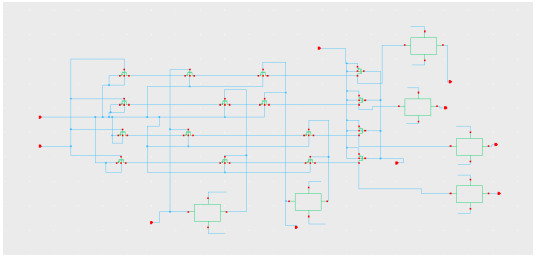

Fig. 17. The 2x4 dynamic decoder

for construction of the 6x64 decoder we are using both static and dynamic decoder for that we should construct the 2x4 basic decoder.

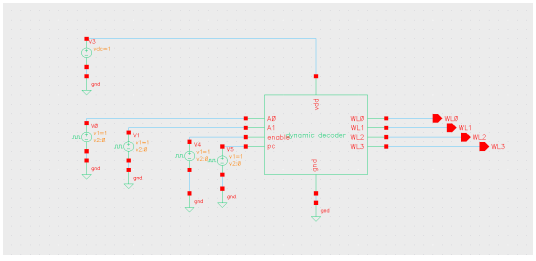

Fig. 18. The 2x4 dynamic decoder test circuit

for the construction of the dynamic decoder we are usin the and gates and in the above figure we can see that .

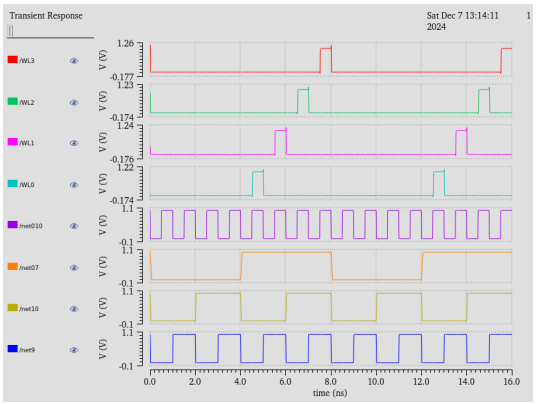

Fig. 19. output of the dynamic decoder

C. 4x16 Decoder

from the 2x4 decoder we are constructing 4x16 decoder using both dynamic decoder and static decoder. and the we are using the 4x16 decoder for both column and row decoder in last circuit.

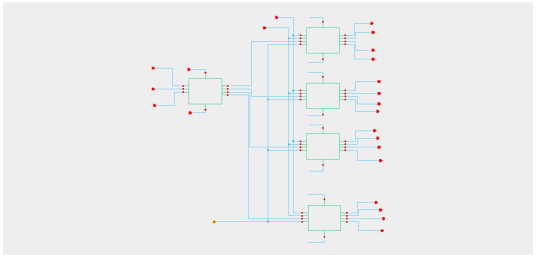

Fig. 20. 4x16 circuit

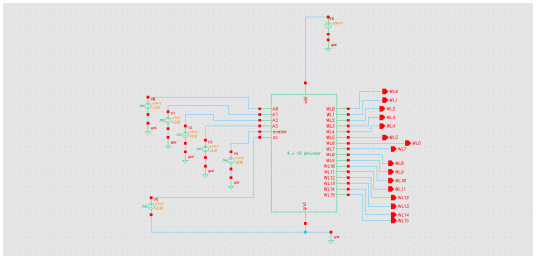

Fig. 21. 4x16 symbol

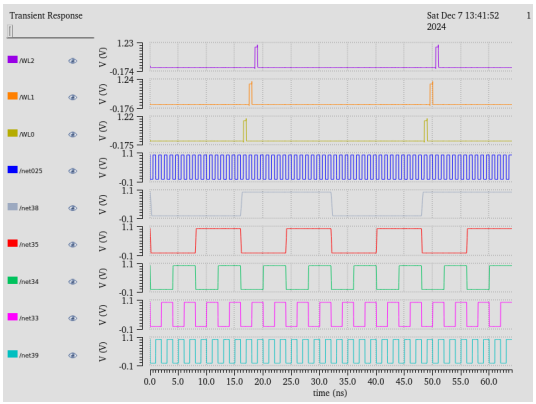

Fig. 22. 4x16 output

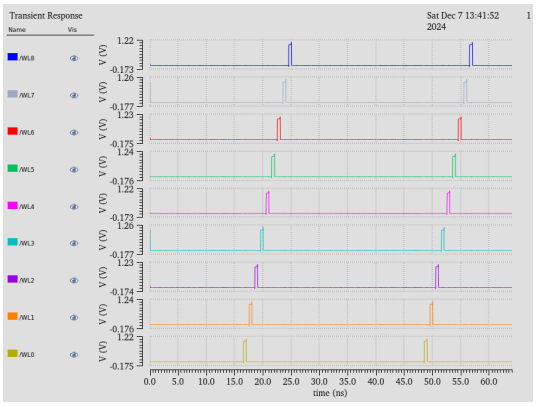

Fig. 23. 4x16 output

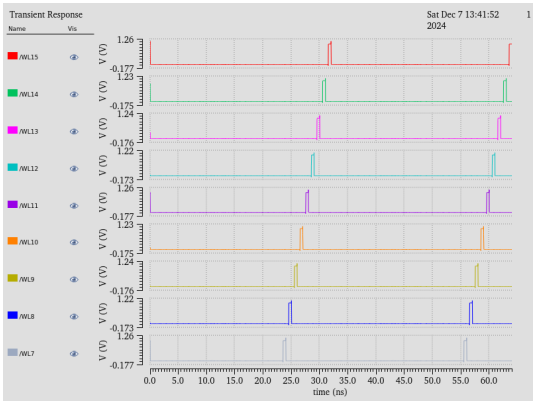

Fig. 24. 4x16 output

D. 6x64 decoder

we are using the same decoder as the row decoder and in the last circuit . for the we are using the 6 bit input.
in the 6x64 bit the we are using the both static and dynamic decoder.this is the main circuit in the 64x16 bit SRAM.

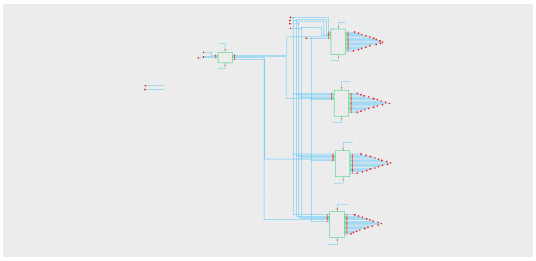

Fig. 25. 6x64 decoder

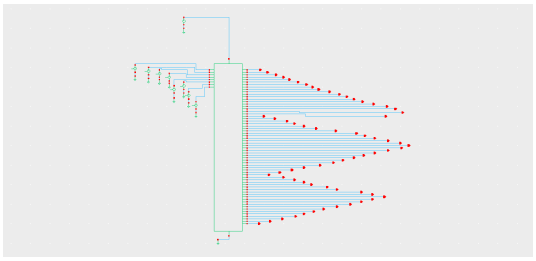

Fig. 26. 6x64 decoder symbol

A 6x64 decoder in SRAM converts a 6-bit binary input into one of 64 unique outputs to select a specific row or column in the memory array. It ensures that only one line is activated at a time for read or write operations, enabling efficient addressing in the memory. This decoder uses logic gates for translation, balancing speed and power efficiency, and is a crucial component for compact and high-speed SRAM functionality.

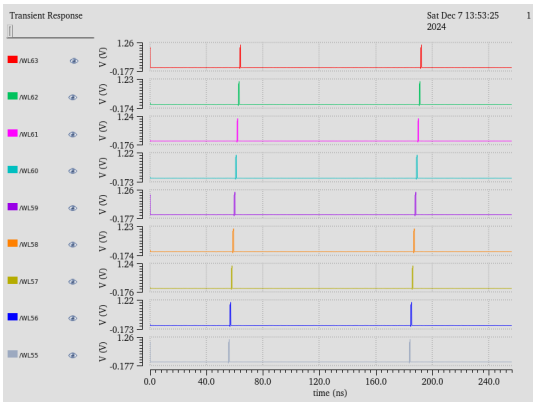

Fig. 27. 6x64 decoder output

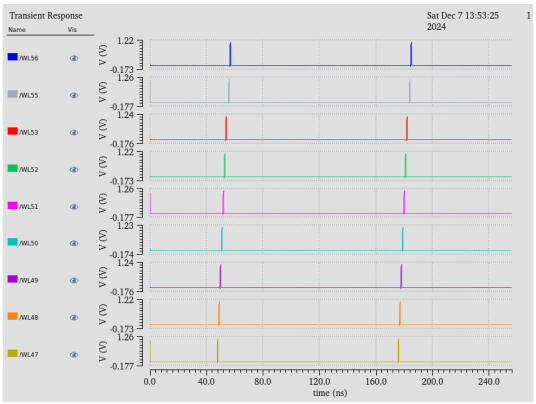

Fig. 28. 6x64 decoder output

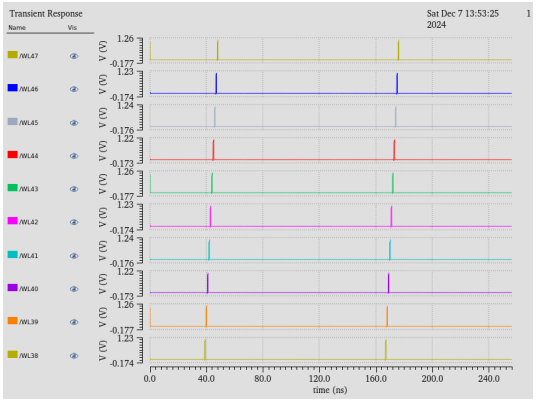

Fig. 29. 6x64 decoder output

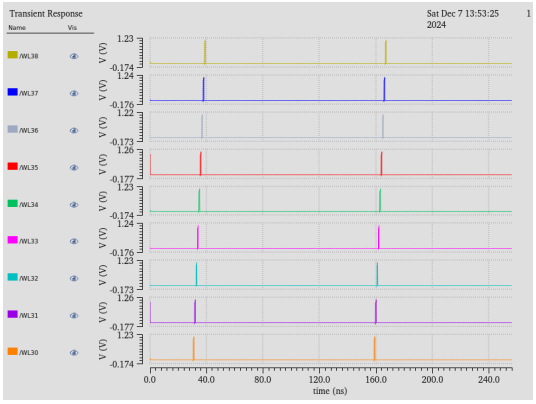

Fig. 30. 6x64 decoder output

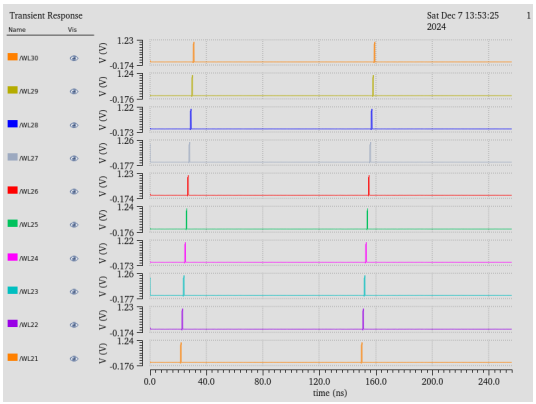

Fig. 31. 6x64 decoder output

E. SRAM

The SRAM unit cell is the basic building block of Static Random Access Memory, typically designed using six transistors (6T). It consists of two cross-coupled inverters forming a bistable latch for data storage and two access transistors for read and write operations, controlled by the word line.

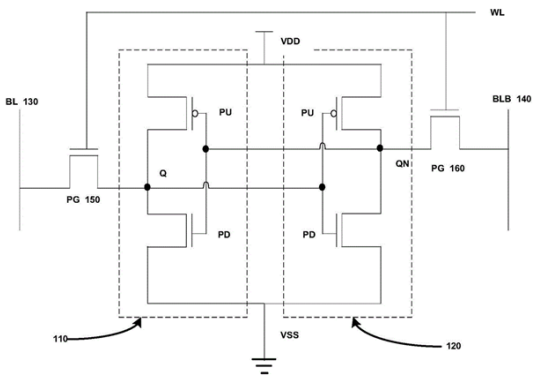

Fig. 32. SRAM UNIT CELL

During write operations, data is driven onto the bit lines and stored in the latch, while during read operations, the latch's value is sensed via the bit lines. The unit cell provides high speed and stable data retention without the need for refresh cycles, though it consumes continuous power to maintain the stored state. This design is ideal for applications requiring fast and reliable memory, such as cache in processors.

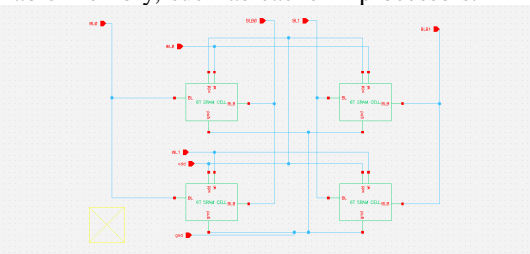

Fig. 33. SRAM 2X2

A 2x2 SRAM is a small memory array with 4 memory cells, organized into 2 rows and 2 columns. It consists of SRAM unit cells, row decoders to select one of the 2 rows, column decoders to access specific columns, and control circuitry to manage read and write operations. Each cell can store 1 bit of data, enabling a total storage capacity of 4 bits. Bit lines and word lines facilitate data access, while sense amplifiers and precharge circuits ensure fast and reliable operation. The 2x2 configuration is a basic representation of larger SRAM arrays, used for educational or demonstration purposes.

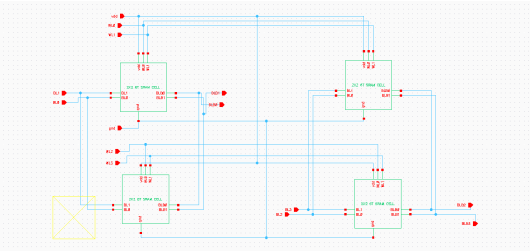

Fig. 34. SRAM 4X4

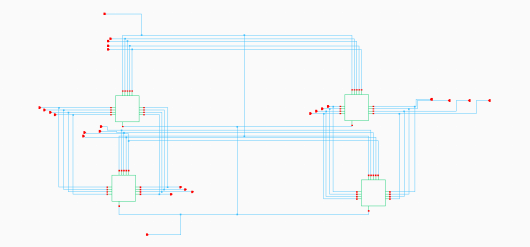

Fig. 35. SRAM 8X8

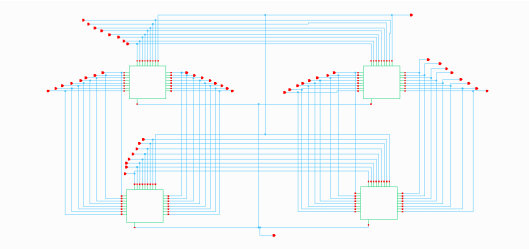

Fig. 36. SRAM 16X16

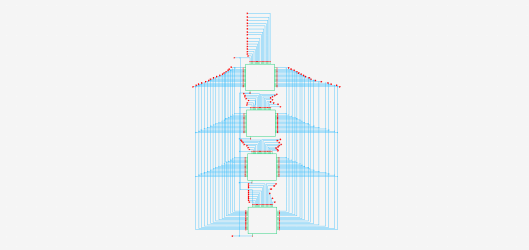

Fig. 37. SRAM 16X64

F. write circuit

The write circuit in SRAM facilitates writing data into memory cells. It works by controlling the bit lines and word line to store a desired value (0 or 1) in the selected cell. When a write operation is initiated, the write enable (WE) signal activates, and the bit lines are driven to the appropriate logic levels based on the input data. The word line is asserted to turn on the access transistors, allowing the bit lines to overwrite the existing data in the cell's cross-coupled latch. The write circuit ensures efficient and reliable data transfer to the memory cells during operation.

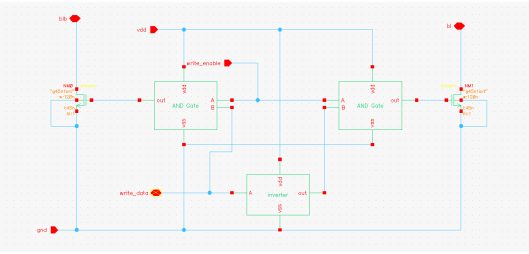

Fig. 38. write circuit

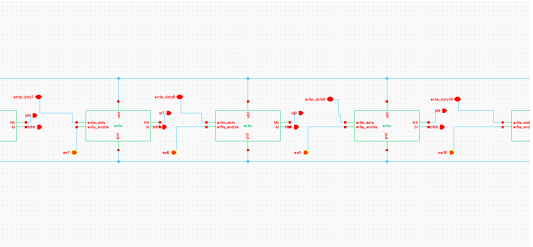

Fig. 39. write circuit 16 bit

A 16-bit write circuit in SRAM enables writing 16 bits of data simultaneously into memory cells. It uses write drivers to set the bit lines (BL and BL') according to the input data, a word line to activate the target row, and a write enable (WE) signal to initiate the operation. The address decoder selects the appropriate row, and the write drivers overwrite the memory cells with the new data via the bit lines. After the write, the bit lines are precharged for future operations. This circuit ensures efficient and simultaneous data transfer to 16 cells.

G. sense circuit

A sense amplifier in SRAM is used to detect and amplify the weak signal read from the memory cell to a level that can be processed by the system. It quickly responds to small voltage differences between the bit lines during a read operation, effectively converting the stored 0 or 1 into a readable digital signal. The sense amplifier improves read access time and ensures data integrity by enhancing the weak signal from the memory cell to a stronger, stable output.

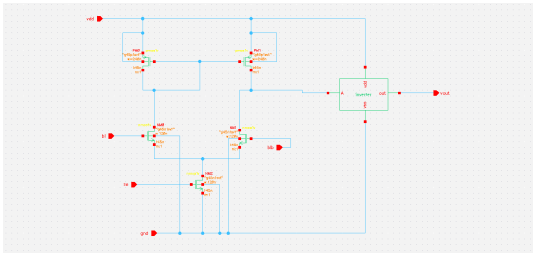

Fig. 40. sense circuit

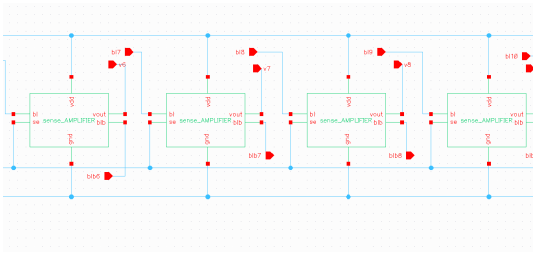

Fig. 41. sense circuit 16 bit

H. pre-charge circuit

A precharge circuit in SRAM prepares the memory array for the next read or write operation by ensuring the bit lines are ready. It precharges the bit lines to a known logic level (0 or 1) before a read or write operation begins. This process helps stabilize the voltage levels on the bit lines, allowing for accurate data transfer. The precharge circuit ensures optimal performance by minimizing signal degradation and interference, which is crucial for maintaining data integrity and high-speed operation in SRAM.

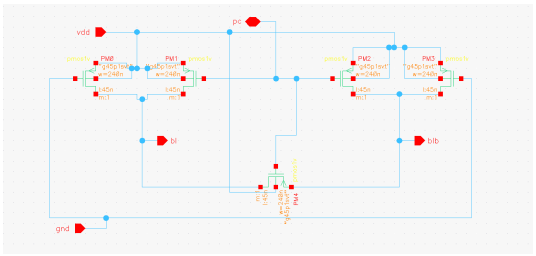

Fig. 42. pre charge circuit 16 bit

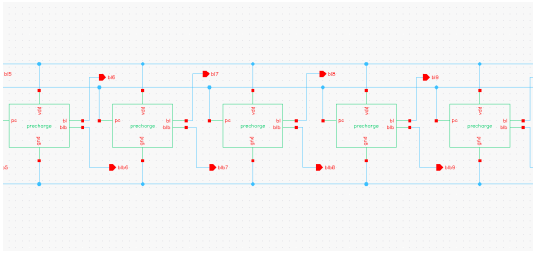

Fig. 43. pre charge circuit 16 bit

V. 64x16 SRAM

A 64x16 SRAM is a memory array with 64 rows and 16 columns, providing a total storage capacity of 1024 bits (128 bytes). Each cell stores one bit of data. The array uses row and column decoders to select specific rows and columns for read or write operations. The control circuitry manages the timing and synchronization of these operations, while sense amplifiers read data from selected cells. Bit lines carry data signals, and word lines activate the corresponding rows. This configuration is commonly used in applications requiring moderate capacity and fast data access, such as cache memory in microprocessors and embedded systems.

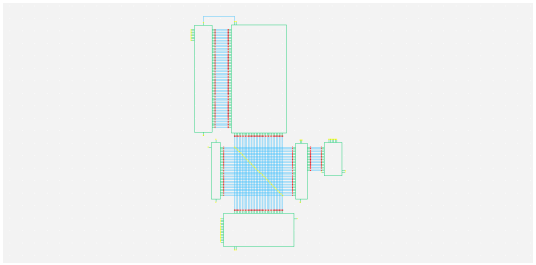

Fig. 44. final circuit

in the below we can see the write operation of the SRAM and output of the write operation.

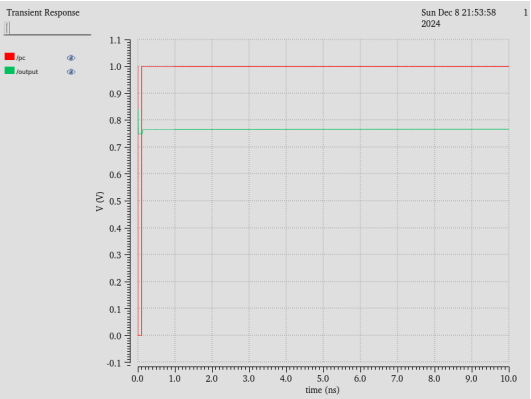

Fig. 45. final circuit output

VI. CONCLUSION

Working with a 64x16 SRAM in Cadence provided valuable insights into SRAM design and simulation. By accurately modeling the memory array, we were able to obtain the correct results, demonstrating the functionality and performance of the SRAM. The simulation helped verify the SRAM's operation, including read and write cycles, signal integrity, and timing characteristics. This successful implementation validates the design approach and confirms that the SRAM meets the desired specifications for fast data access and reliability.