

DFT

JTAG

Introduction

What is DFT ?

DFT stands for Design For Testability

Ability of Primary input to set a particular value @ any particular internal node.

- DFT is a stage in IC design of adding test logics to a design which gives maximum controllability and observability.
- It doesn't modify or add any functional logic.
- Once IC is fabricated in the foundry, it is prone to many manufacturing faults.
- DFT patterns help to identify those faulty parts.
- 3 types of DFT patterns
 - BSCAN patterns - (Boundary Scan)
 - ATPG patterns – (Automatic Test Pattern Generation)
 - MBIST patterns – (Memory Built In Self Test)

Similarly, observability is nothing but the ability of the primary output and inputs to observe any particular value at any particular internal nodes in the design.

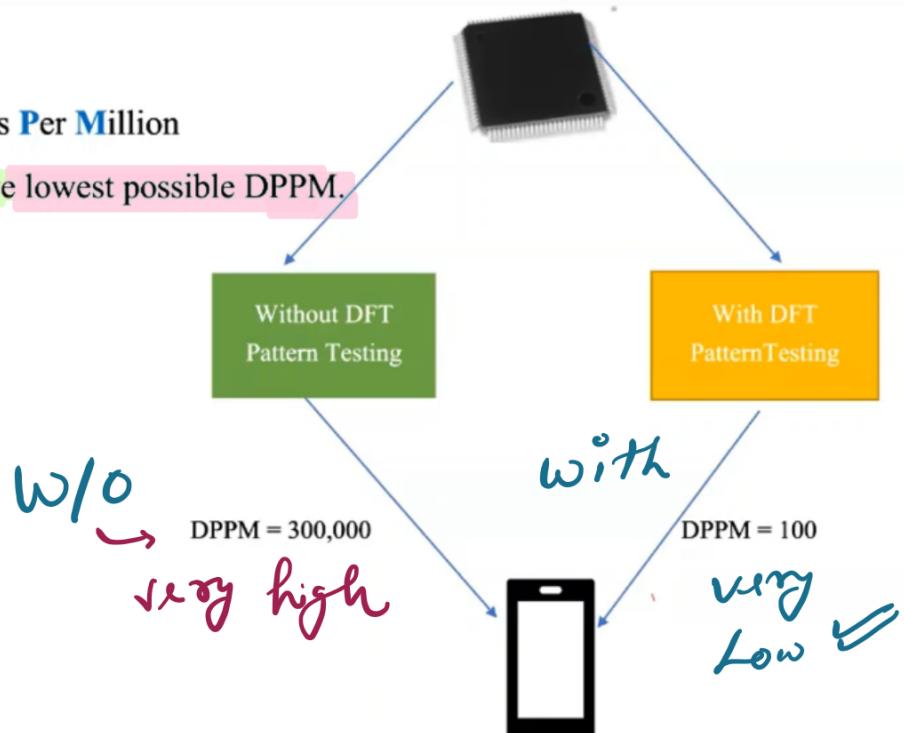
What is DPPM?

- DPPM stands for Defective Parts Per Million

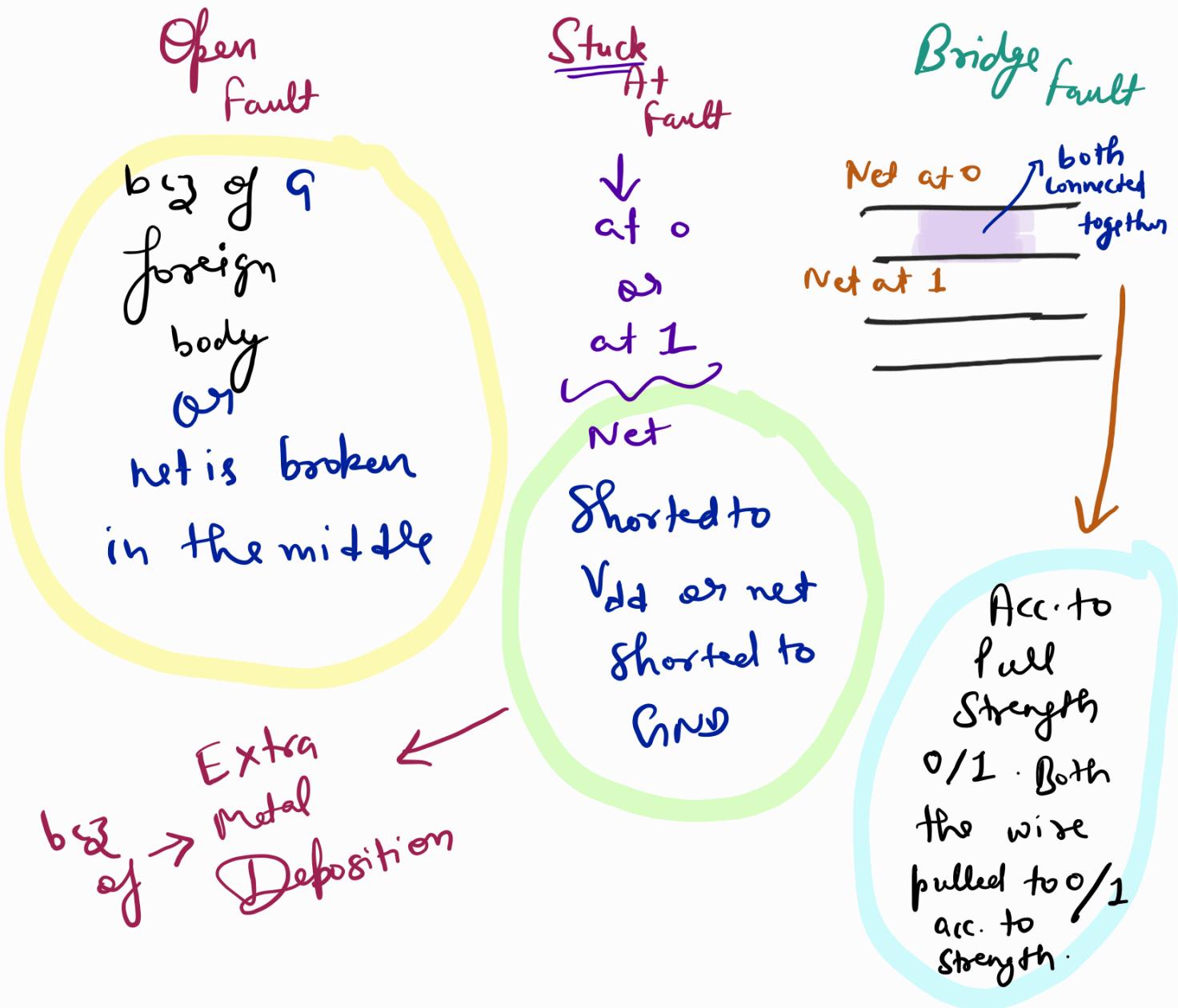
Primary goal of DFT is to achieve lowest possible DPPM.

For Ex:

$$\text{Foundry Yield Loss} = 30\%$$



manufacturing faults
Silicon defects formed during IC fabrication



JTAG

JTAG

JTAG stands for Joint Test Action Group

for what?

- Industry standard for verifying designs on printed circuit boards after manufacture.
- JTAG formulated certain protocols and introduced an IEEE 1149.1 standard in 1990.
- Test logic to test the components within itself or the interconnections between the components.
- IEEE 1149.1 introduces TAP (Test Access Port), Boundary Scan cell and TDR (Test Data Register).

Conceptual Architecture of a Chip

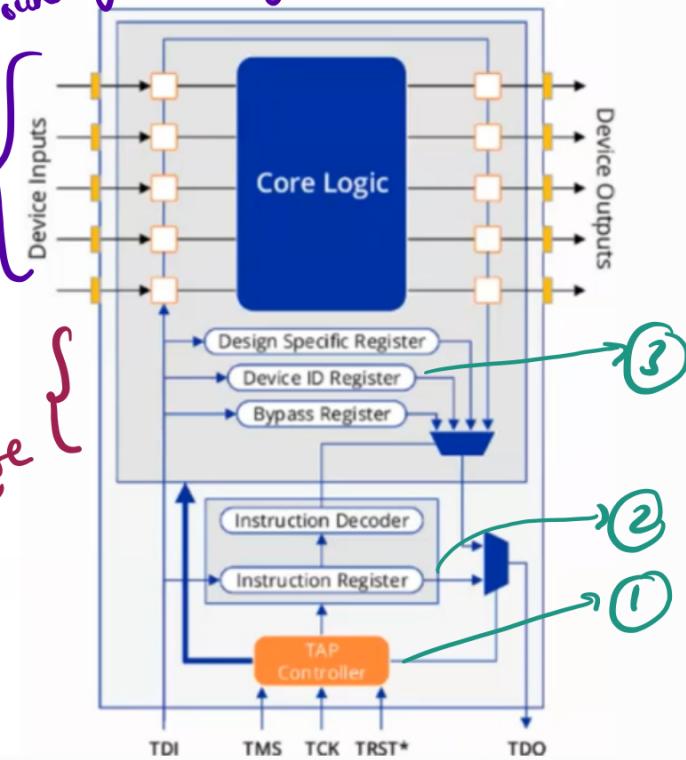
It has 5 major components

1. TAP controller (TAP FSM)
2. Instruction Register
3. Data Registers
4. Data Mux
5. TDO Mux

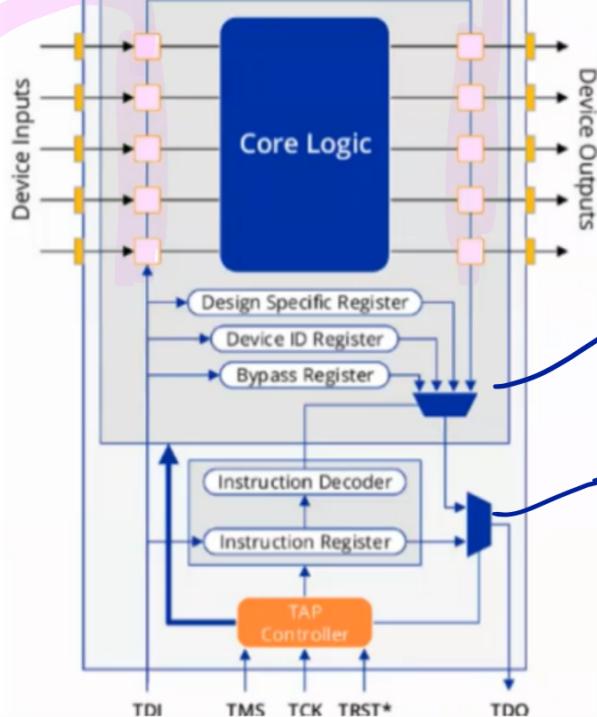
TAP Controller Generates following 6 signals

- | | |
|-------------|-------------------------|
| 1. ClockIR | To Instruction Register |
| 2. ShiftIR | |
| 3. UpdateIR | |
| 4. ClockDR | To Data Registers |
| 5. ShiftDR | |
| 6. UpdateDR | |

Boundary Scan Register



These All are Boundary Scan cells



TAP is Test Access Port

4 types of Data Registers :

① Boundary Scan Register:

Serial Shift Register consists of Boundary Scan Cells.

② Bypass register:

1 bit reg. used to pass test sig from a chip when it is not involved in current test operation

③ Device-ID Register:

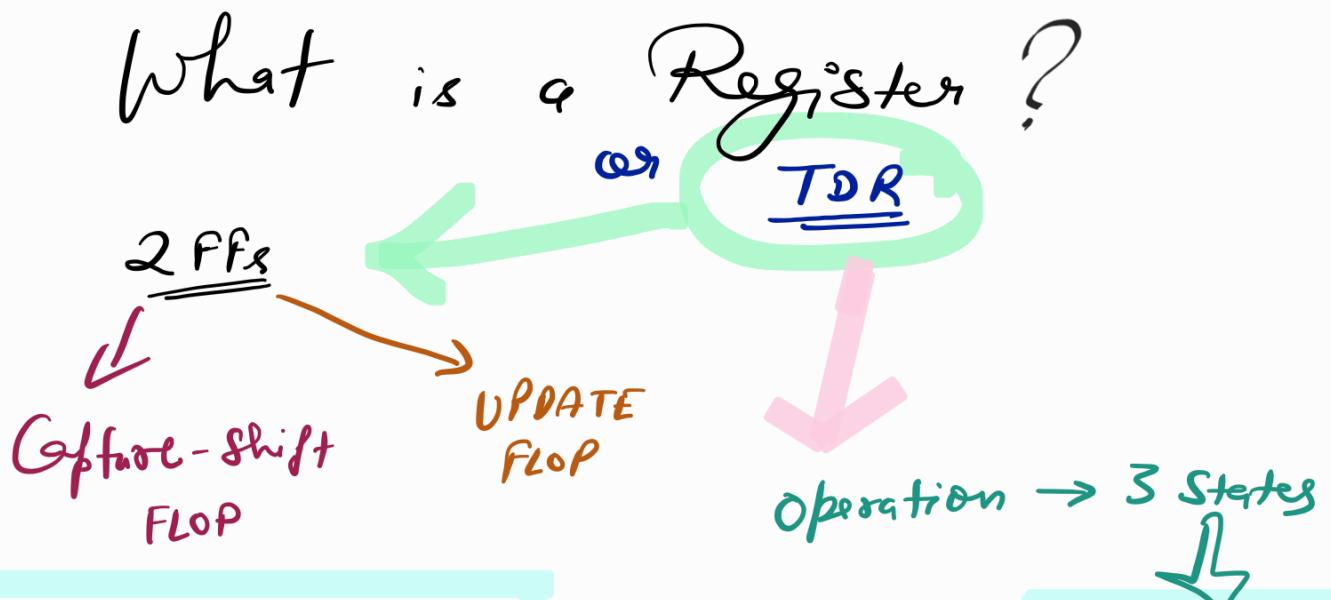
Contains Product information

User Defined Reg. →

④ Design Specific Registers:

for other purposes like test configuration, ATPG, BIST etc.

Optional Registers are also known as TDR



PI: Primary

I/P

SI: Shift

"

PO: — -

O/P

SO: — -

"

&
all
other
States

Capture State
Shift State
Update State

STATES	A	B	C
Capture	pulse	0	1
Shift	pulse	1	0
Update	0	0	pulse *
All other states	0	0	0

Diagram below:

Understandings from the Table:

for Capture & Shift: $\text{Clk} \rightarrow \text{Pulse}$
they themselves $\rightarrow 1$
(TDR's)

For Update: $\text{Clk} \rightarrow 0$; Update TDR itself $\rightarrow \text{PULSE}$

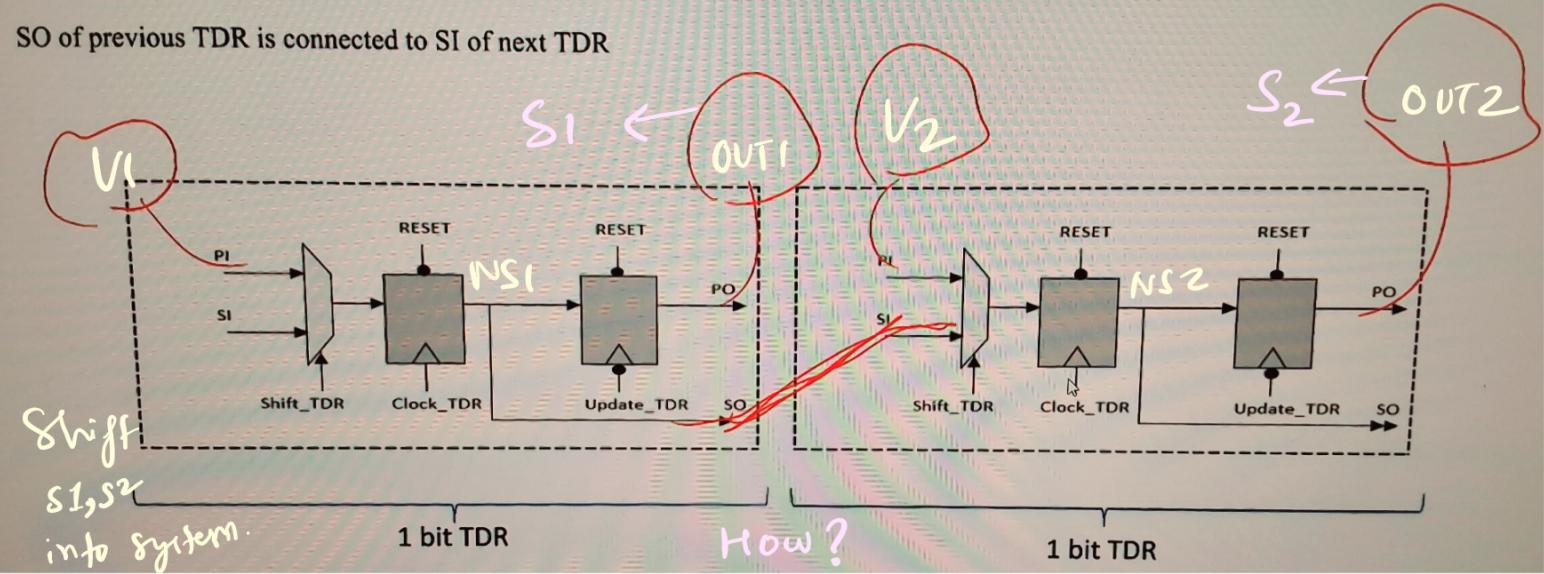
Test Data Reg. (Multi-bit)

Multi-bit TDR is formed two 1-bit --

So, SO of previous TDR is SI for next TDR.
True or Not?

How Read / write Operation happens by using 3 States?

SO of previous TDR is connected to SI of next TDR



During Capture State:

$$\text{Shift-TDR} = 0$$

$$\text{Update-TDR} = \text{No CLK}$$

$$\text{Clock-TDR} = \text{Pulse}$$

V_1 is captured in N_{S1} next stages
 $\& V_2$ is --- N_{S2}

During Shift State:

Apply S_2 in SI of first TDR.

$$\text{Shift-TDR} = 1$$

$$\text{Update-TDR} = \text{No CLK}$$

We can already observe V_2 in SO.

Now give $\rightarrow \text{Clock-TDR} = \text{Pulse}$

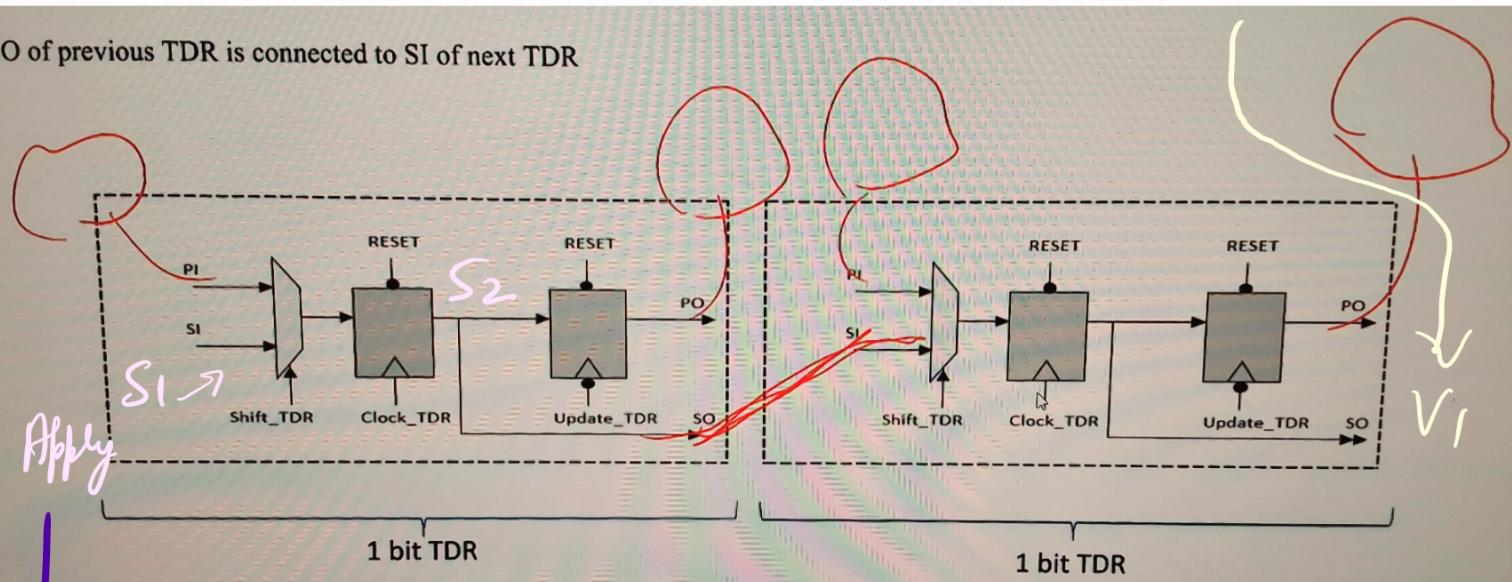
V_1 from N_{S1} comes to N_{S2}

S_2 from IIP side of SI go to N_{S1}

This is after the 1 pulse of Shift State.

Now, we can observe $v_1 \downarrow$

SO of previous TDR is connected to SI of next TDR

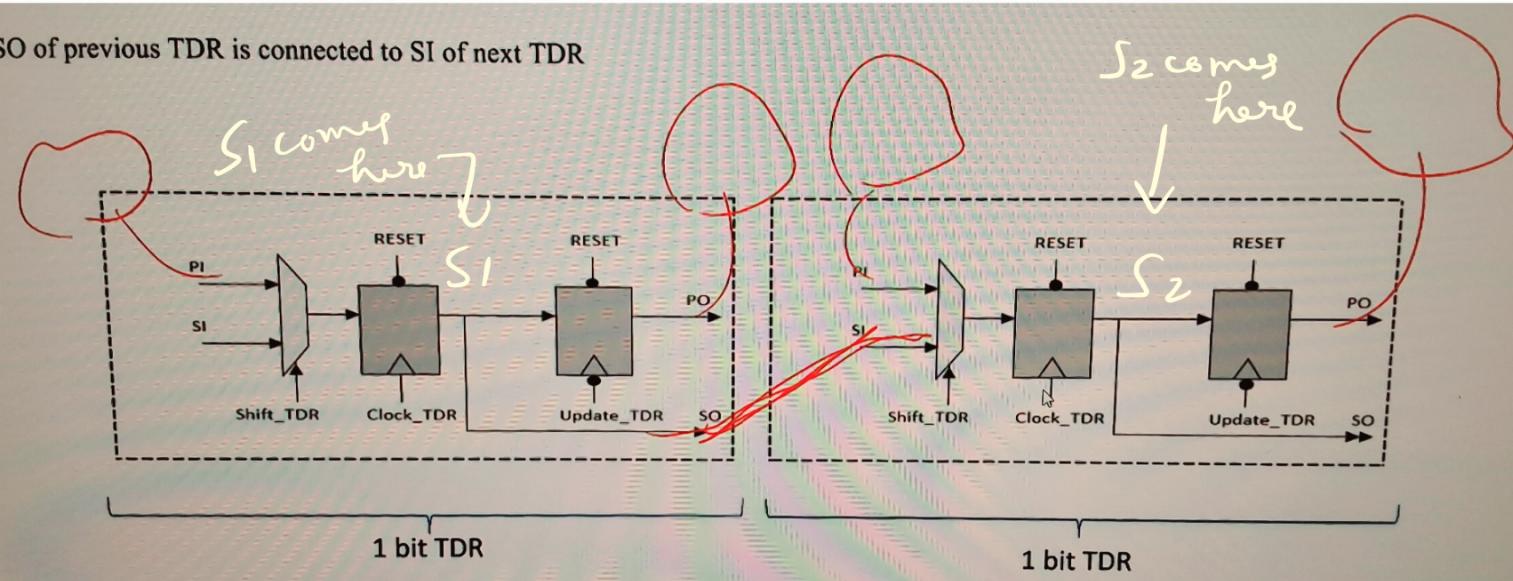


Both v_1 & v_2 can be read now.

give
clock-TOR
pulse
 \downarrow
so $\neg J$

END of Shift Phase.

SO of previous TDR is connected to SI of next TDR



UPDATE PHASE: $Shift - TOR = 0$

$$\text{Clock - TPR} = 0$$

$$\text{UPDATE-TBR} = \sum \text{pulse}$$

