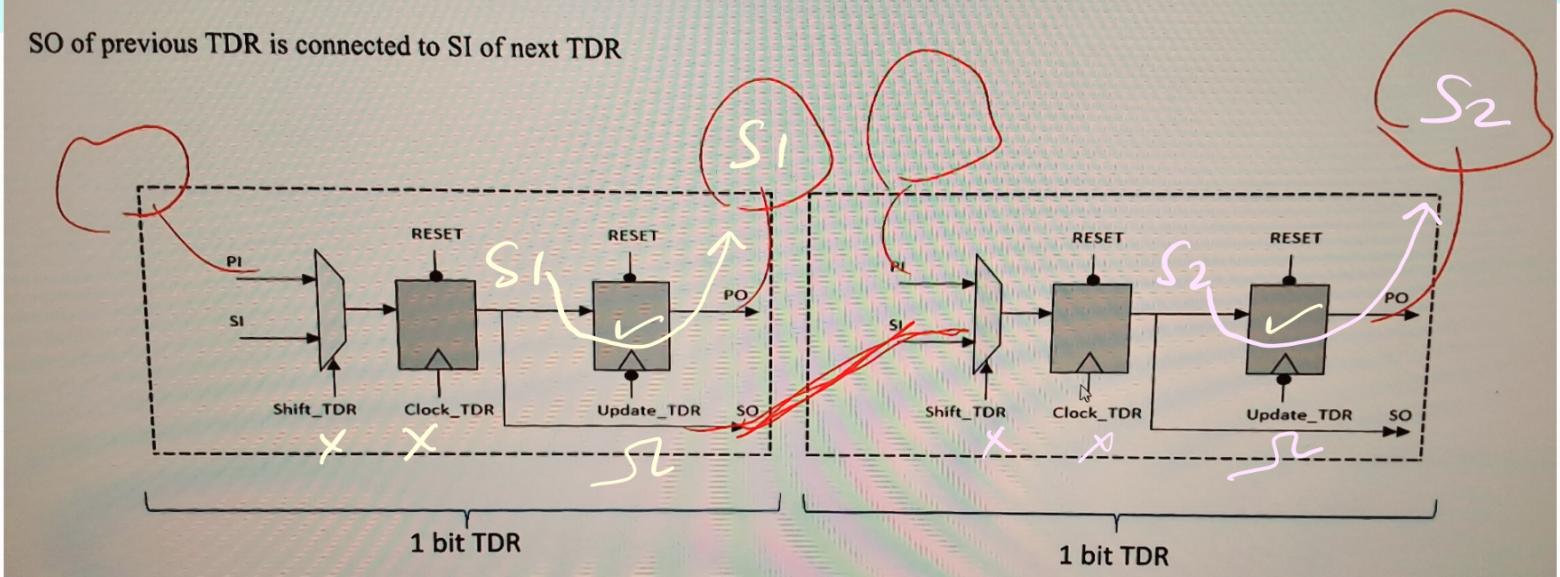


SO of previous TDR is connected to SI of next TDR



WRITE TASK Completed

To send --- / write -- S1/S2 from/into System.  
We've to give two pulses of clock in Shift-TDR State

# its two sets of two pulses.

One set:



Another set:



Formulate: How many no. of Single bit FLOPs in a TDR  
that many no. of shift Signals are needed  
to successfully do a Read/Write Opr.

3 Types:

3-bit Write Only

3-bit Read Only

{No update FLOP}

3-bit  
Read-write  
Read Only  
Write only

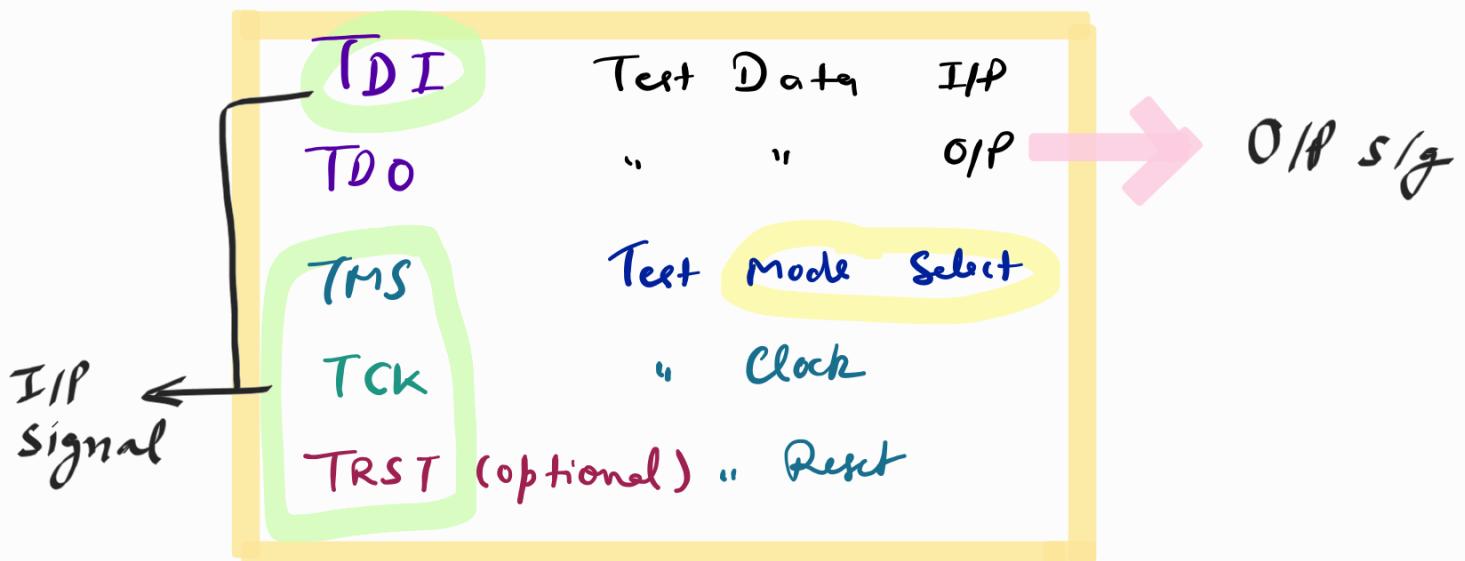
IEEE

1149.1  
Standard

TAP (Test Access Port)

On-chip  
FSM  
Logic

Interfaces with external world  
with 5 Signals

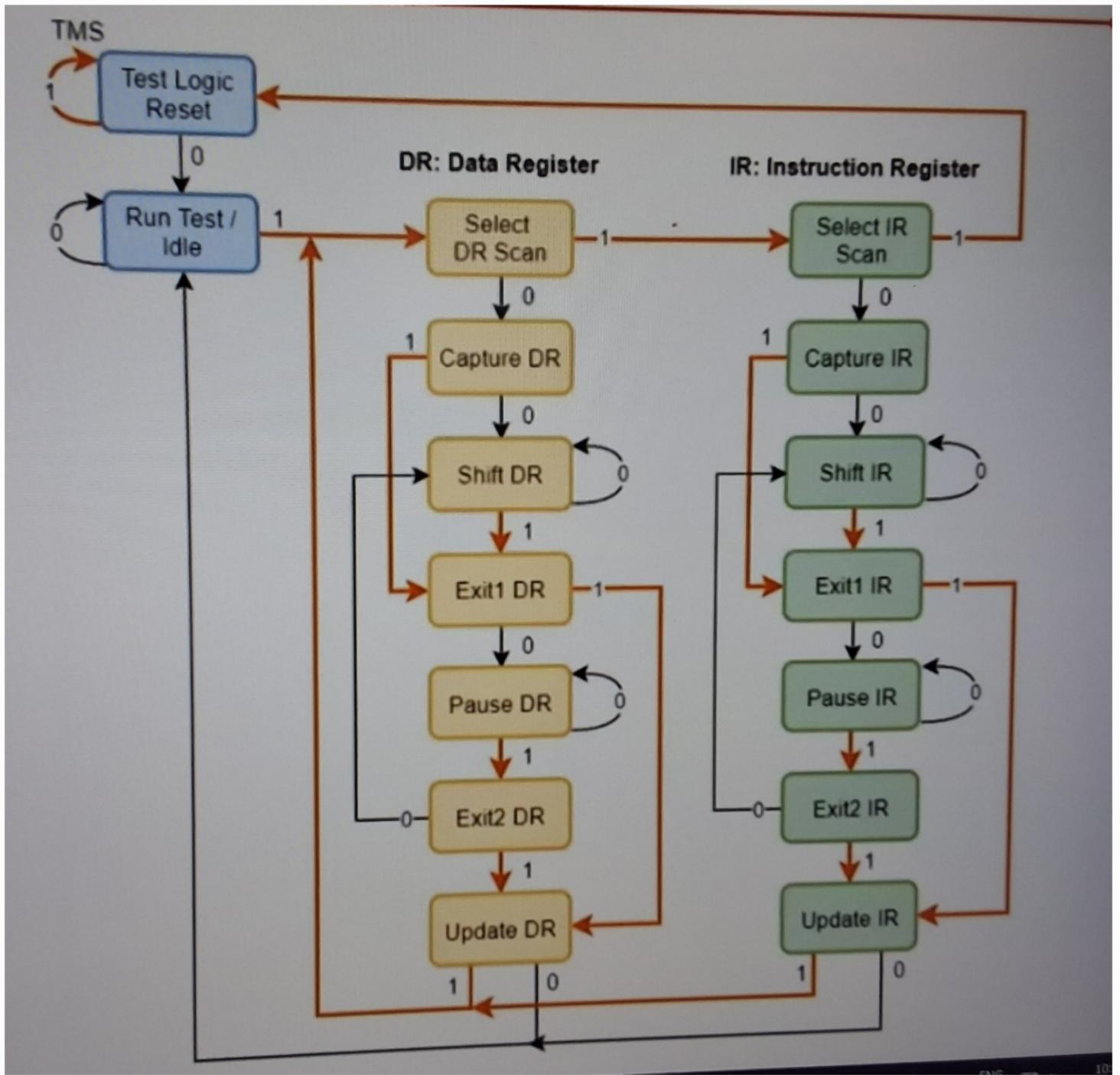


# TAP FSM State Machine:

# Total 16 States:

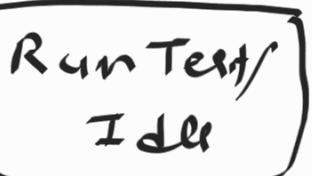
- At every posedge of TCK, the FSM will move from one state to another state depending on TMS signal.
- The signal on the arrow is TMS. \* → Test Mode Select
- Hold TMS = 1 for 5 cycles to return to Test-Logic-Reset from any other state.
- Hence TRST is an optional signal.
- TDO is driven by negedge of TCK

} grp



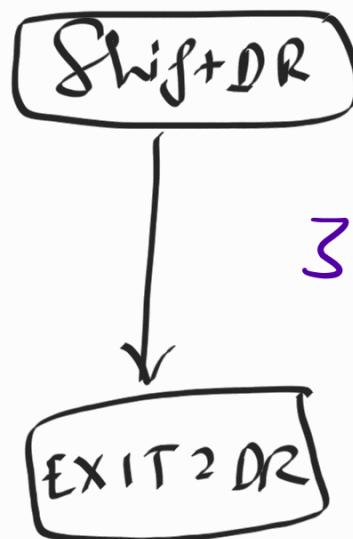
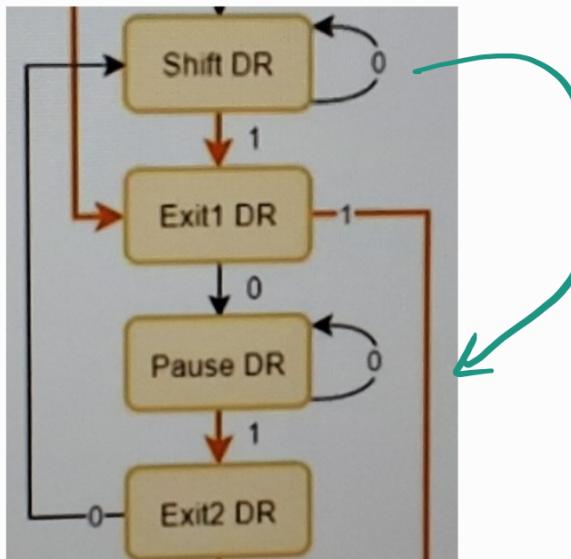
Hold TMS=0 for 1 Clk Cycle

To move from



state

Similarly



3 cycles needed

For a 4 bit **DR** → it takes nine cycles  
**IR** → 10  
 For what?

to read/write into the Register from the run test/Idle state.

Two Mode Concepts

DR & IR  
 Scan operations

Min TCK cycles so that TMS should be held HIGH

So, that the TAP FSM

from any other State

↳ can make a transition into  
 'Test Logic Reset'

5 ✓