

Boundary

SCAN

a

Cell

b

Instructions

⑨ IEEE 1149.1 introduces a Boundary Scan cell.

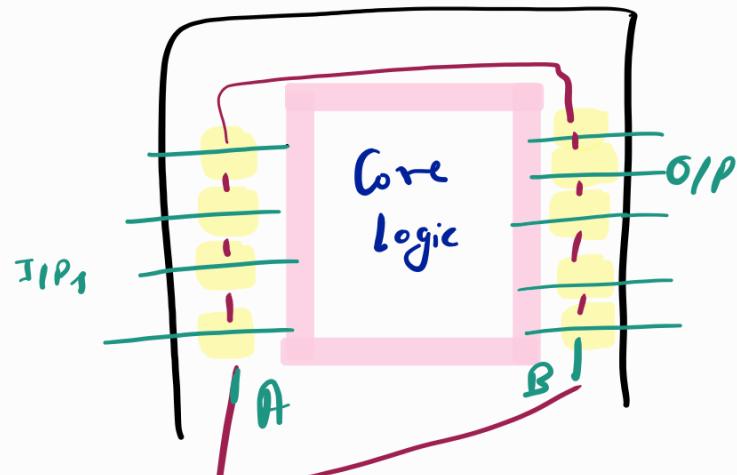
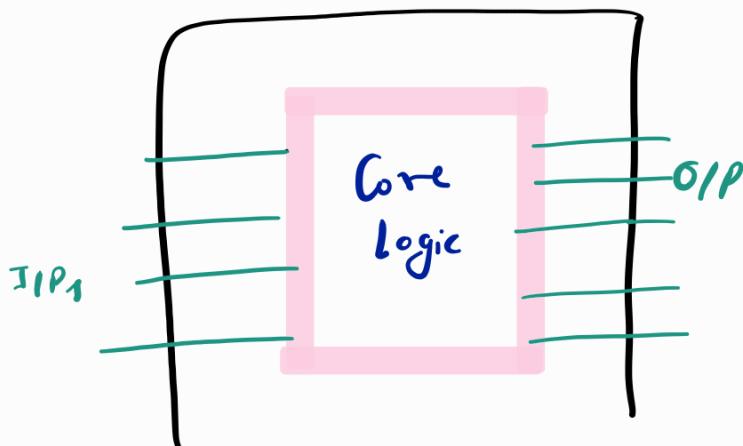
Allowing Testing of a chip external circuitry  
& Interconnects

Inserted into design w/o affecting its  
functional Logic

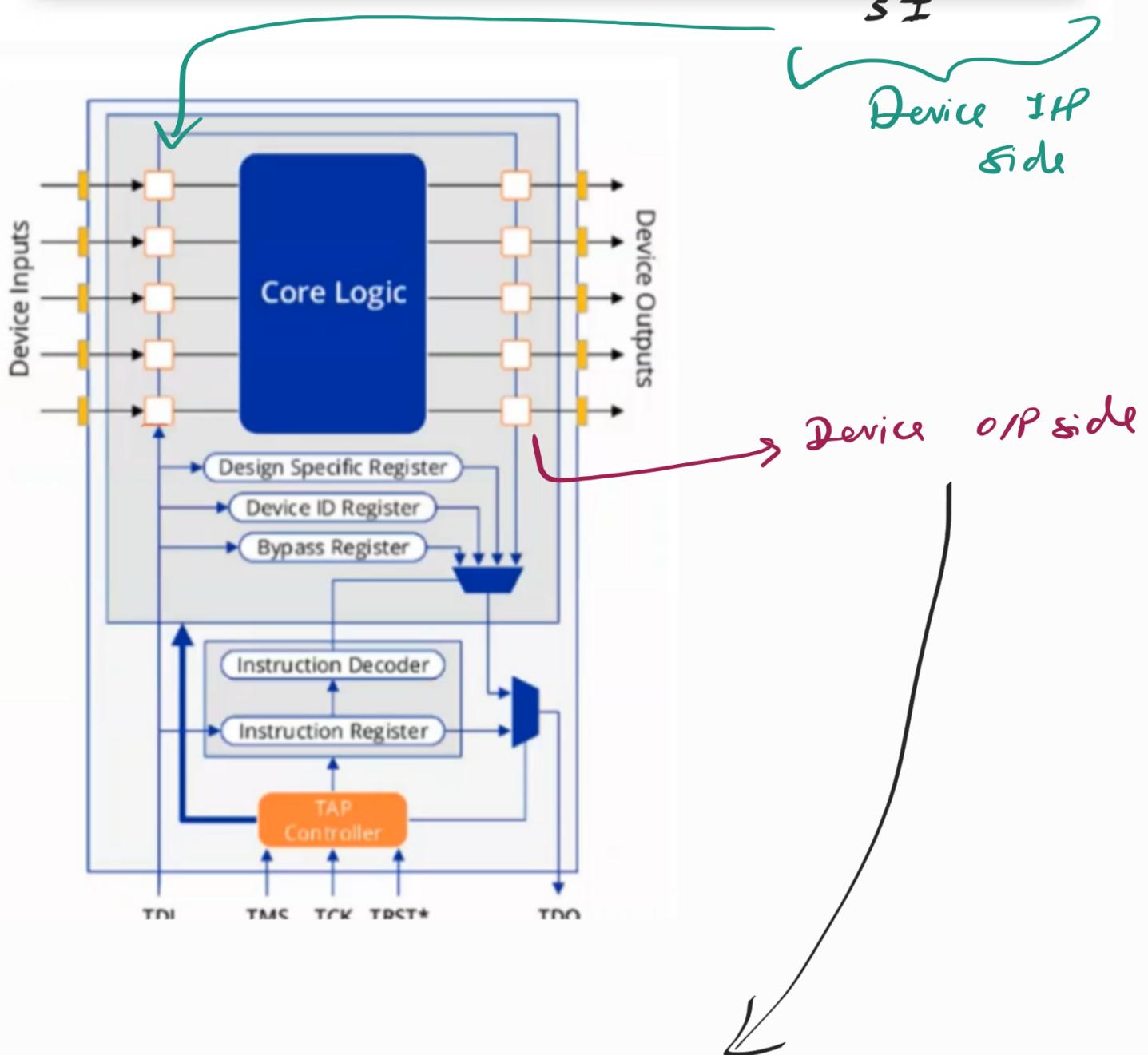
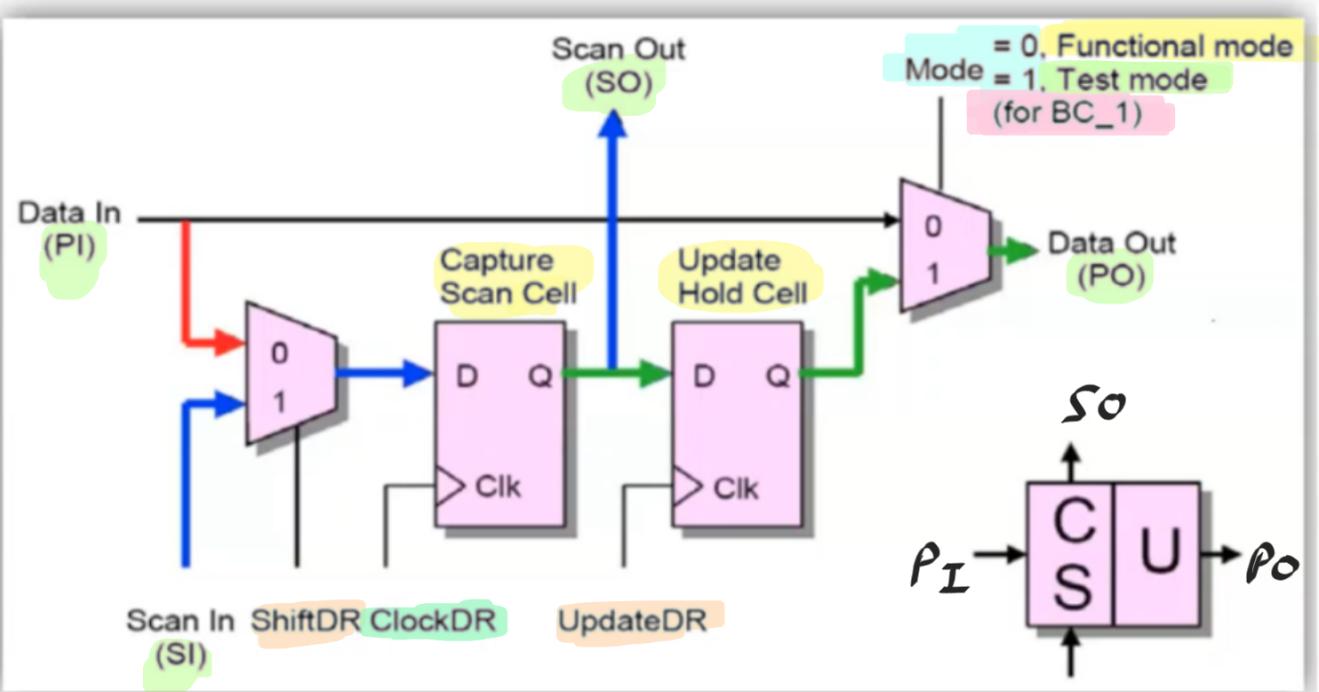
All BSC are connected in Serial buse  
T0I & TDO

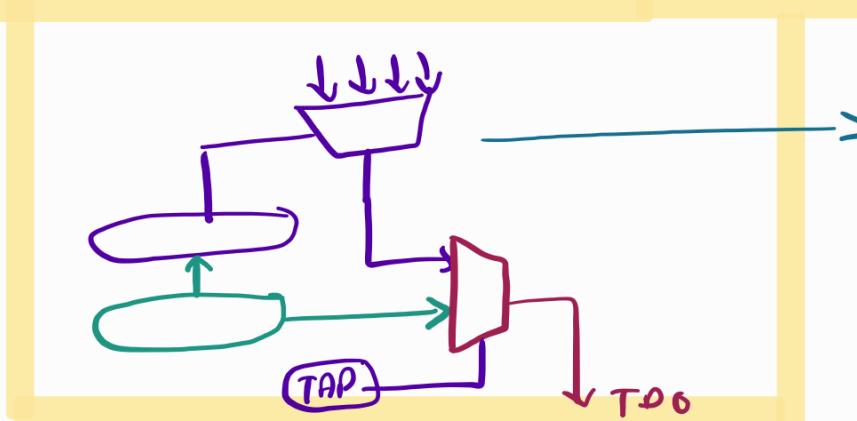
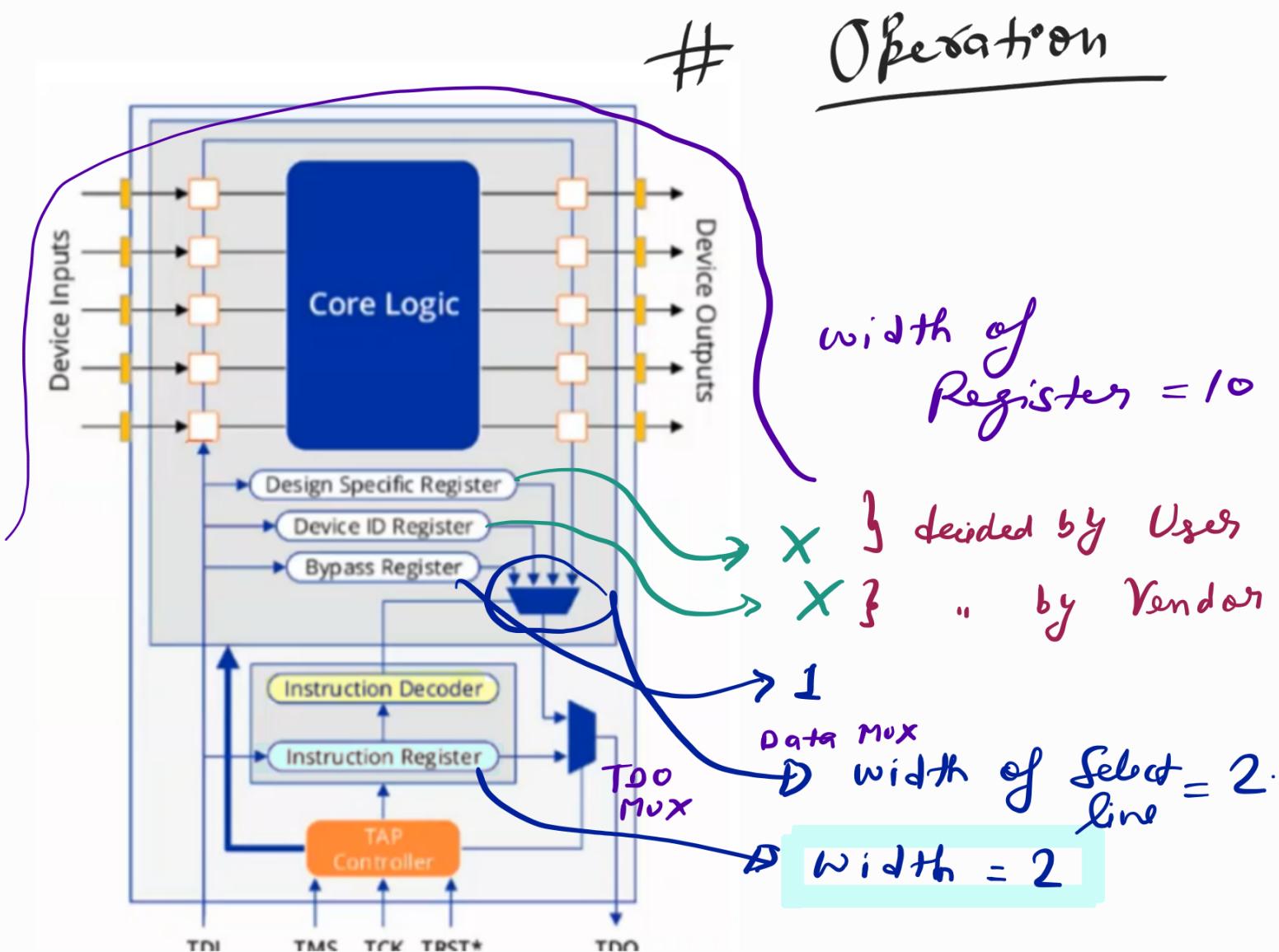
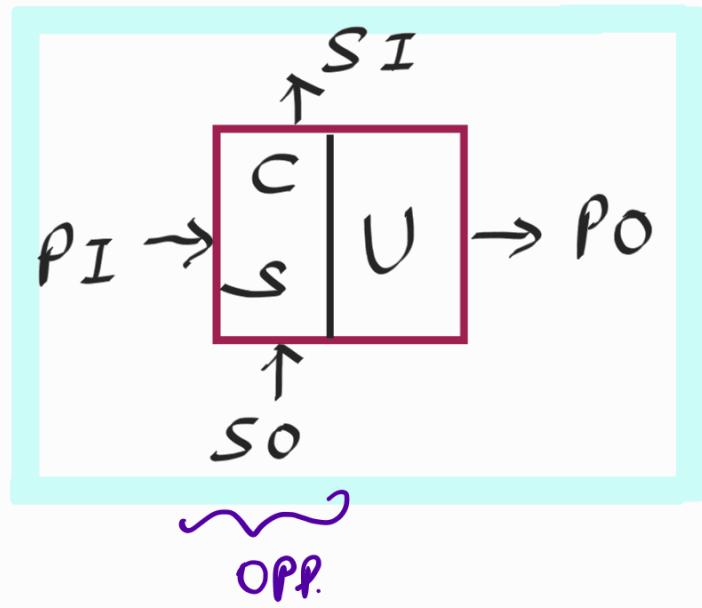
Allows → test data to be serially fed into  
the Chip.

→ S/R Interconnects to be tested  
separately from Components.



Serially ← Stiched together ← Boundary Scan cell





Registers

00	Boundary Scan
01	Design Specific
10	Device ID
11	Bypass Reg ..

If we write 00 into the instruction Register

Now things depends on TAP Controller.

$$TRST = 1$$



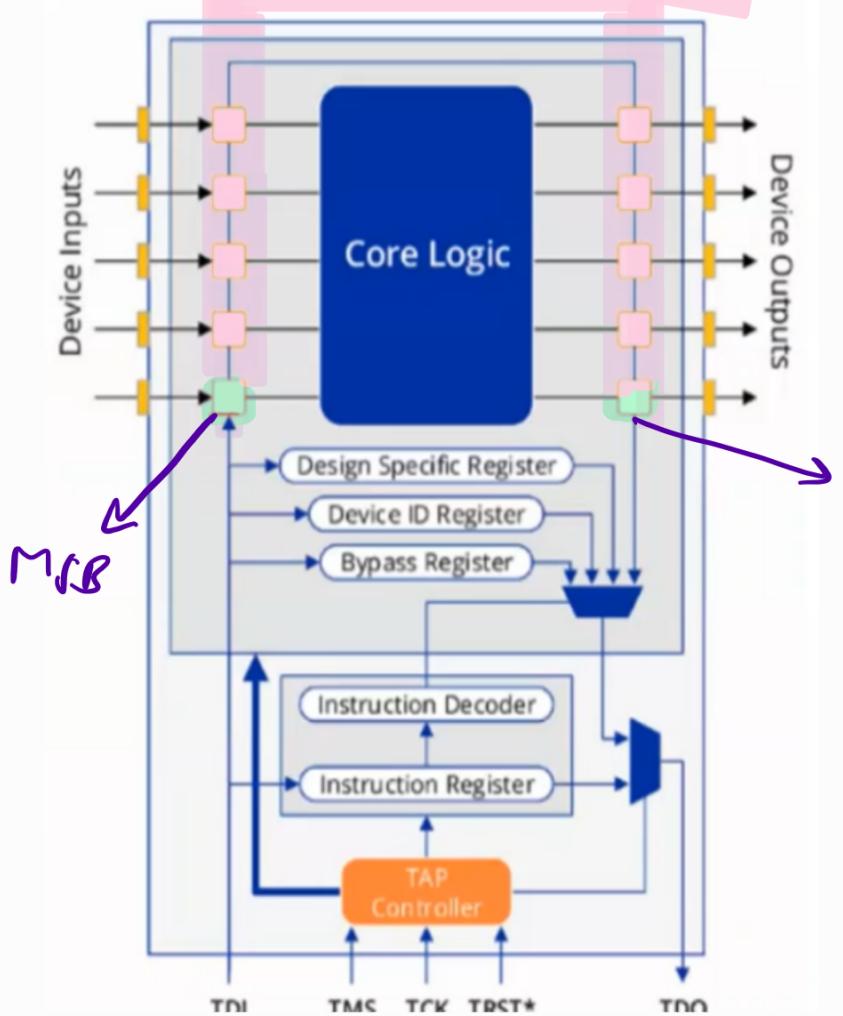
$$IR \text{ Scan} = 00$$



DR Scan operation

= 1010101010  
10 bits

All 10 bits will come here

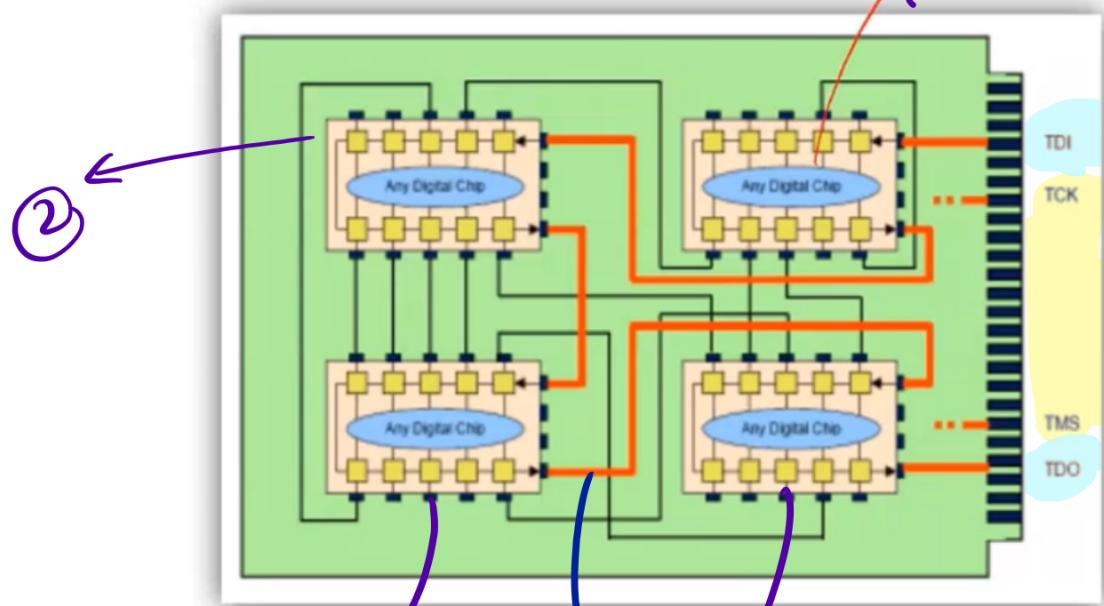


This is how TAP FSM is Operated in order to write a value into the boundary scan register.

To test interconnection b/w IC's on

# Why Boundary Scan and JTAG?

TAP connection within & between IC's in a Printed Circuit Board (PCB).



TCK &  
TMS

are  
broadcast  
to all  
IC's

but TDI &

TDO

are connected in a  
Serial chain fashion.

like this  
in Red arrows

you can see

Serial Connections.

? Daisy Chain  
Fashion

Boundary Scan cell architecture is shown in the diagram.

It has 4 modes of operation:

1. Normal mode :

Mode = 0;

Data Out = Data In



2. Shift mode :

ShiftDR = 1

Pulse ClockDR

Scan In → Scan Out;

3. Capture mode :

ShiftDR = 0;

Pulse ClockDR;

DataIn → Scan Out;

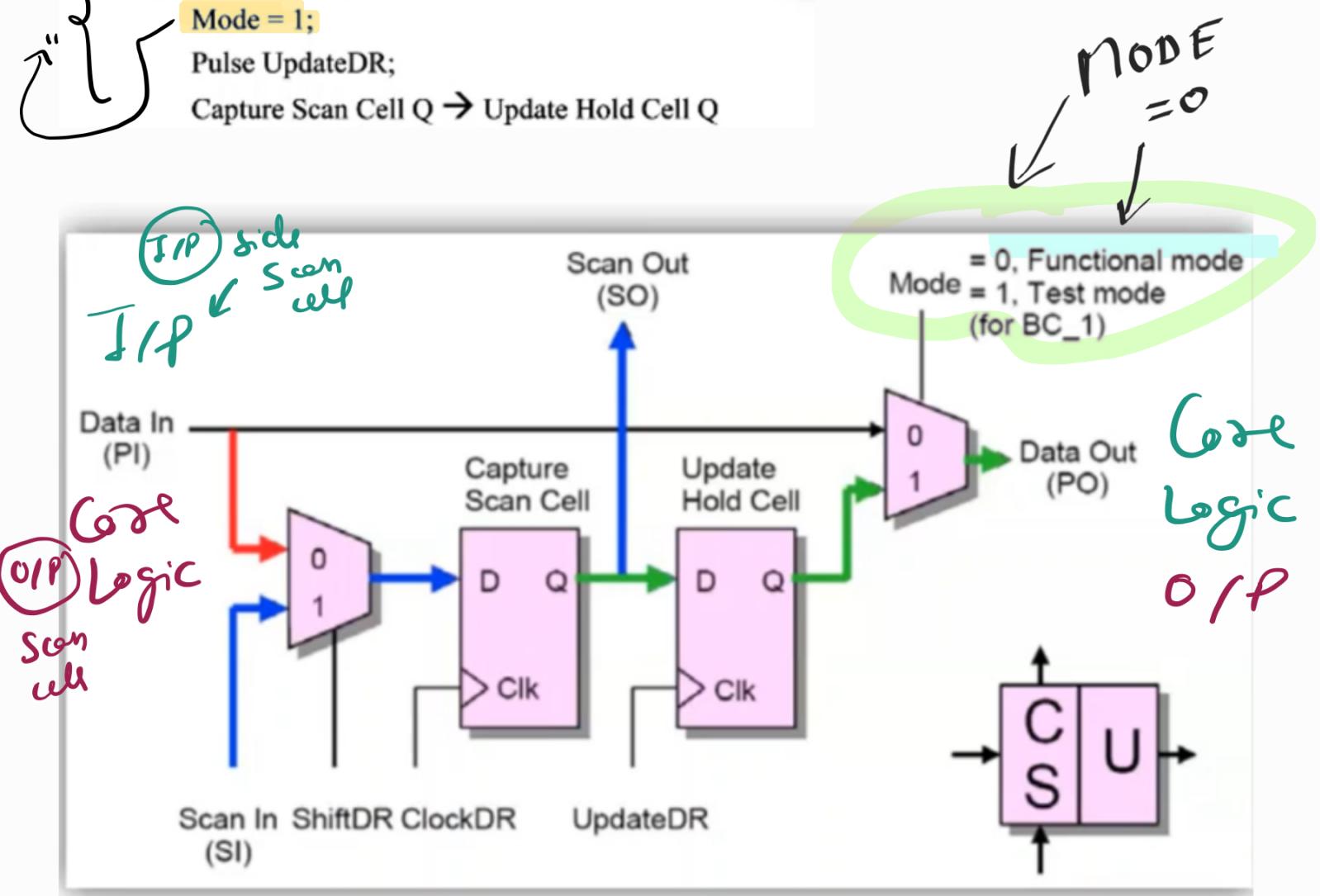
4. Update mode :

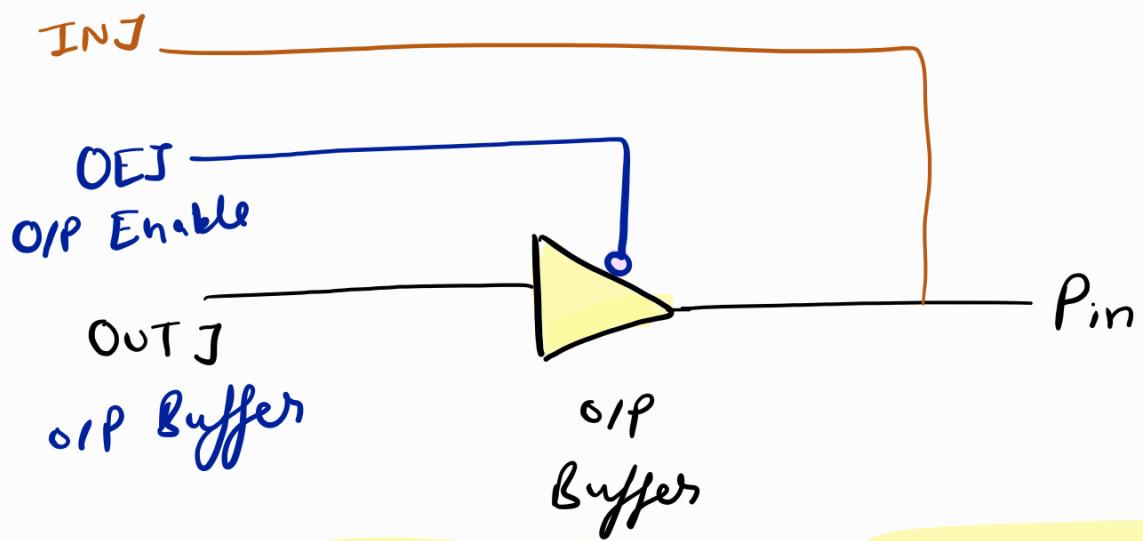
Mode = 1;

Pulse UpdateDR;

Capture Scan Cell Q → Update Hold Cell Q

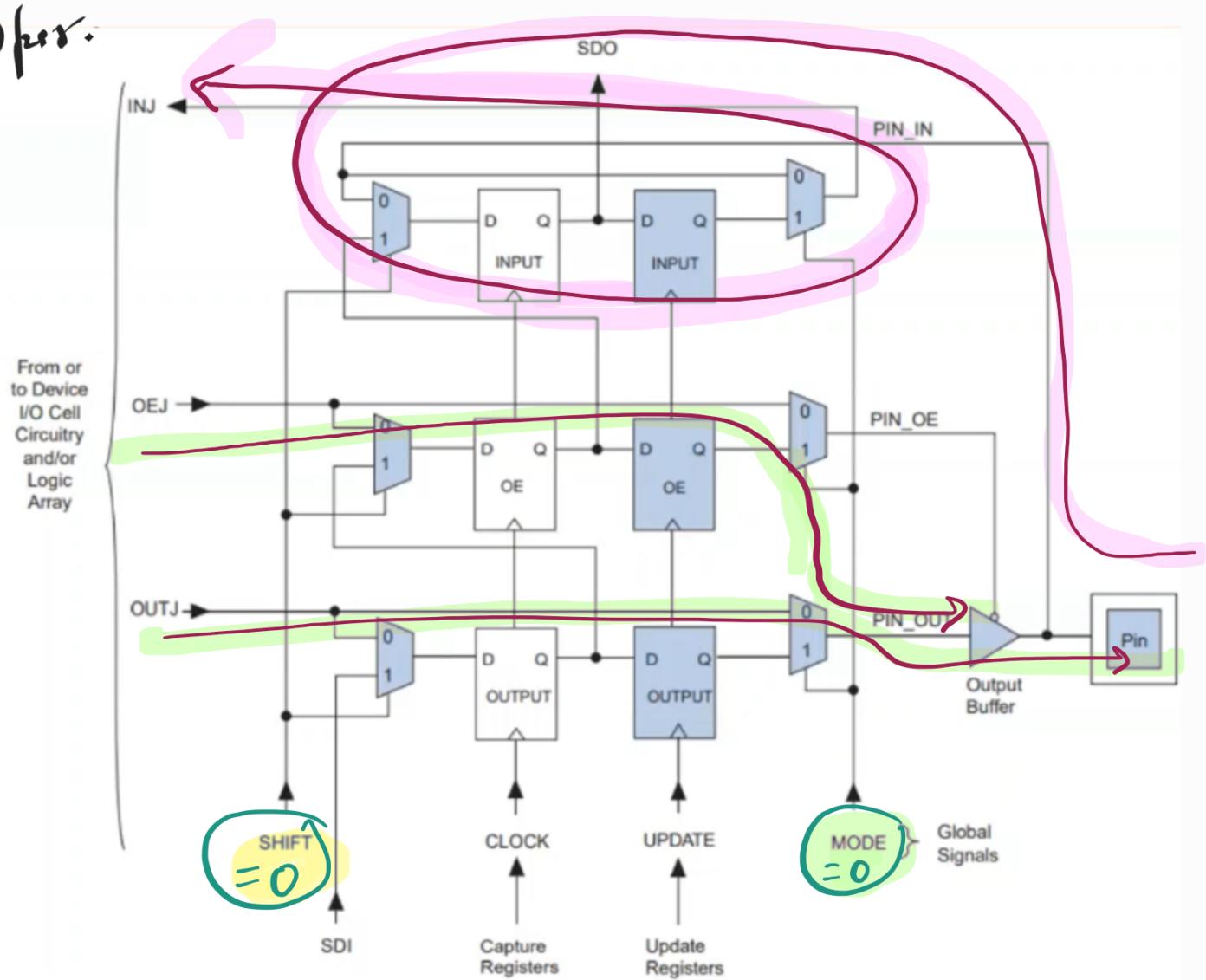
Previously  
Studied



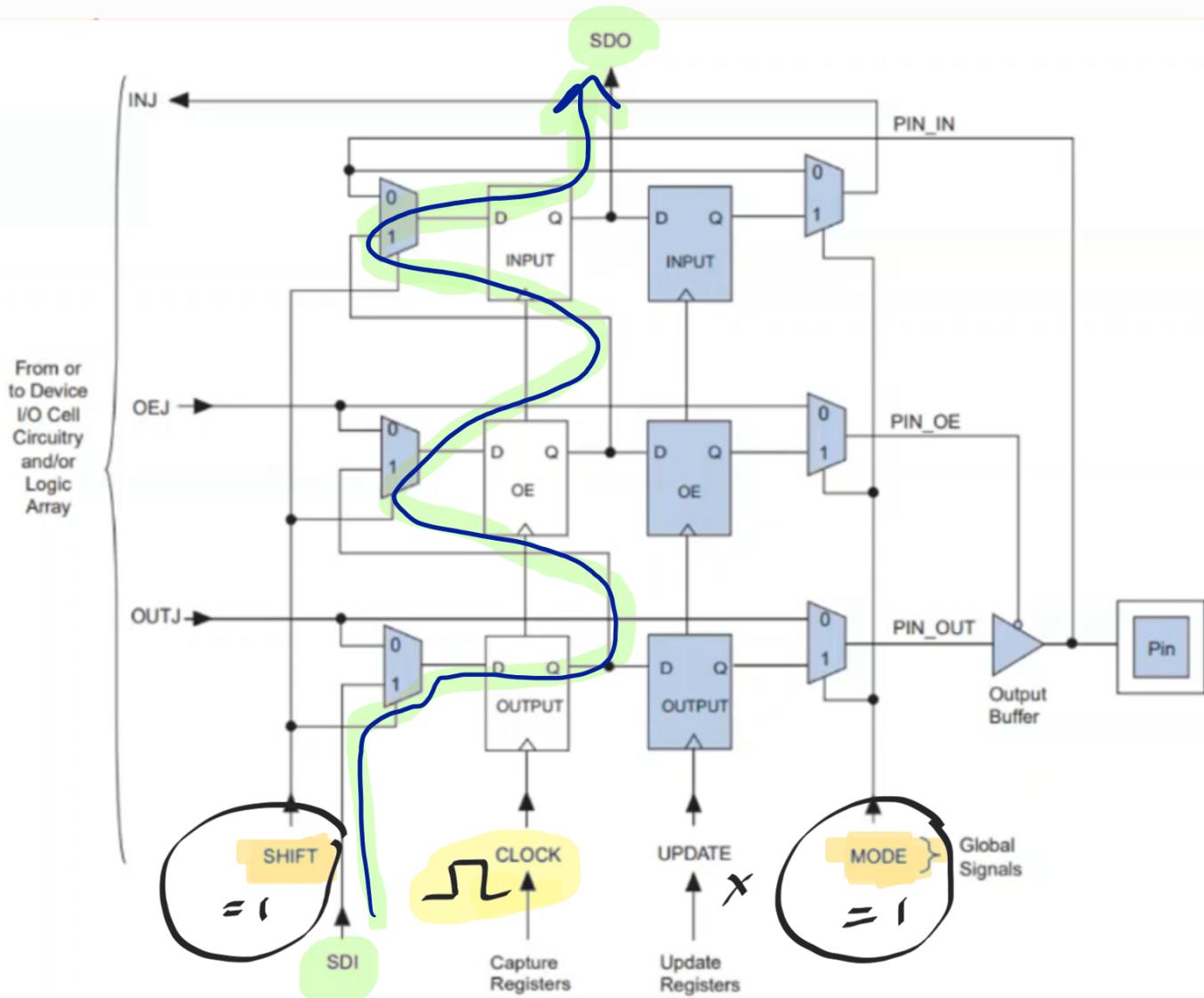


Normal  
Oper.

MODE = 0

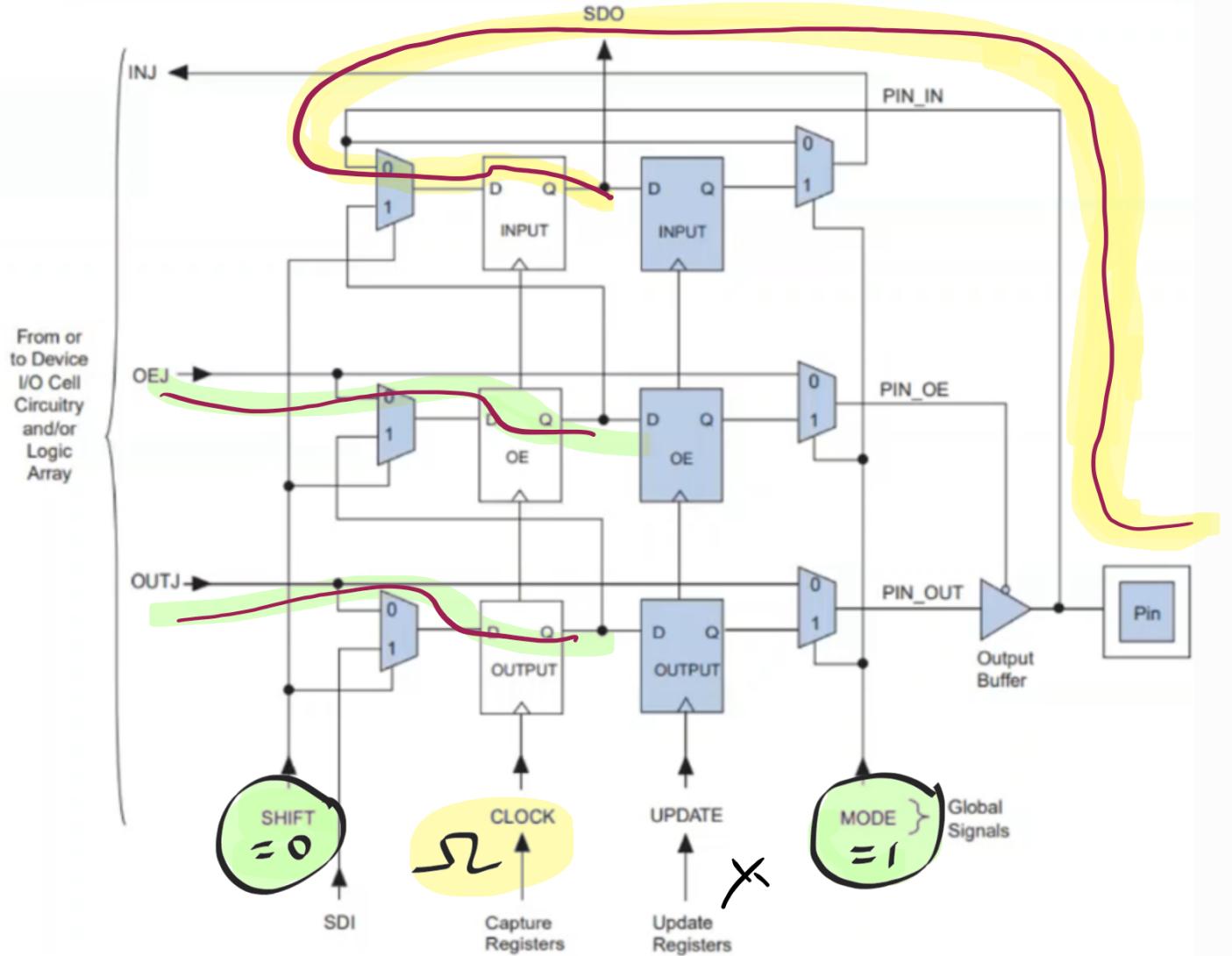


# Shift Mode : Mode = 1



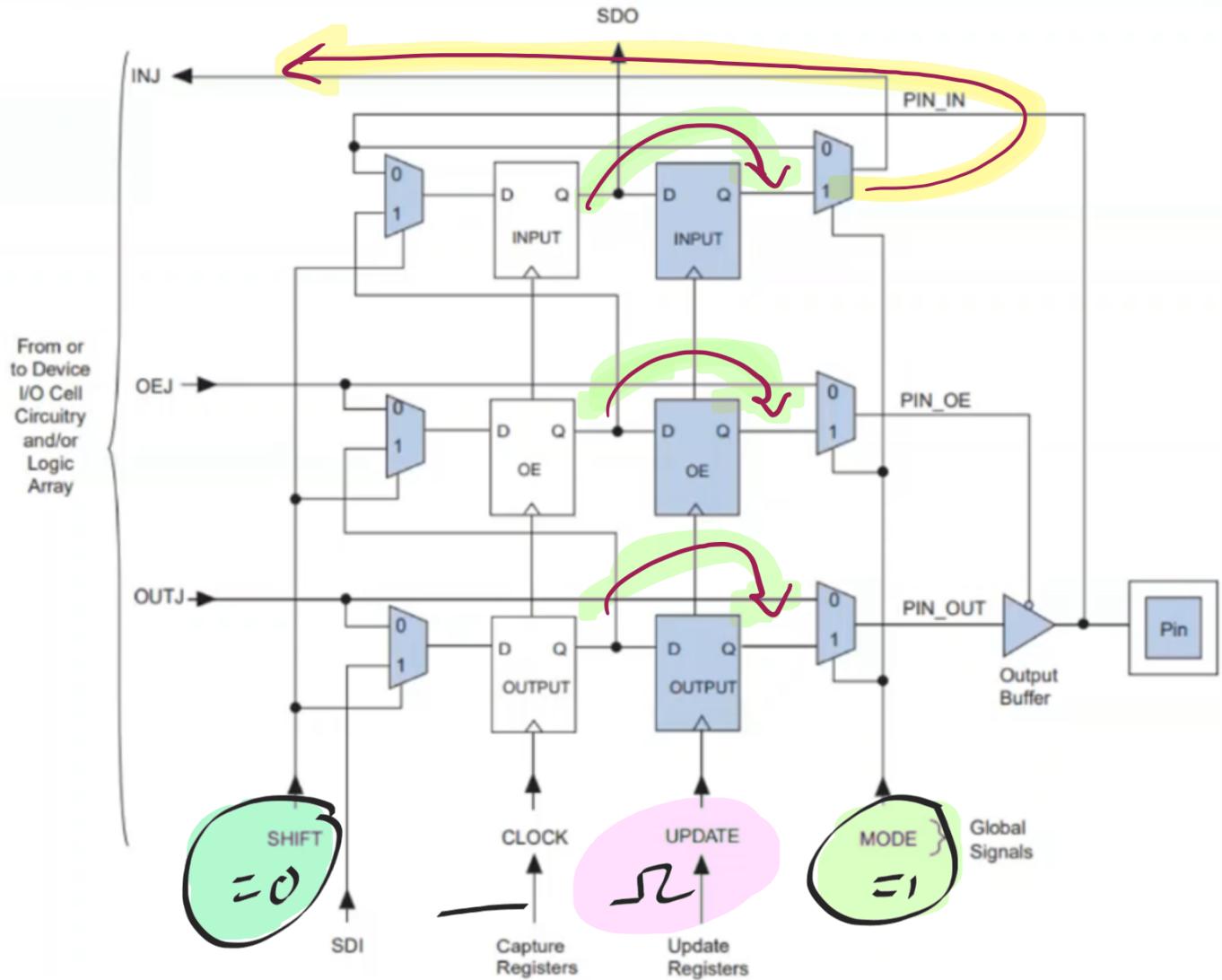
width of BSC = 3

Capture Mode : Mode = 1



UPDATE MODE: MODE = 1





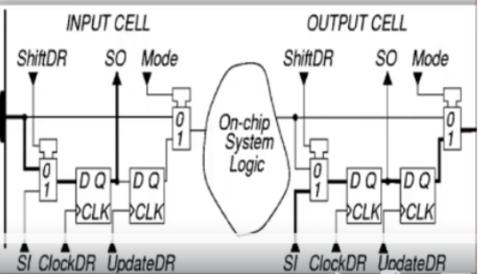
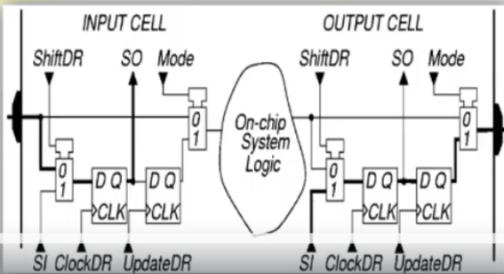
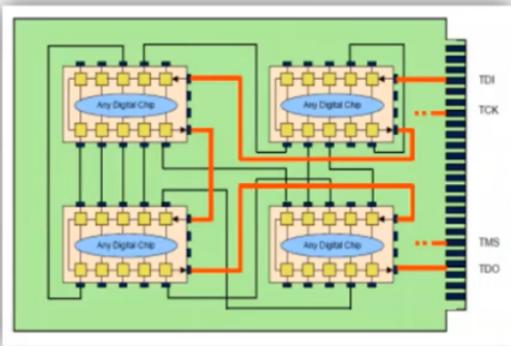
## Standard Instructions

Instruction	Selected Data Register	
EXTEST	Boundary scan	Mandatory Instructions
BYPASS	Bypass	
SAMPLE	Boundary scan	
PRELOAD	Boundary scan	
INTEST	Boundary scan	
IDCODE	Device ID	
USERCODE	Device ID	
RUNBIST	Result	
CLAMP	Bypass	
HIGHZ	Bypass	

## EXTEST Instruction

- Boundary Scan register is selected.
- Test interconnection between chips of board.
- Tests off-chip circuits.
- Fault models used are : Stuck-at faults, bridging faults and open faults.
- Test vectors shifted in boundary scan register and applied to PCB
- Vectors from boundary scan registers are captured as input vectors on other IC's

1



After  
that

Mode = 1  
Using  
shift mode  
capture mode  
update mode

2 What is a bypass Instruction?

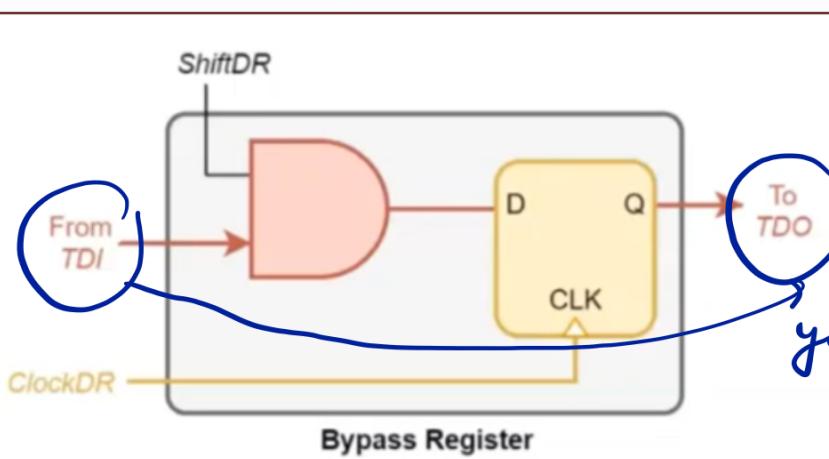
# Bypass Register is Selected.

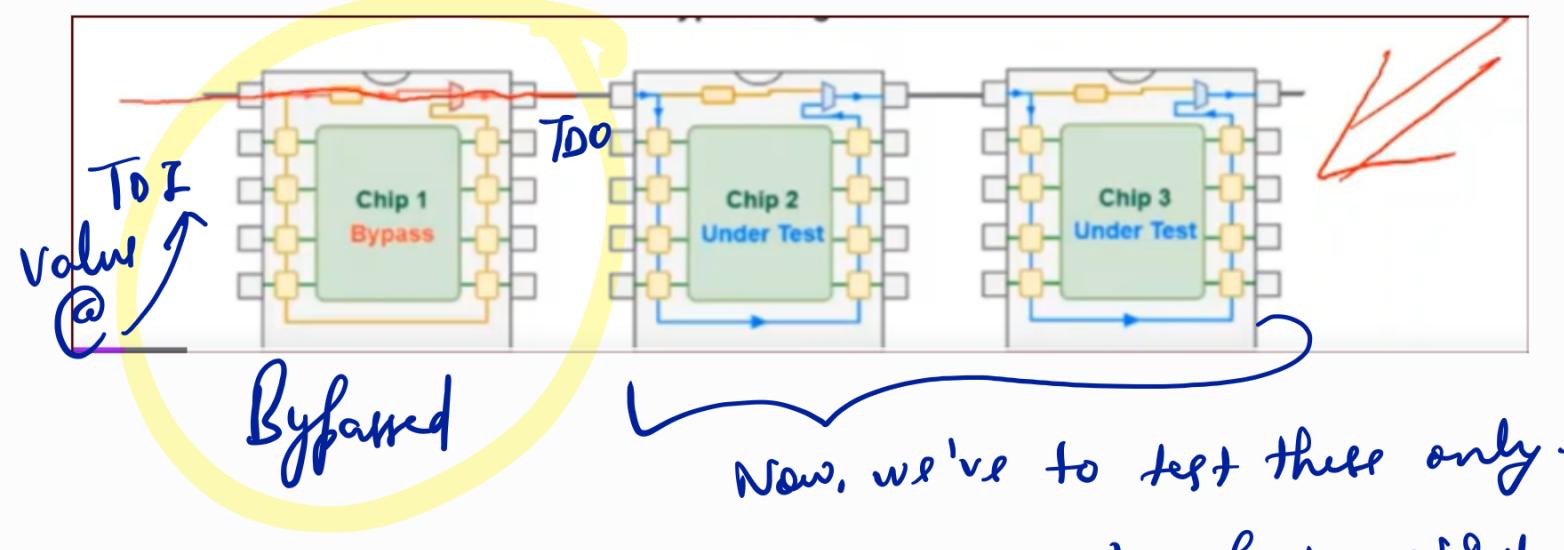
# used when one or more comp. in the

design  
needs  
to  
be

you can  
skip

Skipped.

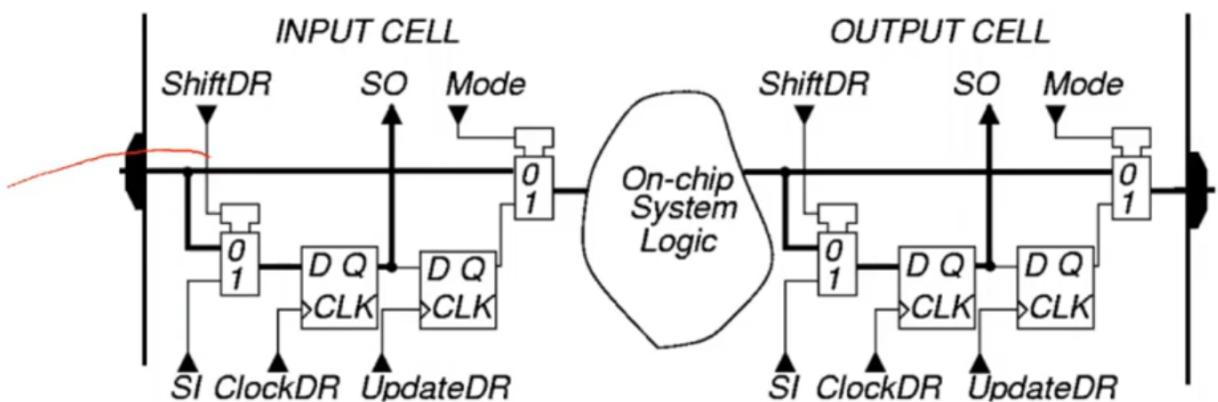




### ③ SAMPLE Instruction

#### SAMPLE Instruction

- Boundary Scan register is selected.
- Chip in functional mode  $MODE = 0$
- Samples signals entering and leaving the chip during EXTEST



### ④ Preload Instruction

#### PRELOAD Instruction

- Boundary Scan register is selected.
- Chip in functional mode  $MODE = 0$
- Preloads a pre-defined value into the Boundary scan registers before it samples signals entering and leaving the chip during EXTEST

Value before

5

## In test Instruction

### INTEST Instruction

- Boundary Scan register is selected.
- Chip in test mode
- Loads stimulus into the Boundary scan registers and captures/shifts out the response through boundary scan register.
- FSM states : ShiftDR → UpdateDR → CaptureDR → ShiftDR

TMODE = 1

6 IDCODE — - -

### IDCODE Instruction

- Device ID register is selected.
- Shifts out the pre-loaded value from Device ID register through TDO.

7 USER MODE —

### USERMODE Instruction

- Device ID register is selected.
- Shifts in and stores user defined device ID value into the Device ID register through TDI.

8 RUNBIST

### RUNBIST Instruction

- Internal BIST register is selected.
- Used to initiate internal BIST for memory or logic.
- Pass/Fail register targeted as final selected register.

⑤

## CLAMP

### CLAMP Instruction

- Initially Boundary scan register, then later Bypass register is selected.
- Used to allow the state of the signals driven from the pin to be determined from boundary scan register.

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## HIGHZ

### HIGHZ Instruction

- Initially Boundary scan register, then later Bypass register is selected.
- Used to set all the user I/O pins to an HIGHZ state.
- These pins are tri-stated until a new JTAG instruction is executed.

## Testing Connections

How we test connection between IC's ?

