1 of Videos

DFT

What is DFT?

Working of Scan chains

LOS/LOC

What is MBIST?

Vision of VLSI design → Implementing Billions/ millions of Switches in nm

→ Low Power, Area, Cost

ASIC FLOW

Design - Specification
- → Code
- → Verification

Synthesis

DFT

PD

Signoff

Tape out

Packaging & Testing

Testability:

↓

Checking defects

	Good IC	Defective IC
Pass Test	True Pass	Test Escape
Fail Test	Yield Loss	True Reject

→ Reducing them is Good Testing

PAD → Comm b/w chip & external world.

Voltage Regulators

PIN → I/P & O/P of any cell that is instantaneous in any design

PORT → I/P & O/P

Clock Gating ?

Turn off the clock to modules

ICG? Integrated Clock Gating to avoid Glitches

Use ICG Cells ← -ve level trigg latch

Latch	FF
Level	Edge
Not scan, not in library	will be scan, — —
enable s/g	Clock

DFT? Inserting test Structure into a design to detect — — defects in a chip

Process Variation ← Width, thickness Vary

Random Implant/ Imperfection

O.C.
S.C. --

Engineer Work?

↓

Don't check functionality

They check quality — —

Meta stability → O/P of Flop oscillates btw 0 & 1.

Goal of DFT Engineer

Maximization of Test Coverage
Fault "

Minimization of Test Patterns
Test time & Generation effort

W/O DFT what will you do?

Functional Testing (PI & PO) → More time & More test Patterns.

ATE Automatic Test Equipment

↳ Store Test Patterns.

PIN electronics has Comparator → Compare test result available with Golden result

Factors Consider for testing (or) Limitations of Testing

→ Chip → Not burn
Tester → should n't Damage

Crystal oscillator for better Price
10MHz to 200MHz

DFT Engineer

will take less time to check

Have more

Controllability &

Observability

Req. less Pattern to test the chip

Functional Verification

More time to check the chip.

Have less

DFT FLOW

Defect? Unintended Physical Differences

Fault? Logical Representation of Physical Defects

Error? Deviation of expected & Obtained Results.

Insertion MBIST EDT OCC Scan

Generation ATPG Patterns

Validation

Simulation - Timing

No timing → Check (Logical)

DFT → Goth

Vector → Pattern

Front-end → RTL impln

Back end → P.D.

Dff → Delay ff / Data ff

Net → Wire Connection

Netlist? → Group of Interconnections b/w Seq. & comb. logic gates.

Why ATE limits higher freq ?

b/c of high test cost

Based on Tester — How will you get high freq. ? thru PLL → (OCC) =

Verification vs Testing ?

Verifies correctness of — Functionality ⟹ Design

RTL file ⟶ Gate level Netlist ?

thru Xilinx using test benches

Mainly, Verilog ⟶ Gate Level

RTL vs Behavioral Verilog Code

Code specifies how data flows b/w Registers & Logic Gates.

Behavior of the ckt @ higher level of Abstraction, w/o specifying details of hardware Implementation

Scan Insertion

Converting → Normal DFF → Scan DFFs by

Inserting (2*1 MUX)

↓

Stitch Scan FFs to Scan chain

(q to SI path)

Scan Chain Ops?

Shifting ← SE = 1 → No. of clk = No of Pulses FFs

Scan IN
Scan Capture
" OUT

Capturing ← SE = 0 → Clk Pulse = 1

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10 FFs

Serial

Load + Capture + Unload
10 (1) (10)

21

Depend on Flop

Parallel simulation

1 + 1 + 1

3

Independent on Flop

DFT seq. less Vectors than Functional ?

$2^3 = 8$ Vectors

Only 3 vectors

Scan Insertion ? why.

To gain Controllability & Observability

Ability to drive each & every net with either 0 or 1 value

Ability to observe the response in O/P side.

DFT Condition ? / Hierarchy

Clock & Reset Sig → Drive from Top level *

Scan cells / Designs → Mux-D Scan cell

→ Clocked Scan — FF with extra Clock

→ LSSD Scan cell (2 Latches)

Level sensitive scan design

Full Partial

Partition

Scan Methodologies → Top-down Flat

→ Bottom-up Hierarchal

Full Scan → All Storage elements → Scan cells

Comb. ATPG used

Partial Scan → Subset of → Scan cells

Seq. ATPG used

Benefit

Highly Automated Effective Predictable / Assured Quality

	Scan all mode	TM	SE
Functional	Normal	0	0
DFT	Shift	1	1
	Capture	1	0

Scan Insertion Flow?

* Setup Phase Read
  Analysis " DRC
  Insertion "

Inputs	Outputs	Reports
Gate level Netlist	Scan def file	Scan all Report
Lib file	Scan Inserted netlist	" Chain "
Script / Do file	ATPG Dofile	

DRC in Scan Insertion ?

- X-Source
- Feedback Loop
- Clock Controllability
- Set/Reset
- Potential Race Cond.
- Bus Contention

Edge Mixing ✗ Domain Mixing = clock Mixing

both +ve edge flops + -ve edge flops

(ffs) with diff. scan clocks.

Control sig during (Scan Insertion)

clk, rst, SE, TE

Problems

Area overhead

Power ↑ Time ↑ Performance ↓

Tie-State Buffer: Two or more Buses drives force opp. logic onto bus.

Bus keeper: Holds Previous Value } All buses same Value

Dummy cycle: Unbalanced chains will add

Scan DEF file: tells starting flops & ending flops.

Design change format

used by PD team

Rules for Scan chain Reorder:

1. Don't Reorder flops b/w → Multiple Scan
2. ——— flops which has ↓ lock up latch b/w them — chains
3. I/P file for PD team.

Scan Sub chains → Already existing chain to Main chains → Sub Chain

Pre-existing chains →

Type of I/Ps from Designer

No. of Scan chains (1) * Channels (2) Decided how?

(1) by no. of external I/O pins

(2) external pins of chip

Why need Shifting?

To Load data in ff → After that → Capture + Shift out.

(36) Lockup latch ?

↳ Used to avoid clock skew

↳ also provide half cycle delay?

Whenever +ve x -ve flops are there is same scan chain, tool will add Lockup latch in scain chain

→ used to avoid hold violations

→ merges two diff. Clock domains in same scan chain.

LOS / LOC both test transition faults

Launch on shift / Launch on Capture

during Shift Operation (Scan mode)

(Functional mode) during capture Operation

Simpler test gene

May req. additional..

Power Consump

HIGHER

LOWER

used → Shift Clocking → Functional Clocks

Consecutive shift cycles @ high speed

OCC ? (1) w/o OCC we can't generate two pulses

On-chip Clock Controller → controls switching b/w ATE Low freq & functional freq.

→ use OCC (ckt) → to get fast clock or Max freq. internal PLL

→ types (1) Standard (2) Parent - child

OCC is inside the IP. acts like a buffer. generates pulses for intest

for extest

(3) Syn OCC
(4) Custom OCC
(5) Cascaded

OCC → fast sequential ATPG

Max. no. pulses by OCC → 6/8... * may be more.

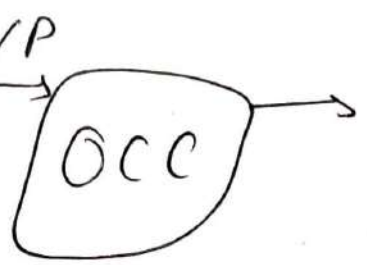
Clock Skew? Diff. b/w time taken by clk to reach (a) Capture FF (b) Launch FF

↓ due to Multiple clock domains.

→ How solve while Shifting?
(1) Use same clock domain
(2) Adding Lockup latch

Amnt. of clock from Source of the clk to Sink is Latency.

SE=1 (shift)
SE=0 (capture)



Scan-IN

Scan-out clock

TM=0 OCC will be bypass
TM=1 OCC will active

Fast_clk o/p of PLL
FAST_CAP_MODE

Mode select Sig ..

Scan-clk Scan clock (SE=1)

EDT

Embedded Deterministic Test

Disadvantage: Area overhead ↑
- Test Pattern Volume

Advantage: Test time ↓
- Data Vol. ↓
- ATE Cost ↓
- Package Cost ↓

Test time: No. of Patterns * No. of shift cycle Patterns * Clock Period of Scan clock

Test Volume: No. of Patterns * No. of ——— * * No. of channels

No. of cycles: No. of FF in (a) chain scans + (b) Masking shift Register.

No. of bits in pattern: No. of FF in (a) ↓ + (b) Scan Register

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EDT FLOW:

- Setup Phase
- Analysis Phase
- Synthesis Phase

During load
No. of shifts
↓
(a) Scan chain length with max flops + (b) Initialization Cycles

During Unload
No. of shifts → (a) Scan chain only ———

testproc file?

Procedure for → test setup
→ shift
→ Load & Unload

Scan Clock → (Seq) ← Func Clock

DFT team will decide

Design team will decide

Multiple Clock Domains?

need to insert OCC per domain.

——— . make sure lockup latch is there, if planning to mix domains

Domain mixing will do scan clocks

Compensate timing by → adding Buffers

add — . Lock up Latch

Chain Balancing → Dividing eq. No. of flops into each scan chain

↓

If Not done

→ ④ test time

→ Shifting operate @ same time.

→ All scan chains → Operate in 11 nd

Mandatory DFT Signals

Scan clock
Scan Reset
SE
TM EDT Update
EDT Clock

Signals
Channel I/P & O/P
EDT Clock
EDT Update
EDT bypass

LFSR Logic

Diagonal relation b/w adjacent bit Stream

We'll not get all possible Streams

Phase shifter logic

Better

It will Introduce more bit Stream ~~in the~~ O/P of LFSR which is given to Phase shifter.

Still we'll not get all possible combinations.

Hence patterns are given from external Logic. (ATE)

X-Propog. if there are some black boxes they aren't bypassed during ATPG

Use Masking Logic

Why decoder? So that Less I/Ps → more no. of Outputs

XOR decoder → used X-masking

whichever scan chain is prop. X it will mask those scan chains by masking the other I/P of AND = 0

One hot decoder? → do debugging

Enable only one scan chain at a time.
& MASK other scan chains.

When / Why Patterns fail

→ go for one-hot decoding

during

(a) Simulation (Mismatch in Lib file, Netlist, Database)

(b) Manufacturing → (defect)

Use of Bypass Lockup Latch added whenever positive by followed -ve flip flops

during bypass

Head Lockup Latch? → Added bcz of Domain Mixing. So, stg moves for EDT clock domain to Scan clock domain

Tail Lockup Latch: → Added bcz of Compressor Logic or domain mixing

Whenever we have pipeline flops.

Comparator? Basic.

→ Basic ? Allow one / All Scan chains based on mode bit

→ Xpress ? 1 Hot Masking / X Masking based

Link →
↓
Libraries
↑
Target →

Except (EDT Clock) All other pins can be shared with functional pins

↓

If +ve triggered & internal chain clk → -ve trigg

↓

then test Compress adds 2 Latches

EDT

I/Ps
Library file

O/Ps
EDT ~~pattern~~ Dofile

DRCs you faced in EDT?

K5
K9
K13
K19

K20
K21
K22

D5
D7

E4
P65

Test Compression Ratio?

No. of Internal Chains / No. of External Chains

How to decide?
Check with functional Team
Should get the equal Scan chain length by varying

Vector	Pattern
for Logic Simulation	Fault Simulation.

Test Cost: → depends on Test Time & no. of Chips we can test at a time.

Test Plan: Document → Prepared before execution of DFT Project by DFT lead.

→ tells about

(a) List of blocks
(b) Overall Architecture
(c) How its interlink with other block.
(d) Clock Diagram
(e) Reset Structure
(f) List of DFT related ports
(g) List of Blocks for Scan.
(h) If there exist any third party IP

b/g of tester we use (slow) scan clock *shift for shift.

Scan Clock freq. 25 MHz

High freq may burn Chip.

No of test Clock ↓ by No. of functional Clocks that are controlling a block

Fault Models we've: SA, TDF, PDF, IDDQ, CA

Bridging, Small Delay Defect.

How to find fault?

1. Assume a fault
2. Try to get opp. value on same net by driving logical operation
3. Apply values at input of logic & Justify the Output of Circuit.

Fault Categories

1. Dominance
2. Equivalence
3. Collapsing

Fault Aliasing? If two uncompressed signatures have the same compressed signature

Type of Algor. Involved:

a. D Algo
b. PODEM – Path Oriented Decision Making
c. FAN : A Fan oriented
d. SCOAP – Scandia Controllability & Observability Analysis

FAULT
a. Activation
b. Propogation
c. Justification

COVERAGE will be calculated in → in Capture Phase

Program

→ Lock up latch → Solve problem during → Shift Phase

→ Redundant Logic → No controllability.
which has

ATPG

Testable
Detected
Pos Detected
ATPG Untestable
Undetected

Un Testable faults.
Unused
Tied
Blocked
Redundant

Test coverage % Fault Coverage :

Total no. of → Detected faults / Total faults Testable > ____ / Total faults in Circuits

How to classify Pattern? based on

(a) Format (a) Verilog Pattern (b) STIL (c) WGL (d) Pat+DB

(b) Categories (a) Basic (b) Clock Sequential

(c) Type (a) Chain (b) Mixed (c) Serial

Parallel Patterns	Serial Patterns
Run time → Less	More
Debug → Easy	Difficult
Industry need Parallel Patterns	Testers req. Serial Pattern.

Stuck at faults: bcz of Dust Particals, Material aging effect, Breaking of Wire & PIN

All events occurs in one Pattern?

Load SDi;
Force Pi;
Measure PO
Capture,
Unload SDO

Test Point Insertion? → we add → (to improve) Coverage

To improve cont. & obs we add a flop / MUX

I/Ps → memory models / bisr order file

MBIST → Memory Built in Self Test

O/P → mbist sdc, mbist inserted netlist

Fault Models

1. Single Cell
   - (A) Stuck at faults
   - (B) Transition faults
2. Double Cell
   - (A) Coupling
   - (B) Inverse Coupling
   - (C) Idempotent
3. Address Decoder fault
4. Active NPSE
5. Passive NPSE

} Neighbourhood Pattern Sensitive fault:

Group Memories in a Controlled in ?

(Clock domain / Power domain / RAM / ROM / Physical diff.)

ALGORITHMS

- Zero-one Algo.
- Checker-board Algo.
- March ——
- Mats ——
- Mats + ——
- Mats ++ ——
- March X ——
- March C ——

SCAN INTEST/EXTEST

to test Core logic

to test interconnection blw two blocks of same chip.

SE = 1 in intest always in shift mode for both I/Ps & O/P wrapper cells. (both shift & capture)

In EXTEST for I/P wrapper cells both shift & capture

for O/P wrapper cells → always shift mode

During Scan Extest:

↳ The core flops Clock/rst → Should be Inactive

Clock gating

BIST?

↳ Autom- -test Memories {Also you can provide memory patterns on testers.

Wrapper? To → check Interconnections b/w blocks

↳ used

Boundary Scan? To check interconn - — b/w chips

Tessent MBIST FLOW:

Load the design specific requirements

Create & process DFT specification

Extract ICL

Create & Process Pattern specification

Simulate & Validate

Wrapper Insertion ATPG process on very large & complex design can often be unpredictable

Wrapper Chain? → series of scan cells connected to the boundary of design.

↳ They are scan chains around the periphery of a block that connect to each I/P & O/P of block to be tested.

Wrapper core? → term applies to physical blocks

↳ Purpose of wrapping a core is to isolate its internal logic.

Dedicated Wrappers: Inserting wrapper cell on I/O's adding new wrapper cells but they will (↑) Area overhead.

↓ solve by using Shared Wrappers.

Shared Wrappers?

Re-using the existing flops ←

Intest

Logic located within the Wrapper chain is tested during internal testing of core

Extest

outside

external

Joint Group Test Action → JTAG | IJTAG | Boundary Scan

1149.1
for board level testing
→ to test interconnection b/w two chips

Mandatory Instructions
- Bypass
- Sample
- Preload
- Extest

PINS
- TMS
- TCK
- TDI
- TDO
- TRST (optional)

To reset with TRST,
Set [TMS=1 for 5 TCK clock cycles]

FSM
16 States

EXTEST ?
→ Sample/Update
→ Preload
Chip 1

INTEST
if you do preload & Sample on same chip
→ Instruction code (all 0's)
Chip 2
Capture/Shift
Sample

10 Chips on board
To select 3rd chip ?
First 2 & 4-10 bypass

In Bypass Mode, Why we need a flop b/w TDI --> TDO path?
why we can't directly connect TDI to TDO right?
if flop isn't there, we can't predict when data will be valid for the 2nd chip.

JTAG? Standard Arch. to test the device easily.

having
TAP
TAP controller
Registers
Instruction Set

Data Registers in JTAG?
Boundary Scan
Bypass Register
Identification Register *

Working of TAP FSM: 16 State

→ works under control of TCK & TMS.

→ under +ve TCK edge of → every transition from one state to another occur. with the help of TMS.

→ under -ve edge of TCK it is updated to TDO.

① Test logic reset
② Run idle
③ Select DR scan
④ " IR "
⑤ Capture
Shift
EXIT 1
Pause
EXIT 2
⑩ Update

Provides shortest path

How initialize TAP FSM?
by making TAP to wakeup in Test-logic-reset State

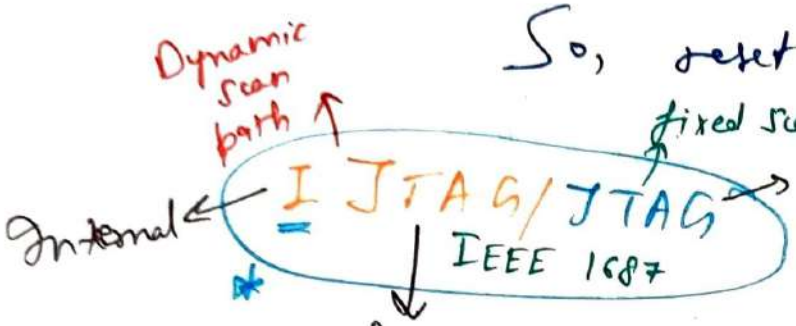
उसको सीधी किसी और State में wake up कि उस से give 5 1's

Bypass Register? is a Data Register which reduce the distance b/w TDI & TDO when Chip is idle.
reduce no. of Clock Pulses

Why reset is optional in JTAG?

by giving consecutive 1's on TMS reset occurs.

So, reset is optional.



have SIB (Segment Insertion Bit)

which makes bypass possible and Resetting easy while forcing

saving the number of Test cycles & Test time.

allows selective inclusion or exclusion of segments.

Simulation

To Validate Pattern that are generated during ATPG

Or wherever we've unconnected internal cut Points do *

ATPG Automatic test Pattern Generation

for a given Fault Model. ← to find ← Manufacturing defects in Real Silicon.

↓

Produce → fault coverage Report

I/Ps	O/Ps	Reports
Lib file, EDT_top-gate.v	Fault List	Scan cell & Scan Chain Reports
EDT.dofile, Script file	Pattern file	

ATPG FLOW?

Setup phase → TOOL → never measure Current

↓

Analysis phase